Millimeter-Wave/Terahertz Circuits and Systems for Wireless Communication

Siva Viswanathan Thyagarajan

Electrical Engineering and Computer Sciences
University of California at Berkeley

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by

Siva Viswanathan Thyagarajan

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Committee in charge:

Professor Ali M. Niknejad, Chair
Professor Elad Alon
Professor Paul K. Wright

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Abstract

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The ubiquitous use of electronic devices has led to an explosive increase in the amount of data transfer across the globe. Several applications such as media sharing, cloud computing, Internet of things (IoT), big-data applications demand high performance interconnects to achieve high data rate communication. The mm-wave/terahertz band offers several gigahertz of spectrum for high data rate communication applications. This thesis explores millimeter-wave/terahertz circuits and terahertz systems for various applications in CMOS technology. Some of them include links for personal area networks, wireless backhauls, chip to chip communication (short-range) links in form factor constrained devices (wireless in a box) and also for long-range high-speed communication (using phased arrays or lenses).

In particular, this research explores the feasibility of millimeter-wave/terahertz systems and also the performance of critical blocks such as power amplifiers. A linear power amplifier is designed in a deeply scaled technology node (28 nm) and the various challenges in the design process are discussed. The performance is validated using measurement results and compared across various technology nodes. Non-linear millimeter-wave switching power amplifiers are also explored due to their high efficiencies and a prototype is fabricated to verify the modeling and simulation results.

The ideas and modeling strategies from the individual blocks are used in the design of mm-wave/terahertz transceivers. Simple modulation schemes such as on-off keying, binary phase shift keying and quadrature phase shift keying are used for transmission of data. Two transceiver prototypes with different transmitter and receiver architectures are fabricated in bulk CMOS technology. The system level considerations and architecture choices are discussed. Theoretical analysis of critical blocks with design choices are explained along with their implementation details. The system level measurements from the two transceivers confirm the feasibility of such links at millimeter-wave/terahertz frequencies. The work from this thesis demonstrates the world's first fully functional link at frequencies greater than 200 GHz in CMOS technology.

To my parents, brother, sister, extended family and mentors

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Chapter 1

Introduction

The ubiquitous use of various electronic devices ranging from laptops, mobile phones, tablets, etc has tremendously increased the connectivity across the globe. Media sharing such as videos and music, online gaming, video chatting and social networking have led to a dramatic rise in the data transfer between devices. It is predicted [1] that by 2017, there would be 1.4 zettabytes of data being shared across the globe. Around 3.6 billion people would be online and the number of connections would increase from the current 12 billion to 19 billion. There would be a 79 % growth in the number of smart phones and 104 % in the tablets leading to increased connectivity and data sharing. Such high data rate transfers would require very high throughput, dense chip-to-chip interconnects in high performance computing, cloud computing, laptops and mobile phones. On the wireline front, today's electrical links can deliver close to 25 Gbps of data at energy efficiencies of 2-4 pJ/bit [2][3] and several demonstrations of data rates beyond 30 Gbps have also been shown [4][5]. However, increasing the data rates further results in lower energy efficiency due to the bandwidth limitations of the channel. On the optical domain, data rates close to 20 Gbps have been demonstrated [6]. However, the performance of these links is generally affected by the high laser power and temperature sensitivity of the devices. Today's wireless 4G LTE standards allow data rates of 30 Mbps to peak values of 100 Mbps for mobile smart phones [7]. With the latest 3GPP release in December 2014, these values would increase to a maximum of 1 Gbps. Thus, the increased data transfer in the future requires high bandwidth interconnects for high performance computing, data centers and mobile applications.

The millimeter-wave (sub-terahertz) and terahertz bands offer tremendous potential to achieve this target due to the availability of several gigahertz of spectrum in the band. Fig. 1.1 shows the electromagnetic spectrum. The millimeter-wave/terahertz region is defined from 30 GHz to 3 THz based on the wavelength of the electromagnetic wave. Electronic devices have been mainly operating in the low frequency regime of this spectrum and their performance degrades as one approaches their cut-off frequencies. Today's CMOS technologies have typical cut-off frequencies of $\sim$ 200 GHz. On the other hand, there has been significant

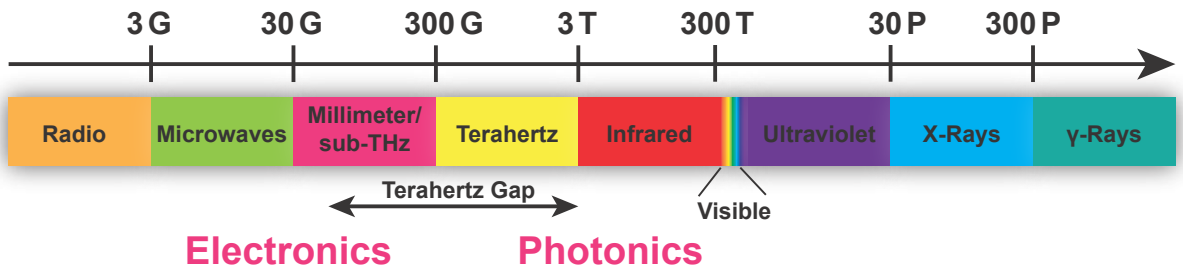

Figure 1.1. Electromagnetic spectrum showing the millimeter/terahertz region

work in the photonics domain at frequencies greater than 3 THz in the infrared region. The photon energy ($E = h\nu$, where h is the Planck's constant and ν the frequency) starts reducing as one approaches closer to the lower end of the infrared region. Hence, a significant proportion of the electromagnetic spectrum is unexplored starting from 50 GHz to 3 THz and is popularly referred to as the terahertz gap. Recently there has been significant interest in the 60 GHz band for high data rate communication in both outdoor and indoor networks. The millimeter-wave/terahertz band is also becoming popular for imaging applications at 94 GHz, 140 GHz and 220 GHz [8]. Applications in the automotive radar industry in the 77-78 GHz band are gaining interest for blind spot detection to minimize accidents. Terahertz chemical imaging or molecular spectroscopy is another emerging area of application where certain substances can be detected based on their high degree of absorption at these frequencies. This can be used to detect harmful gases such as carbon monoxide (which has response at 230 GHz) or phosphine (which has response at 266 GHz). This work inspects the millimeter-wave/terahertz band for communication applications and discusses various circuits and system designs at these frequencies.

1.1 Communication in the 60 GHz band

As described earlier, the 60 GHz band (V-band) is becoming popular for commercial products due to the availability of 7 GHz of unlicensed spectrum from 57 GHz to 64 GHz. This would allow very high data rate communication in applications such as personal area networks (PANs) for media sharing and wireless backhauls as shown in Fig. 1.2. The WiGig standard (IEEE 802.11ad) [9] which is now part of the Wi-Fi alliance allows the whole band to be used in time division duplexing (TDD) mode thereby allowing high data rates. This could be used for streaming high-definition video and transferring files across electronic devices. Today's technology with 802.11ac Wireless LAN standard can support a maximum of 2.5 Gbps with three 160 MHz channels and 256-QAM data rate. In contrast, the 60 GHz band can provide maximum throughputs of up to 10 Gbps at higher energy efficiencies compared to nJ/bit numbers from Wireless-LAN. The V-band could also be used for supporting backhaul networks. With the average backhaul data rate scaling up from 35 Mbits/cell to 1 Gbits/cell in the next five years [7], the millimeter-wave links would handle a significant

Figure 1.2. Millimeter-wave/terahertz networks for personal area networks [left] and wireless backhauls [right]

share of the data transfer. This is made more feasible with the recent Federal Communication Commission (FCC) modifications [7] for the maximum allowed transmission power for outdoor communication applications. The modification allows an equivalent power transmission of up to 82 dBm with an antenna gain of 51 dBi which could easily provide wireless network connectivity over a mile of distance. Additionally, operation at millimeter-wave frequencies allows one to use phased-array antennas that allow robust communication over long distances.

CMOS is usually the preferred technology for these applications due to its low cost and continued scaling that allows transistors to be operated in gigahertz range. However, Moore's law driven by digital circuits is detrimental to the design of high power millimeter systems. There have been several demonstrations of 60 GHz transceivers that achieve very high data rates with reasonable efficiencies. One of the critical blocks that determines the overall system efficiency of a mm-wave transceiver is the power amplifier (PA). The design of the PA is especially challenging due to several issues. The low breakdown voltage of transistors and their reduced supply voltages severely limit the output power of the PA. Several on-chip power combining techniques need to be employed to overcome this issue and this leads to degradation in the overall efficiency. Additionally the PA must be designed to be wideband in nature to account for process variations. In this work, the design of a linear wideband power amplifier has been explored in scaled 28 nm CMOS technology. Switching power amplifier architecture has also been explored as an alternative to linear PAs in constant envelope modulation scheme transmitters. The design of an inverse class-D power amplifier has been discussed with measurement results.

Figure 1.3. Futuristic flexible device with wireless interconnects

1.2 Communication beyond 100 GHz

The 60 GHz band offers potential for high speed applications. However, to achieve even higher data rates, this research explores frequencies beyond 100 GHz into the terahertz regime. Todays smart phones and tablets incorporate multiple radios (GPS, Bluetooth, 4G LTE, etc) and signal processing units (multi-standard baseband, graphics and CPU) on a single board. Given the form-factor constraints of such a handheld portable device, the high density of integration of these features has become a serious design challenge. One might be able to achieve smaller interconnect footprints and greater flexibility instead by employing short-range wireless links that could replace or complement wired buses, thereby utilizing the available extra space for other features (like high battery capacity).

An equally important application of directional high-data rate wireless interconnects can be envisioned to serve as wireless backhaul networks in data centers. As described earlier, there is a continued demand for high data rates and by the next decade, data rates for the server I/O and core networking are projected to increase to about 100 Gbps and 1 Tbps respectively [10]. This would be a serious bottleneck for the cloud and would require advance hardware resources, often at a steep cost. Therefore, during intermittent periods of heavy data, wireless links could be deployed to ease congestion. Such links would assist the wired network and provide both bandwidth and flexibility to simultaneously transport huge amounts of data. Such links at 60 GHz are already being deployed in industry data-centers [11][12]. Sub-terahertz wireless interconnects with significantly higher data-rates can be

Figure 1.4. Flexible device can be upgraded by attaching two such devices and the chips communicate with each other wirelessly

achieved by using directional links. Leveraging the well-controlled data center environment can enable the implementation of extremely efficient point-to-point links.

One of the futuristic visions of this work is a device shown in Fig. 1.3. The device is a flexible tablet with a display on it. Here chips are placed in their respective slots and there is only power routing through the flexible device. After being powered on, the chips talk to each other using wireless communication and the whole device can be upgraded on the fly as in Fig. 1.4. As the device is flexible, the wireless interconnect solution is a more feasible option compared to wireline or optical. However, this would only be possible when the chips are low cost and efficient. This work therefore focuses on the design of sub-terahertz systems in CMOS technology due to its low cost and the ability to leverage its digital interface. By operating at these high frequencies, the antennas can be integrated on the die thereby further reduced packaging costs. However, the design at these frequencies is faced with various challenges and requires innovations both at the circuit and system level. The design of these sub-terahertz systems also incorporates ideas from the V-band PA designs described earlier.

1.3 Organization of the dissertation

The primary goal of this dissertation is to explore feasibility of millimeter-wave and terahertz circuits and transceiver systems in bulk CMOS technology. The dissertation covers three basic aspects of design. It includes the theoretical analysis and modeling of various critical blocks using simple analytical expressions that allow the designer to understand the design trade-offs and arrive at a more efficient design. Secondly, designs are explored at the individual block levels to verify the modeling approaches and also observe performance trends with technology scaling. Finally, these ideas are incorporated into the design of a complete transceiver operating at sub-terahertz frequencies. In Chapter 2, we discuss the design, implementation and measurement results of a 60 GHz power amplifier in 28 nm CMOS technology. In Chapter 3, we discuss the system level considerations in the design of a complete sub-terahertz system. In Chapter 4, we cover the design of an inverse Class-D switching power amplifier with block level measurement results. This PA is then integrated into the first prototype of a sub-terahertz transceiver operating at 260 GHz. The measurement results of the system are discussed. Chapters 5 and 6 bring out the shortcomings in the first prototype and describe a power efficient sub-terahertz transceiver operating at 240 GHz with measurement results. Concluding remarks are provided in Chapter 7.

Chapter 2

A 60 GHz Wideband Power Amplifier in 28 nm CMOS

The 60 GHz band with its 7 GHz of unlicensed spectra is a potential solution for high data-rate communication systems in applications such as personal area networks (PANs) and wireless backhauls. Due to the low cost of CMOS technology and its continued scaling in the last decade, transistors can now be operated at high frequencies. However, Moore's Law driven by digital circuits is detrimental to the design of high power RF and mm-wave systems. There have been several demonstrations of 60 GHz transceivers that achieve very high data rates with reasonable efficiency numbers [13–16]. One of the critical blocks that determines the overall system efficiency of a mm-wave transceiver is the power amplifier (PA) [17][18].

The design of the PA is especially challenging due to several issues. The low breakdown voltage of transistors and their reduced supply voltages severely limit the output power of the PA. Several on-chip power combining techniques need to be employed to overcome this issue and this leads to degradation in the overall efficiency. The IEEE 802.11ad standard defines the multi-gigabit wireless communication at 60 GHz and offers the unlicensed band from 57 to 63 GHz for communication in the United States of America. In order to cover this entire band and account for process variations, the PA must be designed as a wideband system with high efficiency and gain. The PA and all the other transmitter blocks must also be made broadband if the same unit needs to be used across the world to cover the WiGig band from 57 to 66 GHz. The improved transition frequencies of the devices provides a partial benefit in this respect. In addition to the above, the stability of the PA is of major concern. Hence, the design of an efficient, high power, stable, wideband PA in a scaled technology node is challenging.

In this chapter, we discuss the design of a linear wideband PA implemented in 28 nm

bulk CMOS technology [19][20][1]. Due to increased coupling between the drain and source nodes (due to scaling), stability of the PA is of concern and is addressed using a drain-source neutralization technique. The design also utilizes low-k transformer techniques to achieve a wideband PA with 11 GHz bandwidth. To achieve a high output power of 16.5 dBm, the design uses transmission line based power combining networks. Section 2.1 discusses the 28 nm technology node by qualitatively comparing it with 65 nm and also describes the modeling of active and passive devices in this technology. Section 2.2 explains the drain-source neutralization technique and low-k transformer networks and also discusses the circuit details of the PA. The measurement results are shown in Section 2.3 and concluding remarks are provided in Section 2.4.

2.1 28 nm technology : Actives and Passives

Scaling to 28 nm technology node improves the transition frequency (f_T) of the devices and these typically range around 250 GHz. This serves as an important metric in mm-wave applications where the data rates are in the Gbps range. In addition, the blocks must be designed to be broadband in nature as there is no convenient way to compensate for process and temperature variations (such as capacitive tuning at lower frequencies). Another important parameter that determines the maximum achievable gain from an active device is the maximum oscillation frequency (f_{max}). The f_{max} can be related to the f_T [21] as

$$f_{max} = \frac{f_T}{2\sqrt{R_g(g_m C_{gd}/C_{gg}) + (R_g + r_{ch} + R_s)g_{ds}}} \tag{2.1}$$

where R_g is the gate resistance, g_m the transconductance, C_{gd} the gate-drain capacitance, C_{gg} the total gate capacitance, r_{ch} the channel resistance, R_s the source resistance and g_{ds} the output conductance of the active device. Due to scaling, the gate resistance of the device degrades (as the thickness reduces) and the ratio C_{gd}/C_{gg} also increases. Although the f_T of the technology improves, the benefit gained in f_{max} due to scaling is marginal. Hence, the achievable f_{max} of the 28 nm technology node is comparable with that of 65 nm. Thus, the maximum achievable gain G_{MAX} of the device is around ∼11-12 dB per amplification stage if one utilizes a common-source structure. The scaled power supply and low breakdown voltages offered by CMOS technology also severely limit the achievable output power levels and efficiency of PAs. In order to achieve high output power, one has to resort to on-chip power combining techniques where power from several unit PAs are combined using on-chip passive networks. This design also utilizes cascode devices to achieve higher gain and output power.

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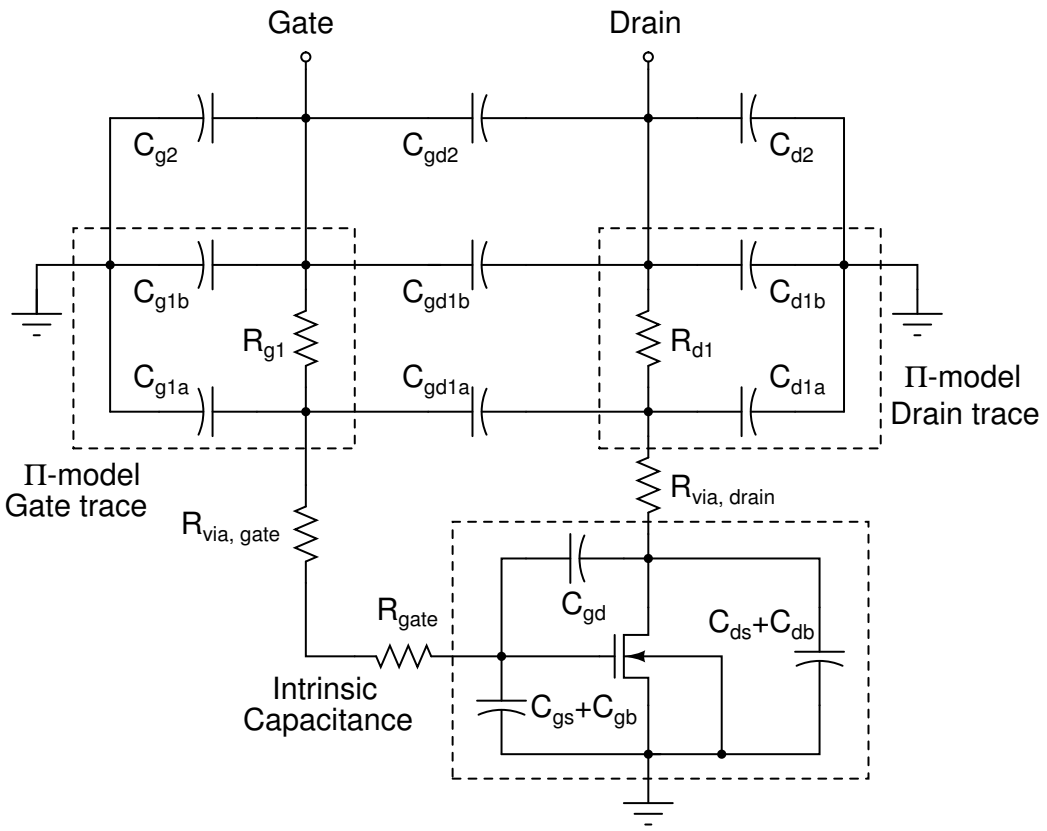


Figure 2.1. Model of unit finger of the active device

The modeling of active devices plays a critical role in determining the overall performance of the PA. The model of the active device capturing the various layout parasitics is shown in Fig. 2.1. Modeling the device at the schematic level with the added parasitics allows one to have a scalable model for design optimization and also reduces the simulation time. The model consists of the intrinsic capacitances C_{gd}, C_{gs}, C_{gb}, C_{ds} and C_{db} between Metal 1 - Metal 1, Metal 1 - Gate and Metal 1 - Ground. The gate resistance is then modeled using R_{gate} whose value is determined from measurement results. $R_{via,gate}$ and $R_{via,drain}$ model the finger gate via resistance and finger drain via resistance respectively. This is followed by a Π-model of gate and drain traces ($C_{g1a}, C_{g1b}, R_{g1}, C_{d1a}, C_{d1b}, R_{d1}, C_{gd1a}, C_{gd1b}$). Multiple sections can be added for higher accuracy. The final gate and drain buses on the top metal are modeled using C_{g2}, C_{d2} and C_{gd2}. This unit active device model is replicated NF times, where NF is the number of fingers. Careful layout of the active device minimizes the trace lengths and parasitic inductances due to the vias. Hence, no inductance is added as part of the core model. The capacitances in the core model are estimated using parasitic extraction tools. Fig. 2.2 shows the simulated intrinsic wiring capacitance ratio as a function of number of fingers (NF) ($W = 1\,\mu$m) and width ($NF = 8$). In both cases, we observe that the drain-to-source capacitance (C_{ds}), gate-to-drain capacitance (C_{gd}) and gate-to-source capacitance (C_{gs}) are comparable. As the C_{ds} is a dominant portion of the wiring capacitance, it plays an important role in determining the stability of the amplifier as discussed in the next

section. We also observe that the ratio C_{gd}/C_{gg} is close to 1/2 and this is one of the factors determining the f_{max} in this technology as discussed above. The same circuit is also used for modeling the cascode device. However, in this case, a diode (representing the p-substrate n-well p-n junction) must be added from the source of the cascode transistor to the ground node to accurately predict the PA performance.

With regard to passive devices, this technology node offers one thick metal layer whose current carrying capacity is comparable to that of the 65 nm node. However, due to the scaling of the metal thickness, the sheet resistance of the lower metal layers is 2-3X worse. The shrink in the lower metal stack moves it closer to the substrate and hence increases the loss contribution due to its conductive nature. The electromigration rules for the lower metal layers are also a factor of 2X worse compared to 65 nm technology node. This requires strapping of the lower metal layers and thus results in higher layout parasitics. Due to the stringent requirements with regard to metal density, passive devices such as inductors/transformers must include dummy metal layers from Metal 1 to the top metal. The layout of a transformer with dummy filling is shown in Fig. 2.3. The dummy fill adds a loss of 0.3-0.4 dB per matching stage due to eddy current losses. Complicated design rules along with the aforementioned issues make mm-wave design in this technology node challenging.

As described before, the active device is simulated using the model in Fig. 2.1 whose parameter values are in turn obtained from RC extraction. The connection traces along with the rest of the passives are simulated using High Frequency Structure Simulator (HFSS). The combiner/splitter transmission lines (to be described later) are implemented using the ultra thick metal layer. The transformers are implemented using vertically coupled spiral inductors on the thick metal and alucap layers. Fig. 2.4 shows the simulated inductance and quality factor of single loop inductors as a function of the outer diameter and width. The simulated quality factor averages around 18 at 60 GHz. Changing the inductor trace width shows no appreciable variation in the quality factor of the inductor (as the loss is dominated by the skin effect at these frequencies). The self-resonant frequency of the single loop inductor varies from 300 GHz to 100 GHz as the diameter is changed from 30 μm to 150 μm. As the quality factor is a weak function of the trace width, a trace width of less than 6 μm is used for all the transformers to obtain a high self resonant frequency, thereby reducing the variation in the inductance values.

2.2 Power Amplifier Design

In this section, we describe the design of the power amplifier. The power amplifier comprises of three stages that are cascaded together using transformer networks. Fig. 2.5 shows the complete circuit diagram of the 60 GHz power amplifier. In order to achieve high output power, the design employs two cascode output stages that are combined using transmission line based power combining networks. In order to mitigate the stability issue in this technology node, a drain-source neutralized cascode stage is proposed. The design also uses low-k transformer networks to enhance the bandwidth of the amplifier. A single

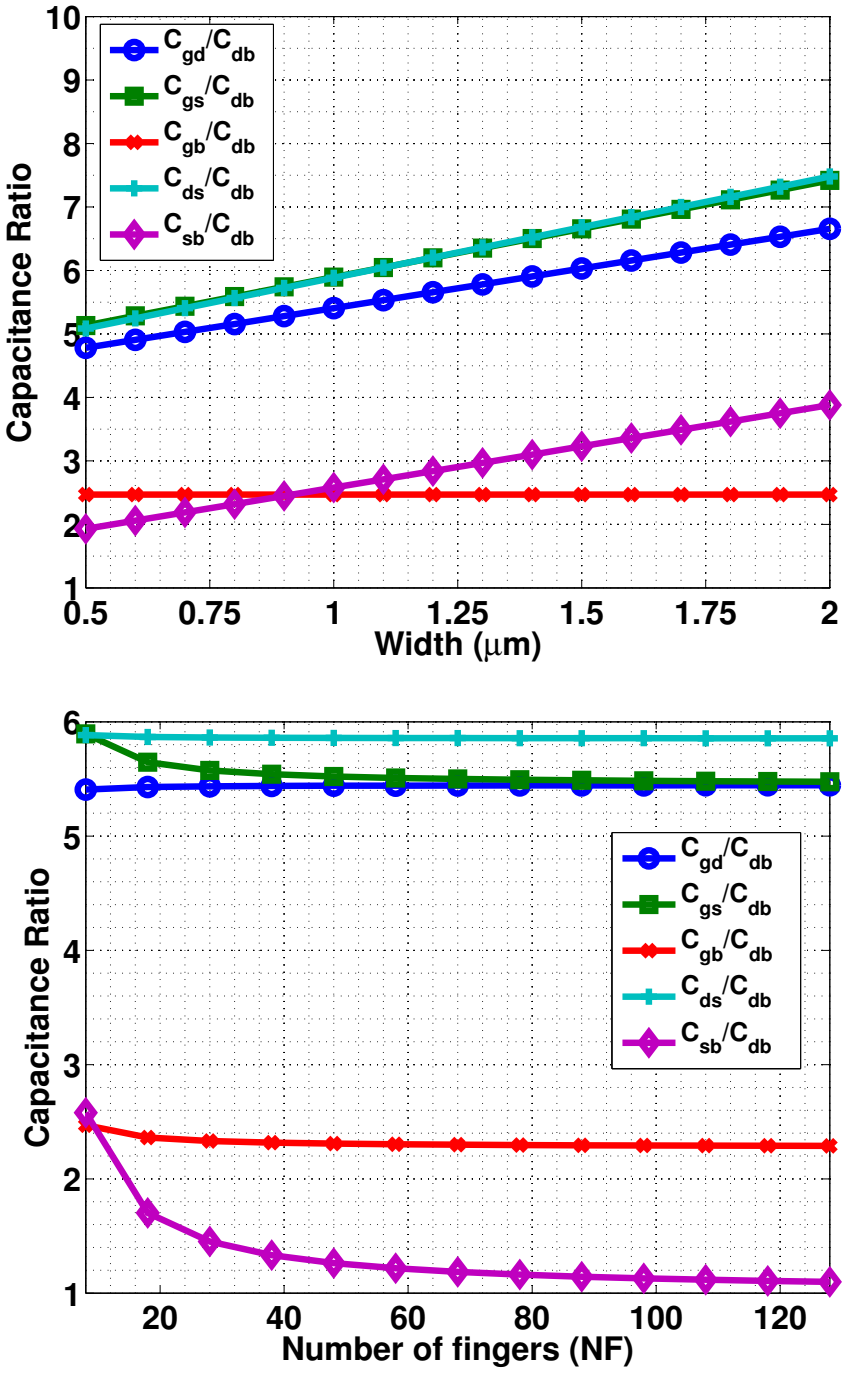


Figure 2.2. Wiring capacitance ratio as a function of width (NF=8) and number of fingers (W=1 μm)

pre-driver stage operating of a 1 V supply voltage drives the intermediate stages. The PA is stabilized for common mode oscillations using resistors at the center taps (Vb1, Vb2, Vb3) of the transformers.

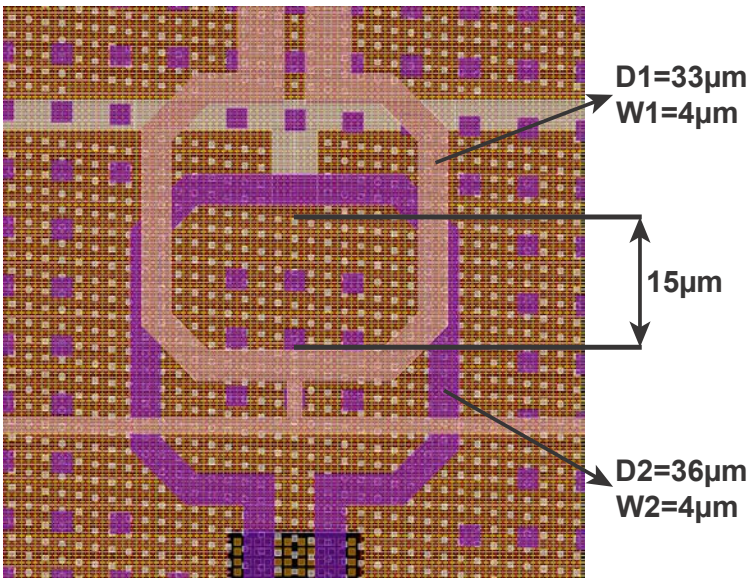


Figure 2.3. Transformer passive network with dummy metal layers

2.2.1 Power Combiner/Splitter

In order to achieve high output power levels, the design utilizes transmission lines to perform on-chip parallel power combining. In parallel power combining, a large PA unit that is load matched is split into two individual units. Due to the parallel combining nature, the impedance seen by each PA unit scales inversely proportional to its size. The achievable output power from the PA is also determined by the maximum achievable swing. The maximum achievable swing at the output is limited by gate-drain breakdown voltage of the active devices and is $\sim 1\,\mathrm{V}$ in this technology node. By employing a cascode output stage, theoretically this can be doubled to $\sim 2\,\mathrm{V}$. A differential implementation further doubles this swing. In a two-way parallel power combiner, the impedance seen by each branch is $100\,\Omega$. Thus, with the above voltage swing, the theoretically achievable output power by each branch is 80 mW. Hence, by combining two differential output stages, with a $50\,\Omega$ output impedance, the maximum achievable output power is 160 mW or 22 dBm. In practice however, the achievable power is limited by the finite V_{dsat} of the transistors and the passive losses in this technology. To obtain even higher output power, one could employ the Distributed Active Transformer (DAT) architecture [22], where the unit device sizes can be increased progressively by increasing the number of stages, thereby providing a better power enhancement ratio. To keep the layout simple and to verify the modeling strategies in these deep sub-micron technology nodes, this design uses the simplified transmission line based power combiner approach.

In this design, a two-way power combiner has been implemented using coplanar striplines (CPS) as shown in Fig. 2.6. Due to the high common mode impedance of this structure, only the odd mode of the signal is allowed to propagate. As the output load is capacitive (due to pad capacitance), the length of the line plays a critical role in the output matching network

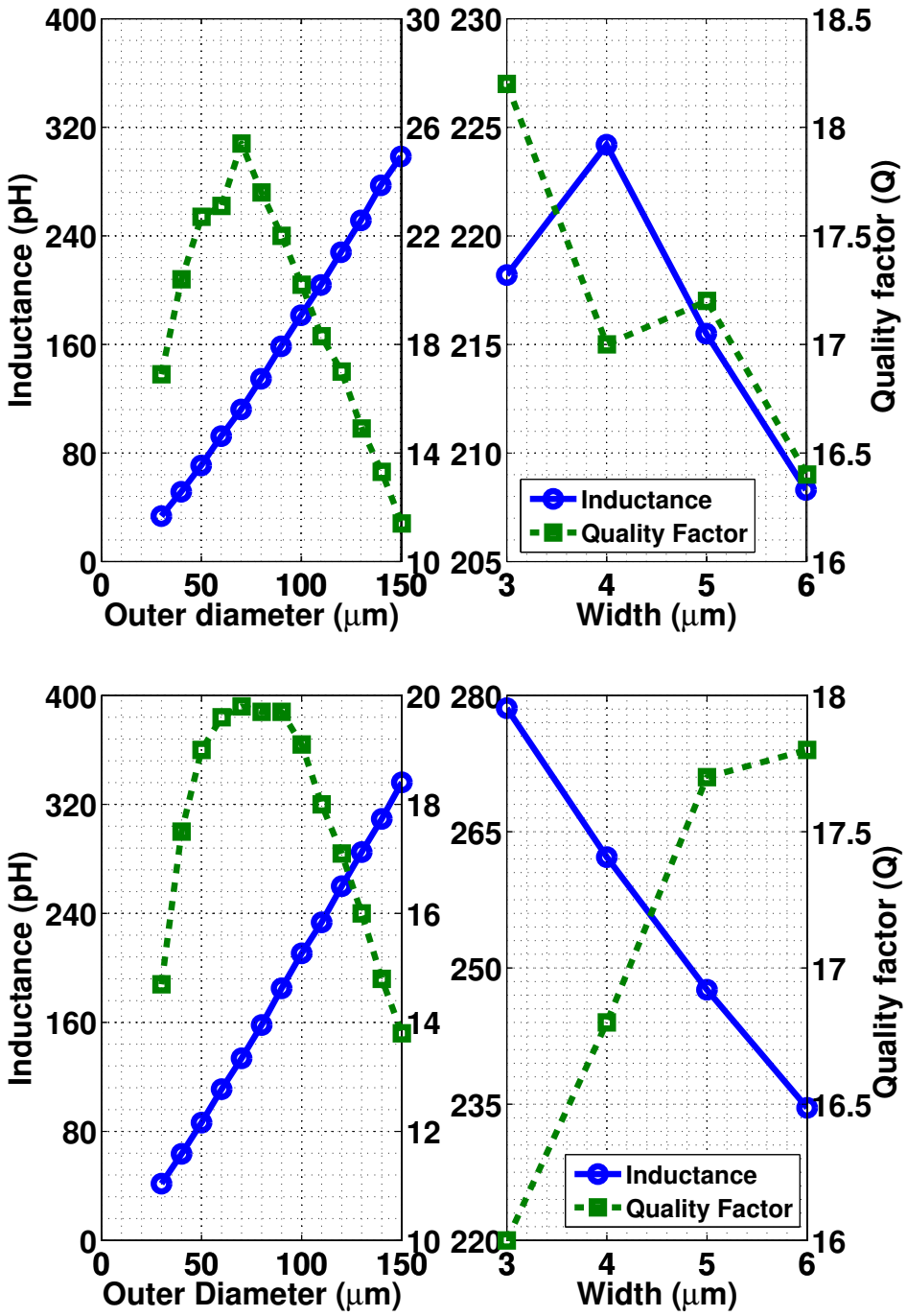


Figure 2.4. Simulated spiral inductance and quality factor as a function of outer diameter ($W = 4\,\mu$m) and width ($D_{out} = 120\,\mu$m) for ultra-thick metal [Top] and Alucap [Bottom] layers

design and must be chosen considering physical constraints in the layout and also its impact on the output transformer network design. The CPS lines transform the output impedance of $50\,\Omega$ with the pad capacitance of $60\,$fF to an impedance of $60\,\Omega||55\,$fF. The CPS lines

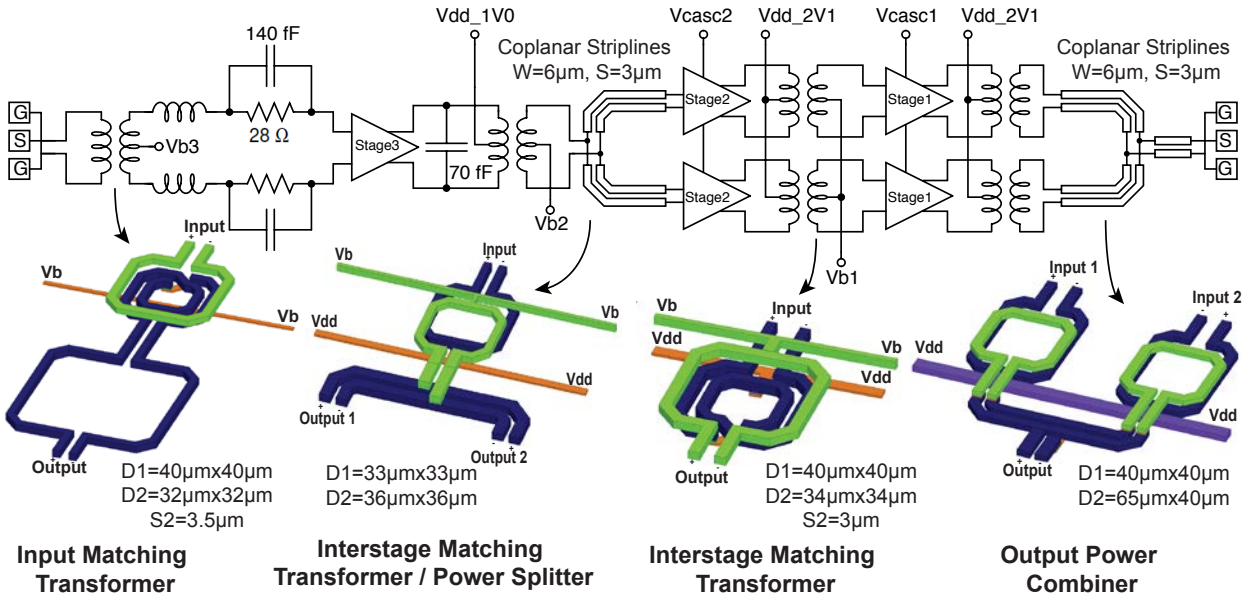


Figure 2.5. Circuit diagram of the overall power amplifier with the matching network structures

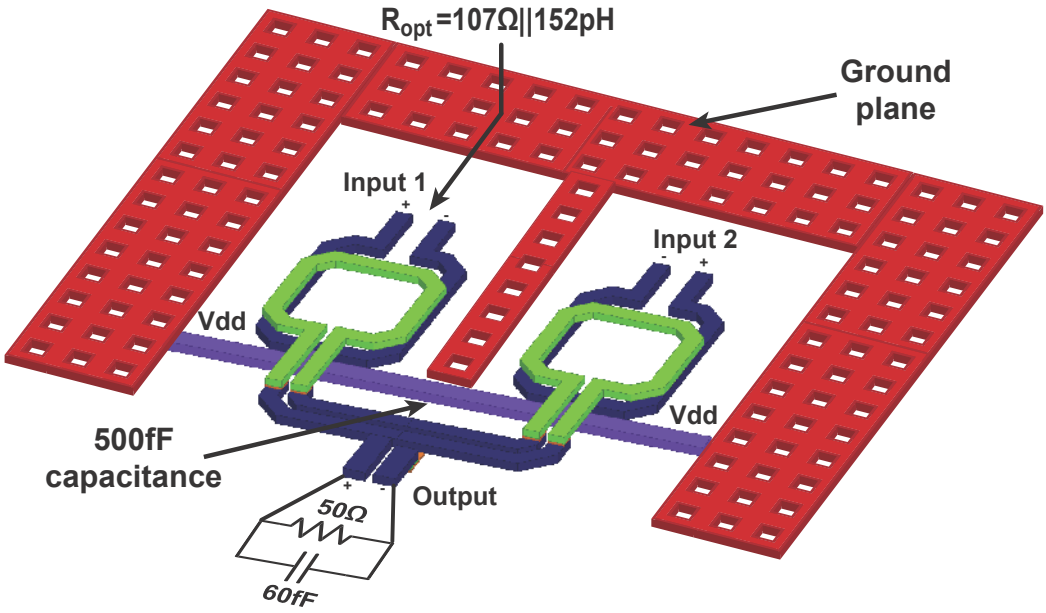


Figure 2.6. Transmission line based output power combiner

have a width of 6 μm and spacing of 3 μm with a characteristic impedance of $Z_0 = 28\,\Omega$. The simulated loss of the CPS lines is 1.1 dB/mm. The transformed CPS line impedance is then matched to each PA leg using transformer based networks. The optimal load impedance seen by each PA is 107 Ω||152 pH. In order to achieve an efficient power combining, the even order harmonic currents in the PA must be terminated properly and the center tap of

the transformer must be close to an ideal supply voltage. This is accomplished by adding a 500 fF capacitance at the center tap as shown. Due to the capacitive path, the common mode inductance seen by each PA unit is drastically reduced and this helps increase the overall efficiency of the amplifier.

A similar approach is employed in the pre-driver stage of the PA. Here, the output from the pre-driver stage is split into two branches using CPS lines. The width and the spacing is similiar to the combiner CPS lines. By employing a 10° line, the driver input impedance of the two legs is transformed to 93 Ω||102 fF. Then by using a low-k transformer matching network, the required optimal impedance for the pre-driver stage is obtained. The power splitting is performed at the pre-driver output as opposed to the interstage driver to avoid efficiency degradation due to matching network loss. The interstage driver has a higher impact on the overall efficiency as compared to the pre-driver stage.

2.2.2 Drain-Source Neutralized Cascode Stages

The output stage and interstage PA units utilize cascode devices in order to boost the achievable gain and output power of the PA. By employing a cascode device, the supply voltage can be increased to twice the nominal value and hence the output swing also increases. For this design, a peak supply voltage of 2.1 V is used. The scaling of technology to these deep sub-micron technology nodes is accompanied by stringent electromigration rules as mentioned in Section 2.1. By using a cascode device, the operating supply voltage can be doubled and hence the quiescent current in the transistors is halved for the same required output power. This avoids strapping of multiple metal layers and reduces the parasitic capacitance between the nodes. The cascode devices also provide a G_{max} of $\sim$ 14 dB per stage at 60 GHz compared to 10 dB achievable using a common source amplifier. This design uses triple well devices (with the source tied to the bulk) to achieve better isolation and hence avoid unwanted stability issues. Using a triple well device also avoids any possible gate-bulk breakdown issues.

The implementation of a cascode topology results in stability issues for common mode signals. At mm-wave frequencies, the cascode device is degenerated at the source by a capacitive impedance. Due to the finite C_{gs} of the active device, there is a component of gate current that is in anti-phase with the input voltage. This results in a negative impedance as seen from the gate. Hence, a small parasitic inductance at the gate of the cascode device is sufficient to cause common mode oscillations through the cascode gate node. This is usually mitigated by reducing the lead inductance with proper layout. Furthermore, a capacitor with small capacitance value is added very close to the transistor gate node which causes the frequency of oscillation (if any) to fall outside the f_{max} of the device, thereby preventing any oscillations. This is followed up by adding a low quality factor capacitor (with a low cut-off frequency) in order to attenuate any low frequency common-mode oscillations as shown in Fig. 2.7(a). To avoid the modeling inaccuracies in the gate inductance and to make the amplifier more robust across process corners, this design utilizes shielded lines for the cascode gate node as shown in Fig. 2.7(b). By strapping Metal 2 and Metal 3 buses of width 9 μm

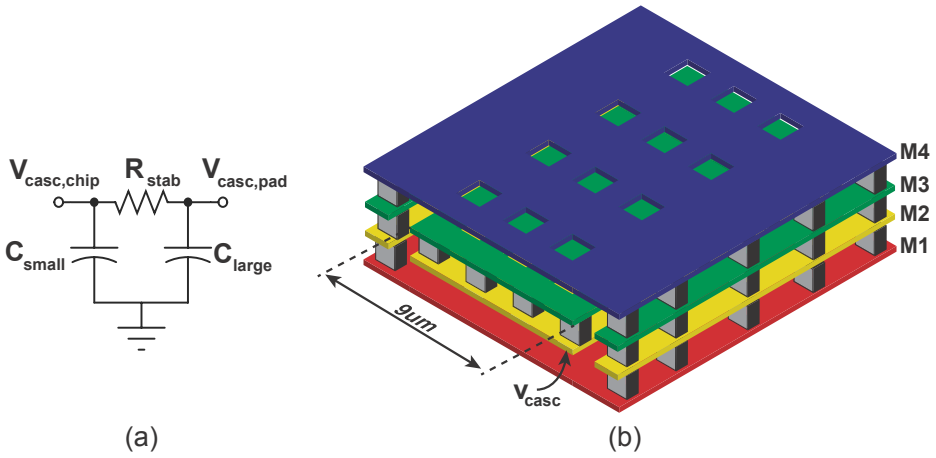


Figure 2.7. (a) Conventional cascode gate stabilization network (b) Shielded cascode gate : M2/M3 signal, M1/M4 ground shield

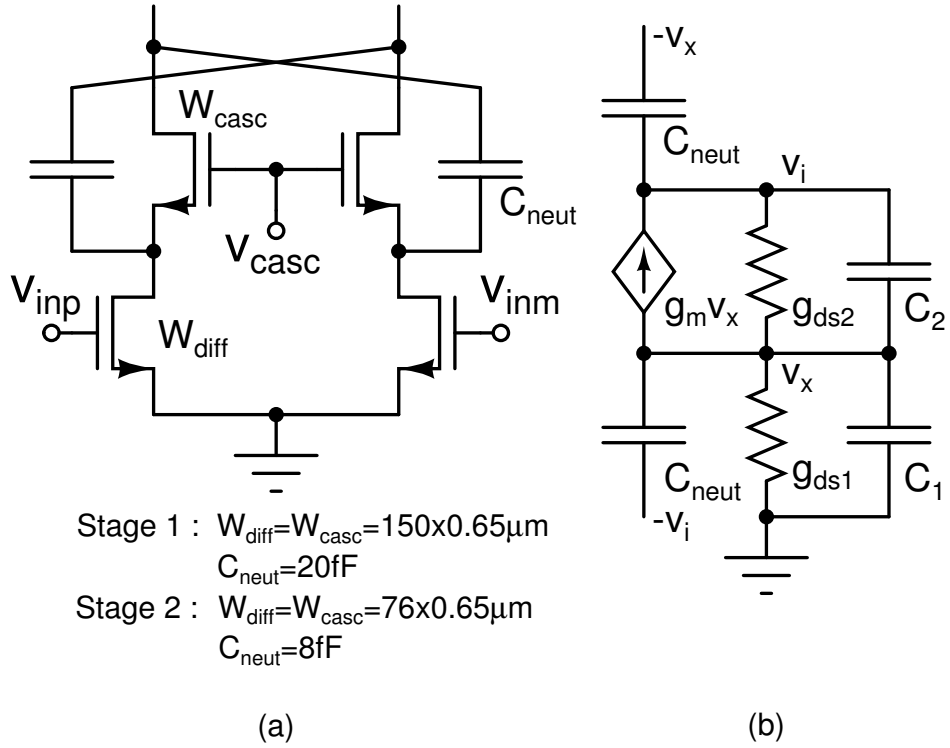


Figure 2.8. (a) Circuit diagram of the output and interstage networks (b) Small signal equivalent circuit

each and shields Metal1 and Metal4, this cage like structure is predominantly capacitive in nature. The calculated characterisitic impedance of the line is 2 Ω.

One of the important factors to be considered in the design of the output stage is the mismatch in the antenna impedance. Due to variations in the antenna impedance, the PA

does not always see the optimal load impedance. If the output reflection coefficient (S_{22}) is close to unity, the mismatch in the antenna and PA output impedance may lead to standing waves. This may cause instability or high voltage swings that may result in breakdown of the active device. The creation of standing waves also causes the output power to vary periodically with frequency. The implementation of a cascode topology in this technology leads to a stability issue from this standpoint. Due to the reduced pitch in this technology, the drain-source (C_{ds}) capacitance of the device is pretty significant. The fringe capacitance in the Metal 1 layer of the device is a major contributor to this capacitance. To understand this effect, consider the cascode device and its small signal equivalent shown in Fig. 2.8. Without the neutralization capacitance, the output admittance y_{in} of the network is calculated to be

$$y_{in} = \frac{1}{2}\left[\frac{(g_{ds1} + sC_1)(g_{ds2} + sC_2)}{(g_m + g_{ds1} + g_{ds2}) + s(C_1 + C_2)}\right] \tag{2.2}$$

where g_m is the transconductance of the cascode device, g_{ds1} and C_1 the net conductance and capacitance looking into the drain of the differential pair, g_{ds2} and C_2 the output conductance and drain-source capacitance of the cascode device respectively. Due to the high g_m/g_{ds} ratio in this technology, the real part of the output impedance in (2.2) is very high. At mm-wave frequencies, the magnitude of g_{ds1}, g_{ds2} is comparable to that of $j\omega C_1$, $j\omega C_2$ and this leads to an impedance whose real part can potentially be negative. This results in an output reflection coefficient which is close to 0 dB or even greater. As mentioned before, with mismatch in antenna impedance, this could be detrimental to the power amplifier design. In order to circumvent this issue, a drain-source neutralized cascode stage is proposed as shown in Fig. 2.8 as compared to conventional gate-drain neutralization (used to boost the gain) [23][24]. Here, cross coupled MOM capacitors C_{neut} are added between the drain and source of the complimentary devices, thereby negating the effect of C_{ds}. With finite neutralization capacitors, the output admittance is calculated to be

$$\begin{aligned} y_{in} &= sC_{neut} \\ &+ \frac{1}{2}\left[\frac{(g_{ds1} + s(C_1 + 2C_{neut}))(g_{ds2} + s(C_2 - C_{neut}))}{g_m + g_{ds1} + g_{ds2} + s(C_1 + C_2 + C_{neut})}\right] \end{aligned} \tag{2.3}$$

When $C_{neut} = C_2$ in (2.3), the real part of the output impedance can no longer be negative. The effect of neutralization on the output reflection coefficient is illustrated in Fig. 2.9. With a lossless matching network, the simulated S_{22} is close to unity. When neutralization capacitors are added and $C_{neut} = C_2$, the S_{22} improves but is only about -2 dB which is not robust considering process variations. With only a lossy transformer network, the value is close to -2.5 dB. To obtain an S_{22} better than -4 to -5 dB or a VSWR of $\sim 4:1$, C_{neut} is chosen to be greater than C_2, thereby overcompensating the capacitance. This adds a positive impedance that is shaped across the band and helps improve the output reflection coefficient.

The layout of the output stage employing drain-source cascode neutralization is shown in Fig. 2.10. A shared junction layout is not used in this case owing to the large device size (which results in long drain and gate traces). The finger width and number of fingers of the cascode and differential pair devices are chosen to be the same for ease of layout. The input

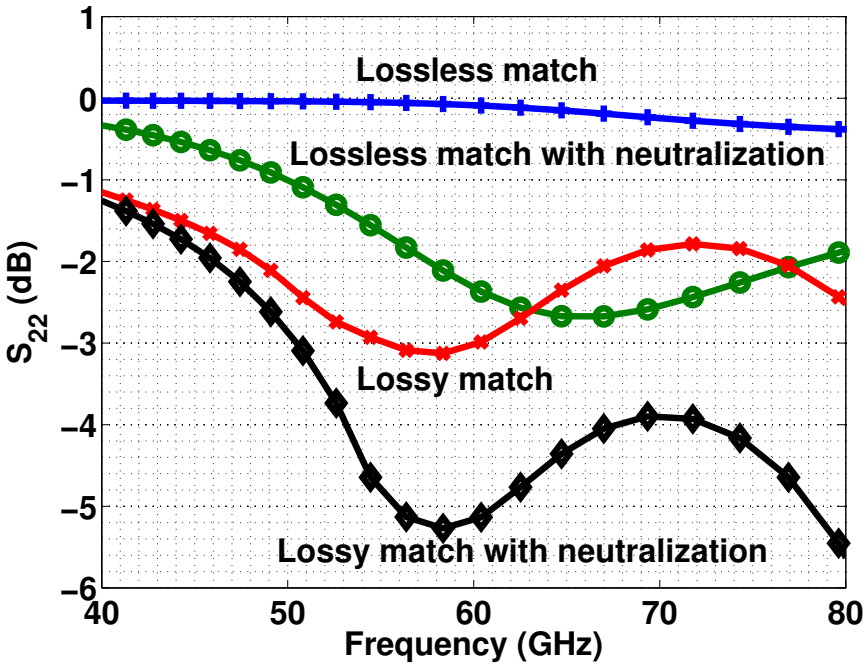


Figure 2.9. Simulated output reflection coefficient S_{22}

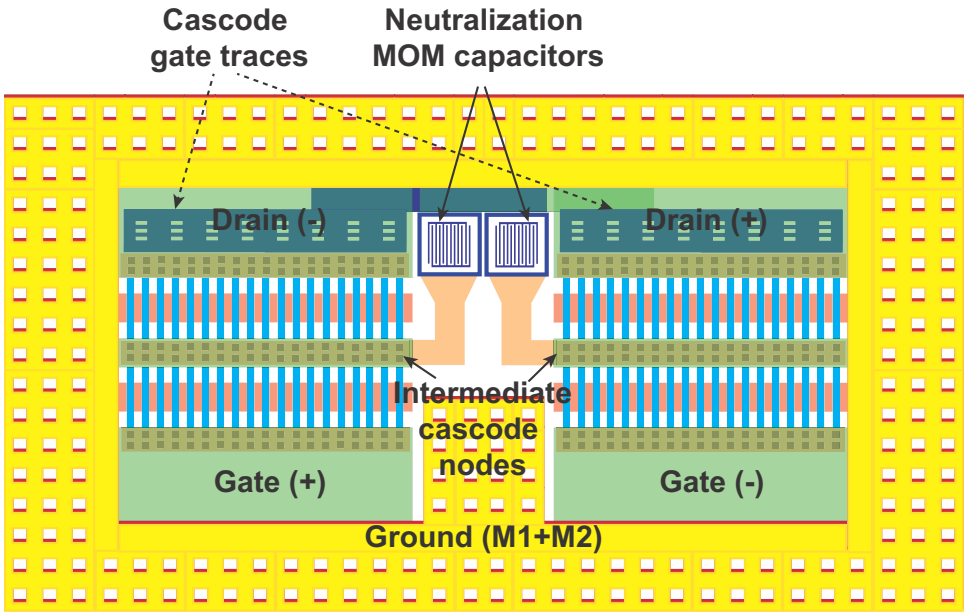


Figure 2.10. Layout of the output and interstage devices

gate traces are fed from the bottom and the output drain voltages are tapped from the top side. The shielded cascode gate traces (described above) run below the drain traces. The metal layers are chosen carefully to minimize the parasitic capacitance between the various

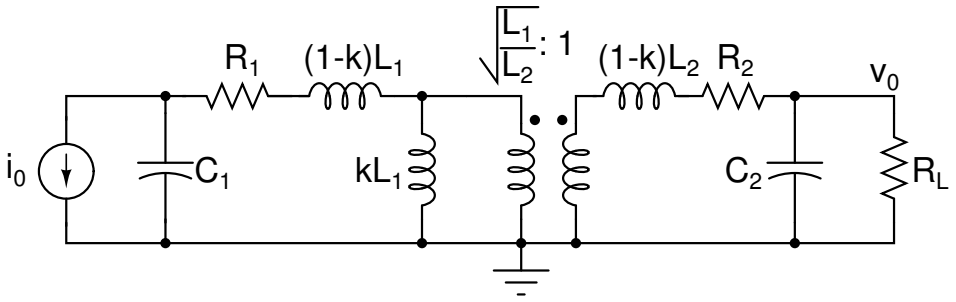


Figure 2.11. Equivalent model of the transformer matching network

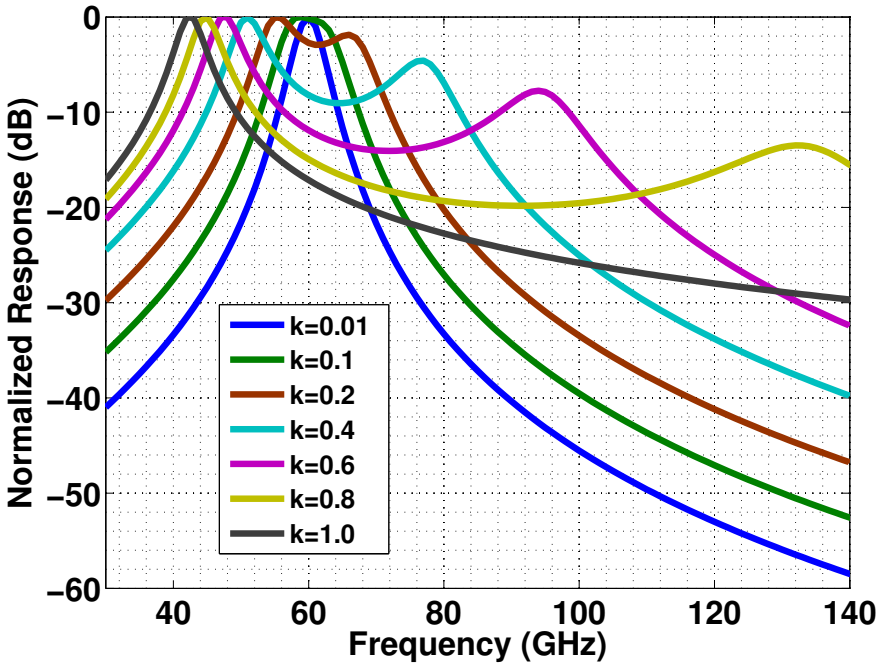


Figure 2.12. Variation of the filter response as a function of the transformer coupling coefficient 'k'

nodes. The neutralization MOM capacitors are laid out at the center and the connection lead lengths are minimized to achieve a high self-resonant frequency for these capacitors. Special care is also taken to minimize the capacitance at the intermediate cascode nodes.

A similar layout strategy is used for the intermediate driver stage.

2.2.3 Low Coupling Coefficient Transformer Networks

The achievable bandwidth of the power amplifier is dictated by the quality factor of the matching networks and the total number of stages in the PA. In order to achieve high

bandwidth to compensate for process variations, one could implement low quality factor matching networks. However, this is accompanied by additional loss in the system and results in the degradation of efficiency and output power of the PA. Hence, this design utilizes loosely coupled (low k) transformers for matching the successive PA stages [25]. Fig. 2.11 shows the equivalent model of a transformer network loaded with capacitors and the PA device is modeled as a transconductor. Here C_1 represents the drain capacitance of the PA device and any parasitic capacitance between the leads of the primary side of the transformer. Similarly, C_2 represents the gate capacitance of the successive PA stage along with any parasitic capacitance on the secondary. The finite quality factor of the transformer spiral inductances L_1 and L_2 (with coupling coefficient k) is represented by the resistors R_1 and R_2 respectively. The transfer function of this network comprises of two conjugate pole pairs. Under a high coupling coefficient case ($k \sim 0.7 - 0.8$), the second conjugate pole pair occurs at a frequency much higher than the resonant frequency of the system. This results in a response similiar to that of a second order system and is the usual mode of operation in conventional transformer based matching networks. When the coupling coefficient is reduced ($k \sim 0.2 - 0.3$), the second pole pair comes in-band and an appropriate design choice could allow the synthesis of various filter networks. The variation of the filter response for different coupling coefficient values is shown in Fig. 2.12. In this simulation, a quality factor of 10 was assumed for the primary and secondary coils. We observe that as the coupling coefficient is reduced from unity, the second pole pair comes in-band and for $k \sim 0.1$, we obtain the maximally flat response.

The transfer impedance of the network under a low coupling coefficient case is given by

$$\frac{v_o}{i_o} = \frac{-sk\sqrt{L_1 L_2}/\alpha}{[1 + sR_1C_1 + s^2L_1C_1][1 + s(\frac{L_2}{\alpha R_L} + \frac{R_2C_2}{\alpha}) + \frac{s^2L_2C_2}{\alpha}]} \tag{2.4}$$

where $\alpha = 1 + \frac{R_2}{R_L}$. As discussed above the equation consists of two conjugate pole pairs. In order to acheive a maximally flat Butterworth response, we can show that the quality factor of the primary and the secondary must be the same and equal to the reciprocal of the coupling coefficient [26] i.e. $Q_1 \approx Q_2 \approx 1/k$ and the resonance of the system must occur at the center frequency i.e. ${\omega_0}^2 L_1 C_1 \approx {\omega_0}^2 L_2 C_2 = 1$. If the quality factor of the primary and the secondary do not match (which is usually the case as the gate and drain capacitances are not equal), additional capacitance must be added to make the quality factors equal. The insertion loss (IL) of the transformer can be derived similar to [22] and is given as

$$IL = \frac{1}{1 + \frac{R_2(1+\omega^2 {R_L}^2 {C_2}^2)}{R_L} + \frac{(1+\frac{R_2}{R_L} - \omega^2 L_2 C_2)^2 + \omega^2(\frac{L_2}{R_L} + R_2 C_2)^2}{\omega^2 k^2 L_1 L_2/(R_1 R_L)}} \tag{2.5}$$

where ω is the operating frequency in rad/s. The insertion loss is a function of the transformer parameters and the load resistance R_L. However, from (2.5), it is clear that the loss depends on the square of the coupling coefficient. In this design, the low-k transformer network has an insertion loss of 1.98 dB.

The low-k transformer network is implemented using spiral inductors that are coupled vertically. The required coupling coefficient is obtained by changing the offset between the

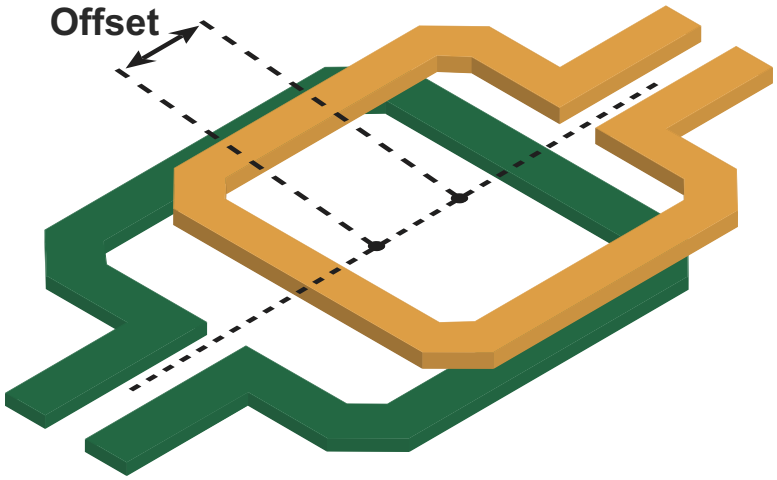


Figure 2.13. Transformer implemented using square spirals : Coupling coefficient is varied by changing the offset

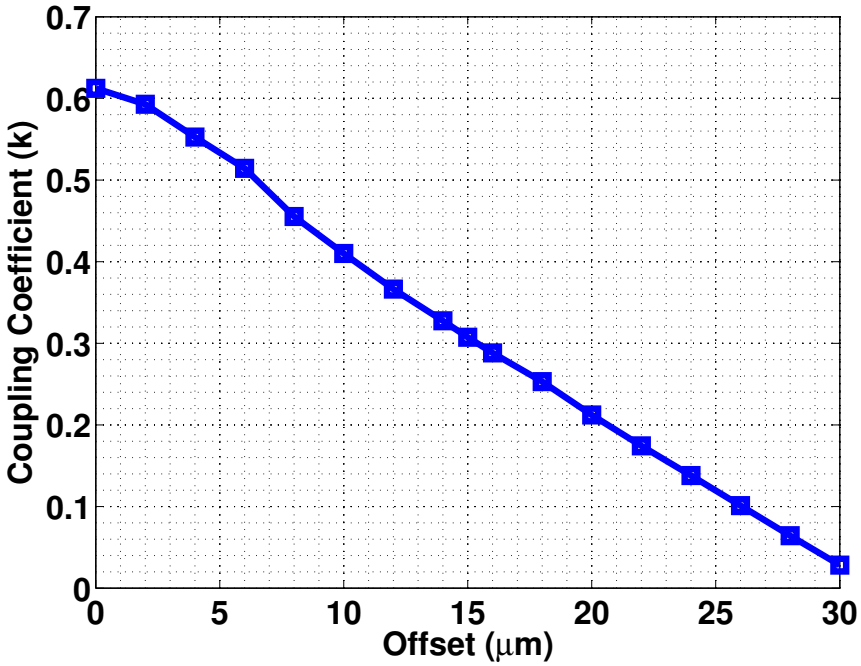


Figure 2.14. Simulated coupling coefficient of a transformer implemented using square spirals

two inductors as shown in Fig. 2.13. In order to make the design robust across process variations, the variation of the coupling coefficient of the transformer must be kept to a minimum to avoid changes in the filter response. Hence, a square shaped spiral is specifically selected as the variation in the coupling coefficient is linear as shown in Fig. 2.14. Also, a square shaped spiral is much easier to layout. In this design, the output and interstage transformer/power splitter matching networks have been implemented using low-k transformers.

The use of these low-k matching networks along with the f_T benefit of the technology helps the PA achieve a bandwidth of 11 GHz.

2.2.4 Pre-driver stage

A single pre-driver stage drives both the interstage drivers. The driver power requirement for the interstage networks is much lower compared to that of the output stage and is also greatly relaxed due to its high gain. Hence, a single differential pair operating out of a 1 V supply is enough to drive both the interstage drivers. A low-k transformer network is used to match the pre-driver stage to the interstage drivers. To make the pre-driver stable at lower frequencies (where the gain is high), a parallel RC network ($28\,\Omega||140\,\text{fF}$) is added to its input [27]. This network adds a pole at 32 GHz and thus any oscillations below this frequency are attenuated. At 60 GHz, the reactance of the 140 fF capacitance is lower than the $28\,\Omega$ resistance and this allows the input signal to propagate to the input of the pre-driver without appreciable attenuation.

2.2.5 Sizing of the amplifier stages

In order to obtain the best tradeoff for f_{max} with respect to the gate resistance and the increased layout parasitics, the design uses a finger width of $0.65\,\mu$m for all the stages. The number of fingers in each stage is then varied to obtain the required output power. The output stage uses 150 fingers for each transistor and this is chosen by co-optimizing the overall efficiency of the PA unit and the output power combiner. The output stage operates in the class AB regime and is biased at a current density of $0.05\,\text{mA}/\mu$m. The number of fingers in the interstage and pre-driver stages are 76 and 36 respectively. The sizing is chosen such that under the worst case corner, the interstage and pre-driver stages have enough power to drive the output stage. The interstage driver is biased with a current density of $0.1\,\text{mA}/\mu$m while the pre-driver stage is biased in the Class A regime at $0.18\,\text{mA}/\mu$m. The device is biased slightly below the peak f_{max} point to increase the overall efficiency of the amplifier.

2.3 Measurement Results

The power amplifier is fabricated in 28 nm bulk CMOS process. Fig. 2.15 shows the die photo of the chip. The chip occupies a total area of $0.64\,\text{mm}^2$ and is pad limited. The core area of the PA is $0.122\,\text{mm}^2$. The chip is characterized using wafer probing.

The measured S-parameters of the PA is shown in Fig. 2.16 and the measured maximum frequency is limited by the equipment capability. The PA achieves a peak gain of 24.4 dB with a 3 dB bandwidth of 11 GHz extending from 56 GHz to 67 GHz. This is mainly due to the increased f_T of the process and the application of low-k transformer techniques for

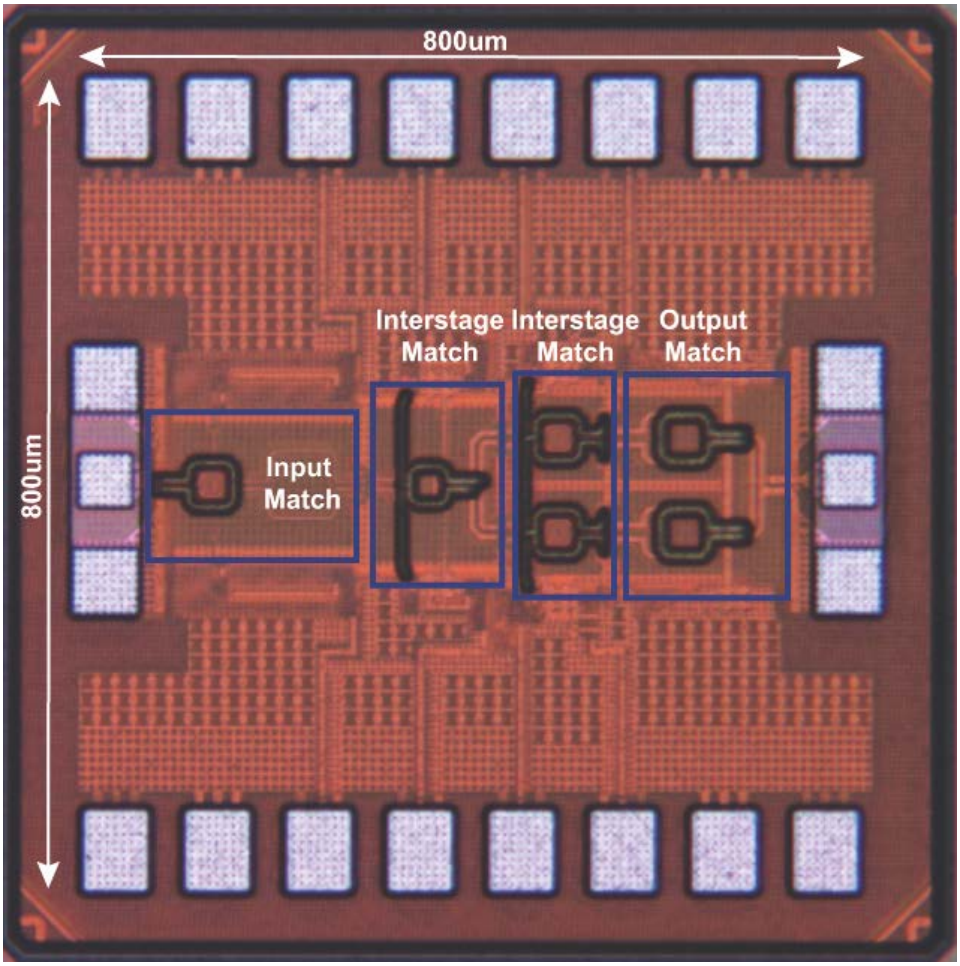


Figure 2.15. Chip microphotograph

the matching networks. The measured S_{11} of the PA remains relatively flat within the band of interest with a value less than or equal to $-10\,\text{dB}$. The measured S_{11} at 56 GHz and 67 GHz are $-8.7\,\text{dB}$ and $-12.5\,\text{dB}$ respectively. The reverse isolation is better than $-40\,\text{dB}$ for the indicated range of frequencies. Due to the neutralization technique discussed above, the output reflection coefficient of the PA is maintained to be less than $-5\,\text{dB}$ for the inband frequencies and has a similar behavior as shown in simulation results. Fig. 2.17 shows the measured stability factor of the PA from DC to 70 GHz and is greater than unity for all the frequencies. This provides the necessary condition for the overall stability of the amplifier.

Fig. 2.18 shows the measured gain, output power, drain efficiency and power-added efficiency (PAE) of the PA at 62 GHz. The PA achieves a saturated output power of 16.5 dBm with a peak PAE of 12.6 %. The measured P_{-1dB} at 62 GHz is 11.7 dBm with a PAE of 6.3 %. Fig. 2.19 shows the measured gain, saturated output power, P_{-1dB} and PAE as a function of frequency. The average saturated output power of the PA is around 15.5 dBm within the band of interest. The average PAE is around 10.5 %. The variation of the PA performance with the output and interstage supply voltage is shown in Fig. 2.20. The output power and

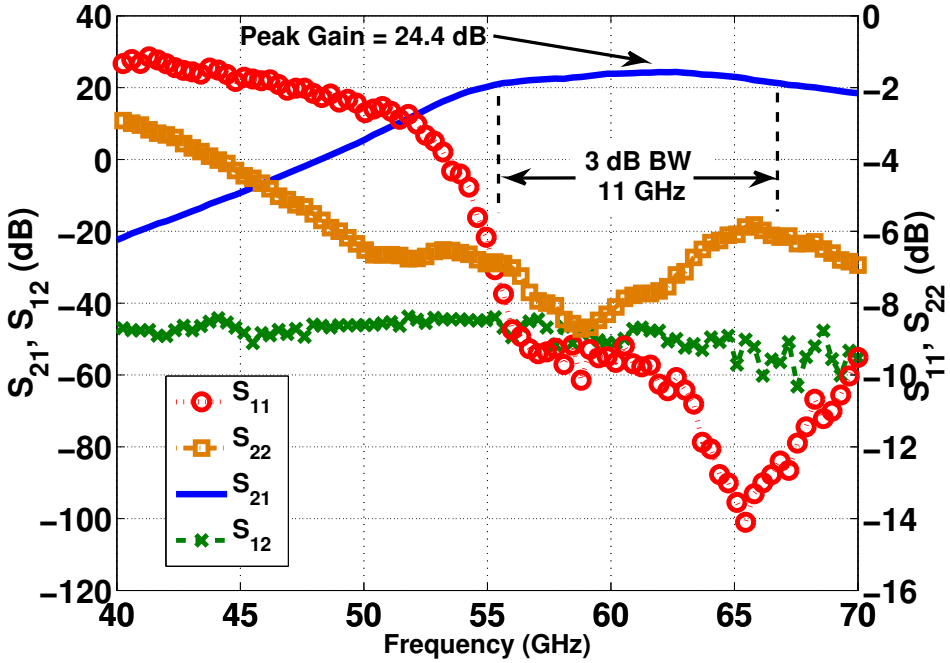


Figure 2.16. Measured S-parameters

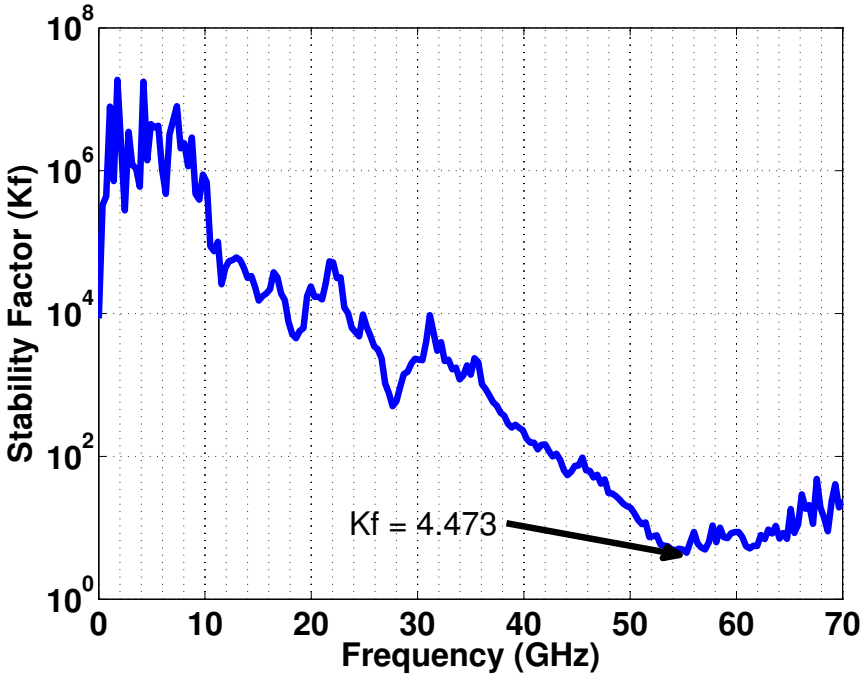


Figure 2.17. Measured stability factor as a function of frequency

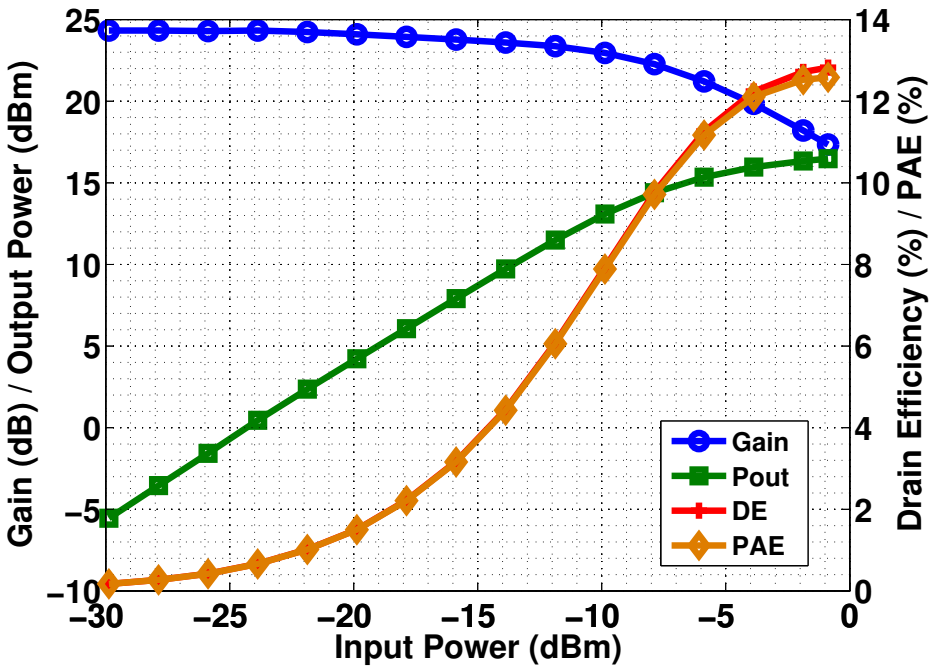


Figure 2.18. Measured gain, output power, drain efficiency and power-added efficiency as a function of the input power at 62 GHz

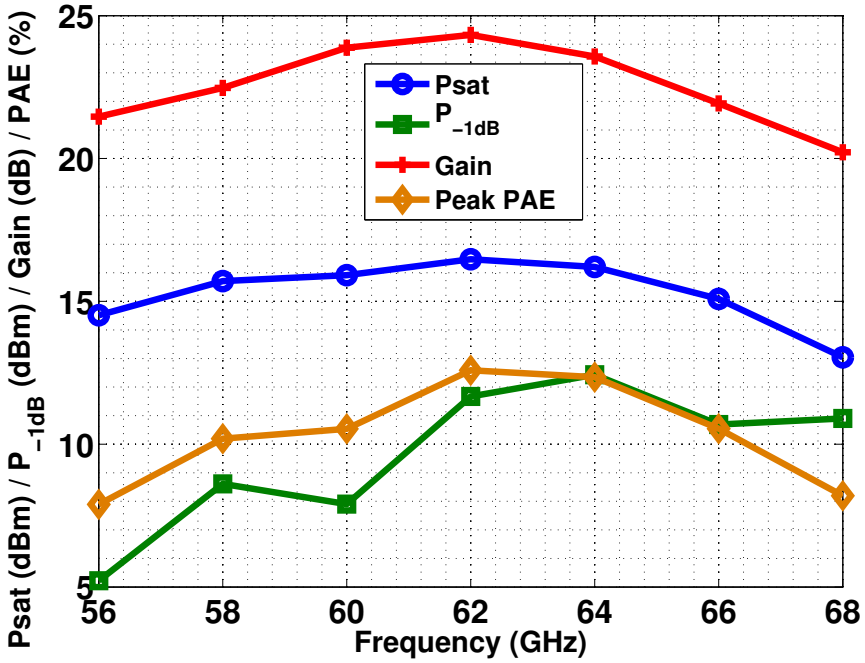


Figure 2.19. Measured small signal gain, Psat, P_{-1dB} and power-added efficiency as a function of frequency

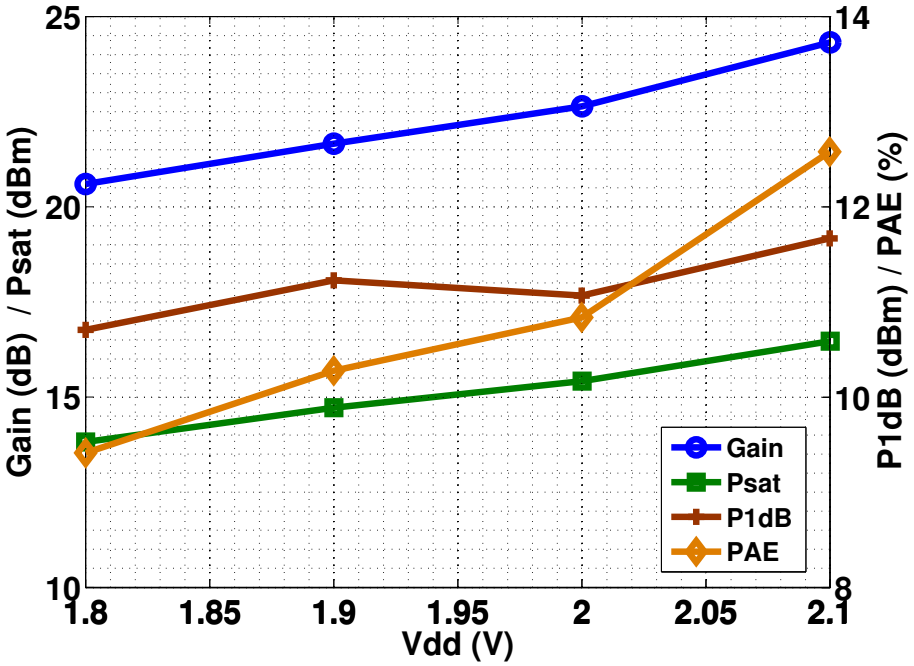


Figure 2.20. Measured small signal gain, Psat, P_{-1dB} and power-added efficiency as a function of supply voltage at 62 GHz

the PAE increase as the supply voltage is changed from 1.8 V to 2.1 V. The peak output power and PAE occur at the maximum supply voltage of 2.1 V and this voltage has been used for all the measurements. The maximum operatable voltage is restricted to 2.1 V to avoid gate-drain breakdown issues.

The AM-to-PM distortion of the PA at the center frequency is shown in Fig. 2.21. The peak phase difference is restricted to less than 10° as the PA operates close to the linear regime. The peak phase difference across the frequency band is shown in Fig. 2.22. The AM-to-PM distortion peaks near the band-edge at 57 GHz and is less than 10° across the band.

The effect of RF stress on the PA was also measured for a period of 5 hours. Fig. 2.23 shows the output power and PAE degradation as a function of time. The output power degrades by 0.2 dB initially while the PAE drops from 12.3 % to 11.6 %. As time progress, the output power and PAE values become fairly constant. For an Orthogonal frequency-division multiplexing (OFDM) signal, the PA operates predominantly at a $6-7$ dB back-off. Hence, the above measurement at peak power indicates a fairly long lifetime for the PA.

Table I shows a comparison table of the state-of-art linear 60 GHz CMOS PAs published in literature. Compared to other work, this design achieves the best gain-bandwidth product while maintaining reasonable output power and efficiency numbers. This is mainly due to the improved f_T of the technology and the application of low-k transformers for matching.

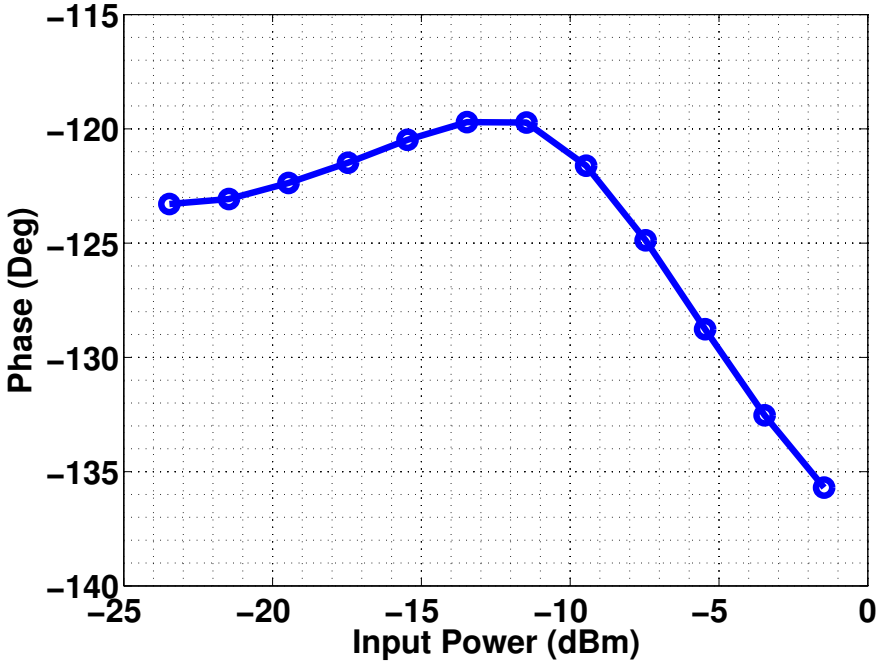


Figure 2.21. Measured AM-to-PM distortion at 62 GHz

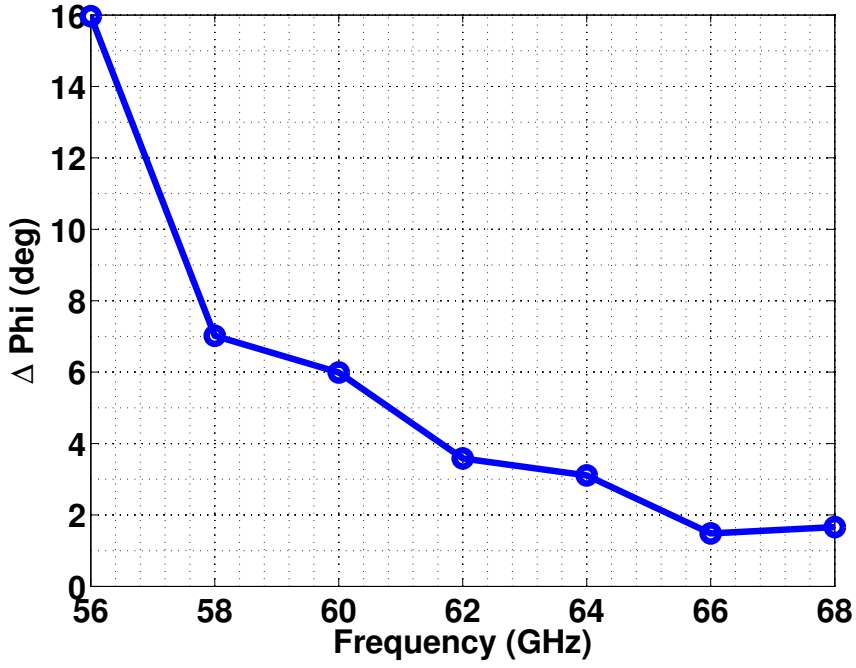


Figure 2.22. Measured peak phase overshoot (AM-to-PM) as function of frequency

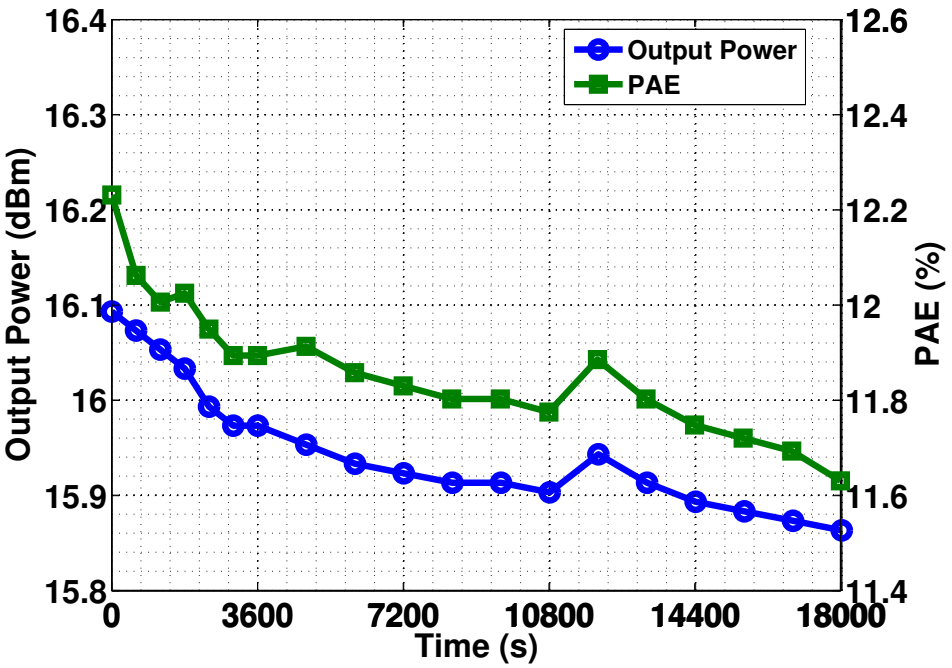


Figure 2.23. Measured output power and power-added efficiency due to RF stress

Table 2.1. Comparison Table of 60 GHz CMOS Power Amplifiers

	Process	Gain (dB) / BW (GHz)	Psat (dBm)	P_{-1dB} (dBm)	PAE (%)
This Work	**28** nm	**24.4 / 11**	**16.5**	**11.7**	**12.6**
[17]	65 nm	14.3 / 15	16.6	11	4.9
[18]	65 nm	19.2 / -	17.7	15.1	11.1
[24]	65 nm	16 / 7	11.5	5	15.2
[28]	65 nm	20.3 / 9	18.6	15	15.1
[29]	90 nm	20.6 / 8	19.9	18.2	14.2

2.4 Conclusion

The design of a V-band PA is demonstrated in 28 nm bulk CMOS technology. The PA achieves a peak gain of 24.4 dB with a bandwidth of 11 GHz. The wideband nature of the PA is due to the improved f_T of this technology and the use of low-k transformer networks. A drain-source neutralization technique is also introduced in order to maintain the stability

of the PA. By utilizing transmission line based power combiners, the PA achieves a saturated output power of 16.5 dBm with a peak PAE of 12.6%.

Chapter 3

Terahertz Transceiver : System level considerations

The design of a millimeter-wave/terahertz system is governed by various challenges. In this chapter, we address some of the issues that govern the choice of the architecture and the challenges faced in the transmitter and receiver design. The high frequency operation also requires accurate modeling of the passive and active elements to avoid performance degradation of the system. Since the design involves blocks operating at various frequencies, issues with regard to coupling need to be addressed. We discuss different modulation schemes namely non-coherent on-off keying (OOK), binary phase shift keying (BPSK) and quadrature phase shift keying (QPSK) and show the feasibility of communication at these frequencies.

3.1 Choice of the carrier frequency

Operation at a high carrier frequency allows one to achieve a much higher absolute bandwidth which results in high data rate communication at the expense of a reduced range. In the designs described in this thesis, the actual bandwidth is restricted to the fractional bandwidth at the intermediate frequency. This is because the modulation is performed at a lower intermediate frequency and then up-converted to the sub-terahertz frequency. One of the biggest advantages of operating at these high frequencies is the integration of the antennas on to the silicon die. This allows the designer to co-optimize the circuit blocks along with the design of the antenna thereby increasing the overall performance of the system.

The dimensions of the antenna are inversely proportional to the frequency of operation. As described earlier, the application requires multiple chips communicating with each other and this would make the die cost a significant factor. In this application, we assume a nominal

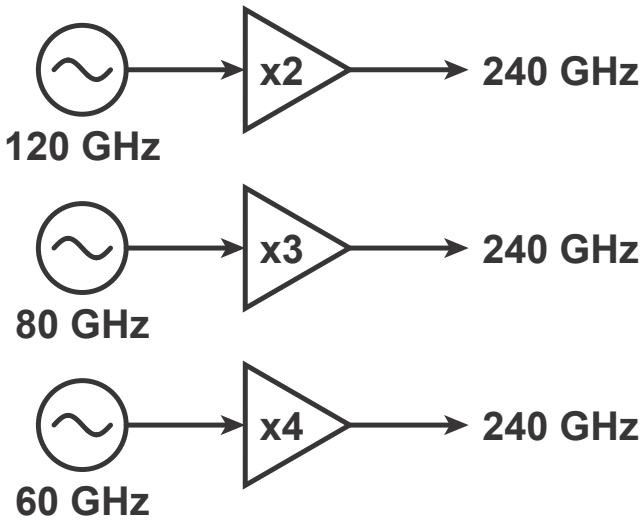


Figure 3.1. Harmonic generation techniques to generate a carrier of 240 GHz

die area of 1 mm × 1 mm for the antenna. Operating at 240 GHz corresponds to an on-chip wavelength of 360 μm. With a two array antenna and additional ground plane routing, this frequency of operation is reasonable for the edge dimension of 1 mm. Additionally, for long range communication using lenses, the atmospheric attenuation in this band is low.

3.2 Challenges in the transmitter and receiver design

The design at sub-terahertz frequencies allows high data rate communication and integration of antennas on the die. However, the range of communication is severely limited by the high path loss as will be discussed later. Additionally, the technology constraints provide further challenges to the transmitter and receiver design.

One of the primary factors determining the feasibility of this application is the cost of the die. As CMOS technology is low cost and widely accessible, it becomes the technology of choice for this application. Apart from the cost advantage, the design can also leverage the digital interface which has benefited from scaling. However, CMOS technology has a low cut-off frequency with a transition frequency of 250 GHz and a maximum oscillation frequency f_{max} of 200 GHz in 65 nm bulk CMOS. Furthermore, the continued scaling has not benefited the f_{max} of the device due to the increase in gate resistance of the device. Hence, operation at IF frequencies around one-half the f_{max} reduces the available gain from the transistor and thus requires multiple stages of amplification which results in higher power consumption. The relatively low cut-off frequency also necessitates one to explore various harmonic generation schemes to generate the required carrier frequency. For example, as shown in Fig. 3.1, the required carrier frequency of 240 GHz can be generated from different IF frequencies namely 60 GHz, 80 GHz and 120 GHz followed by the appropriate frequency

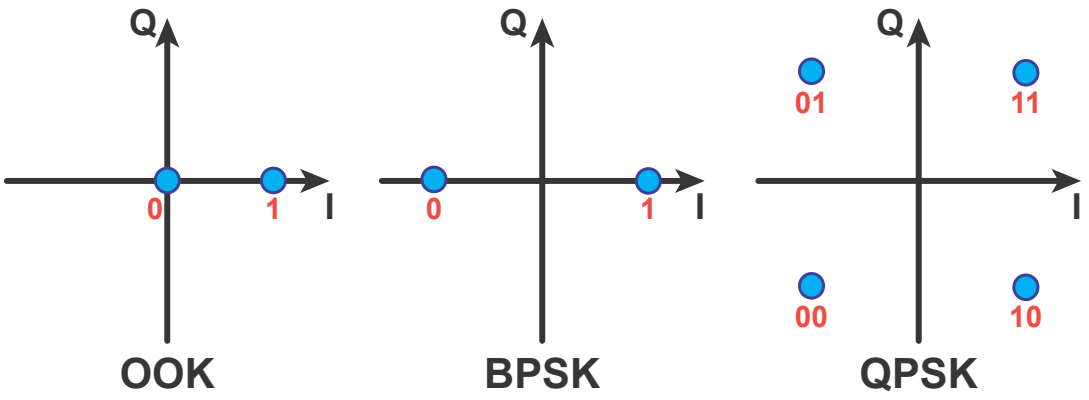


Figure 3.2. Constellation diagrams for OOK, BPSK and QPSK modulation schemes

multiplication. The scaling of CMOS technology in the last decade has also resulted in lower supply voltages and low breakdown voltages for the transistors. This severely limits the power generation capability at mm-wave frequencies. Hence, stacked transistor designs and power combining techniques need to be employed to increase the output power. The equivalent isotropically radiated power can also be increased by increasing the number of antennas on the chip (as has been done in this design).

On the receiver side, the low cut-off frequency of the technology does not allow one to use a low noise amplifier up-front and the down-conversion must be implemented using passive devices. This results in a conversion loss and degrades the signal to noise ratio. Furthermore, due to the conversion loss, the stages following the down-conversion must have low noise figure as they directly affect the noise figure of the entire chain. The amplification stages must also have high gain and wide bandwidth to support high data rate communication. A Schottky barrier diode is feasible for demodulation due to its high cut-off frequency but is seldom used due to it low responsivity. In the designs described in the next chapters, a mixer first architecture has been used for down-conversion.

3.3 Modulation Schemes

As the frequency of operation is in the mm-wave/sub-terahertz region, there is large amount of available bandwidth for high data rate communication. Hence, the designs implemented in this thesis employ relatively simple modulation schemes. The constellation diagrams of the implemented modulation schemes namely on-off keying (OOK), binary phase shift keying (BPSK) and quadrature phase shift keying (QPSK) are shown in Fig. 3.2. In order to calculate the required signal-to-noise ratio and the maximum communication range, we now discuss the modulation schemes briefly.

3.3.1 On-off Keying (OOK)

In OOK modulation scheme, the signal is transmitted only in one basis. As the information is encoded in the energy level of the signal (Amplitude Shift Keying (ASK)), the demodulation can be performed using an envelope detector. Therefore, the transmitted signal is given as

$$s_I(t) = \begin{cases} A_c \cos(\omega_c t) & \text{, if 1 is transmitted} \\ 0 & \text{, if 0 is transmitted} \end{cases}$$

where A_c is the amplitude of the transmitted carrier and ω_c is the carrier frequency.

Using an additive white Gaussian noise (AWGN) model, the received signal for a non-coherent scheme can be shown to have a Rician probability density function [30]. Under this condition, the probability of error P_{error} is calculated to be [30]

$$P_{error} = \frac{1}{2} \exp\left(\frac{-\gamma_b}{2}\right) \tag{3.1}$$

where γ_b is the signal to noise ratio per bit and is given by $\gamma_b = E_b/N_0$. Here, E_b is the average energy per bit and $N_0/2$ the noise variance. It can also be shown that compared to a coherent OOK scheme, the probability of error in a non-coherent scheme is four times larger. The relation between the probability of error for a non-coherent and coherent OOK scheme is given as

$$\left(\frac{P_{error,non-coherent}}{P_{error,coherent}}\right)_{\gamma_b \gg 1} = \sqrt{\frac{\pi\gamma_b}{2}} \tag{3.2}$$

Even though the non-coherent scheme has a high bit error rate, it is preferred in the first design to avoid synchronization between the local oscillator clocks in the transmitter and the receiver.

3.3.2 Phase Shift Keying - Binary (BPSK) and Quadrature (QPSK)

In a phase shift keying modulation scheme, the information is encoded in the phase of the carrier. In BPSK mode, the signal is transmitted only in one basis say I. Therefore,

$$s_I(t) = \begin{cases} A_c \cos(\omega_c t) & \text{, if 1 is transmitted} \\ -A_c \cos(\omega_c t) & \text{, if 0 is transmitted} \end{cases}$$

As this is a coherent scheme, the demodulation circuitry requires knowledge of the exact frequency and phase of the transmitted signal. The demodulation process involved a matched

filter operation i.e. multiplication with the basis function following by integration over a time period. Using an additive white Gaussian noise (AWGN) model with a noise variance of $N_0/2$, the received signal $r = s + n$, where s is the transmitted signal with energy per bit E_b and n the noise. The probability of error P_{error} is given as

$$P_{error} = P(s = 1)P(r < 0|s = 1) + P(s = 0)P(r > 0|s = 0)$$

The probability of transmission $P(s = 0) = P(s = 1) = 1/2$ and the conditional probability is given as

$$P(r < 0|s = 1) = \int_{-\infty}^{0} \frac{1}{\sqrt{\pi N_0}} \exp\left[-\left(\frac{r - \sqrt{E_b}}{N_0}\right)^2\right]$$

Thus, probability of error P_{error} is calculated to be

$$P_{error} = Q\left(\sqrt{\frac{2E_b}{N_0}}\right) = \frac{1}{2}\text{erfc}\left(\sqrt{\frac{E_b}{N_0}}\right) \tag{3.3}$$

For a QPSK modulation scheme, the information is transmitted in the in-phase and the quadrature axis. The transmitted signal s_I and s_Q are given as

$$\{s_I(t), s_Q(t)\} = \begin{cases} \{A_c\cos(\omega_c t), A_c\sin(\omega_c t)\} & \text{, if 11 is transmitted} \\ \{A_c\cos(\omega_c t), -A_c\sin(\omega_c t)\} & \text{, if 10 is transmitted} \\ \{-A_c\cos(\omega_c t), A_c\sin(\omega_c t)\} & \text{, if 01 is transmitted} \\ \{-A_c\cos(\omega_c t), -A_c\sin(\omega_c t)\} & \text{, if 00 is transmitted} \end{cases}$$

Since the transmission in the two axis are independent, the probability of symbol error can be calculated using the BPSK formulation. The probability of error P_{error} is

$$P_{error} = 1 - (1 - P(\text{error in I}))(1 - P(\text{error in Q}))$$

Thus, the probability of symbol error is given as

$$P_{error} = 2Q\left(\sqrt{\frac{2E_b}{N_0}}\right)\left[1 - \frac{1}{2}Q\left(\sqrt{\frac{2E_b}{N_0}}\right)\right] \tag{3.4}$$

Under a high SNR case,

$$P_{error} \approx 2Q\left(\sqrt{\frac{2E_b}{N_0}}\right) \tag{3.5}$$

From (3.5), since QPSK transmits twice the number of bits in a period, the bit error rate is the same as that of BPSK. However, the required bandwidth is half of BPSK for the same data rate.

3.4 Link budget

The range of communication at sub-terahertz frequencies is severely limited by the high path loss at these frequencies. Given a line of sight communication, the received power at the antenna can be calculated using the Friis equation as

$$P_{RX} = \frac{G_{TX}}{4\pi R^2} A_{RX} P_{TX} \tag{3.6}$$

where P_{RX} is the received power, G_{TX} the transmit antenna gain, R the distance of communication and A_{RX} the aperture of the receiver antenna which is related to the antenna gain as $A_{RX} = \lambda^2/(4\pi)G_{RX}$. Here, λ is the wavelength of the carrier and G_{RX} the receiver antenna gain. Thus, (3.6) becomes

$$P_{RX} = \frac{\lambda^2 G_{TX} G_{RX}}{(4\pi R)^2} P_{TX} \tag{3.7}$$

When an array of antennas is used in the transmitter, the electrical field adds up in phase in the space and hence the power varies as the square of the number of elements [31][32][33]. Therefore, $G_{TX} = N^2 G_{TX,unit}$, $G_{TX,unit}$ is the gain of a single antenna. The same is however not true on the receiver side as the noise power received by each antenna is uncorrelated. Thus, $G_{RX} = N G_{RX,unit}$ where $G_{RX,unit}$ is the gain of the a single antenna. Using (3.7), the signal-to-noise ratio (SNR) at the receiver output can be calculated to be

$$\text{SNR} = \frac{\lambda^2 G_{TX} G_{RX} P_{TX}}{(4\pi R)^2 k_B T B F} \tag{3.8}$$

where k_B is the Boltzmann constant, T the temperature, B the signal bandwidth and F the noise factor of the receiver chain. Using (3.8) and the calculated bit error rate equations from the previous section, the link budget for OOK, BPSK and QPSK modulation schemes is calculated and shown in Table 3.1. The link budget parameters are selected based on the designs described in the next two chapters. A carrier frequency of 240 GHz was selected for all the designs. The transmit power from each unit element is 0 dBm. The antenna gains listed in the table have the array factor included in the calculation. In both the designs, a two element antenna array has been used and this allows one to achieve higher equivalent isotropic radiated power (EIRP). The range in the case of the OOK modulation is lesser due to the high bandwidth requirement and also the high bit error rate due to its non-coherent nature. Using the Friis equation and the noise calculations, we observe that in all the three modulation schemes it is possible to achieve high data rate ($>$ 10 Gbps) communication with a BER of $\sim$ 1e-12. The BPSK case assumes a data rate of 10 Gbps considering only one channel in the design. Ideally, the power from the two antennas can be combined to effectively boost the SNR by 3 dB, thereby allowing a higher data rate or a longer range.

Table 3.1. Wireless link budget for OOK, BPSK and QPSK modulation

	non-coherent OOK	**BPSK**	**QPSK**
Carrier Frequency	240 GHz		
Wavelength	1.25 mm		
Transmitted Power	0 dBm	0 dBm	0 dBm
Tx Antenna Gain	4.9 dB	1.7 dB	1.7 dB
Rx Antenna Gain	1.9 dB	−2.3 dB	−2.3 dB
Range	1.3 cm	1.7 cm	1.7 cm
3 dB Bandwidth	20 GHz	10 GHz	10 GHz
Receiver Noise Figure	18 dB	15 dB	15 dB
Bit-rate	20 Gbps	10 Gbps	20 Gbps
Receiver Power	−35.52 dBm	−45.25 dBm	−45.25 dBm
Antenna Noise	−70.82 dBm	−73.83 dBm	−73.83 dBm
Signal-to-Noise Ratio	17.29 dB	13.58 dB	13.58 dB
Bit Error Rate	1.13 e-12	7.42 e-12	7.42 e-12

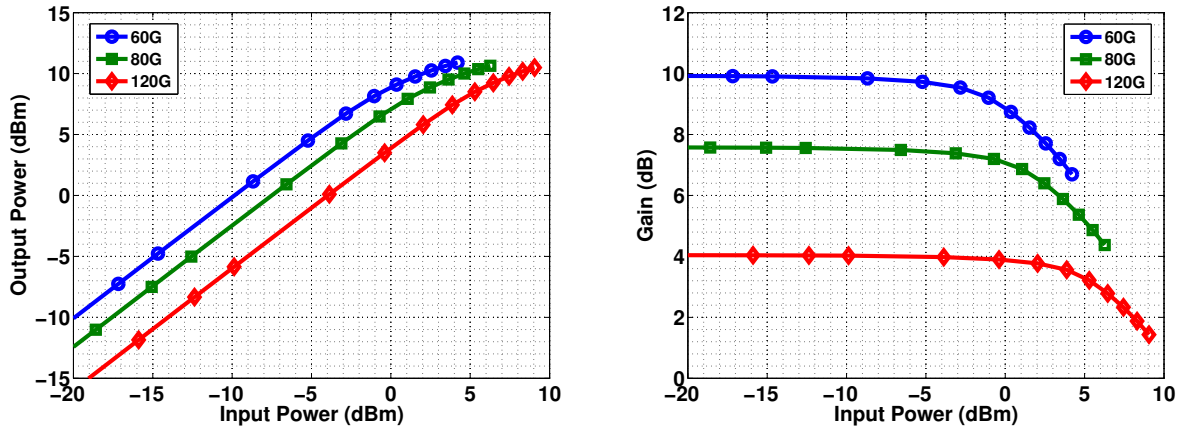


Figure 3.3. Simulated output power [left] and gain [right] as a function of input power at 60 GHz, 80 GHz and 120 GHz for a 54 μm device

3.5 Choice of the intermediate frequency (IF)

As described earlier, the 240 GHz carrier frequency can be generated using three possible harmonic generation techniques from intermediate frequencies 60 GHz, 80 GHz and 120 GHz. A lower IF frequency allows one to generate a higher output power as it is relatively small compared to the cut-off frequency of the device. However, a lower IF requires a a higher frequency multiplication ratio which results in a higher conversion loss. Therefore, given a technology node, there exists an optimal IF frequency and frequency multiplication factor that maximizes the overall conversion efficiency. Fig. 3.3 and Fig. 3.4 show the gain, power added efficiency (PAE) and maximum output power that can be generated using a 54 μm device at 60 GHz, 80 GHz and 120 GHz. As expected, higher amount of power can be generated at a lower intermediate frequency with better efficiency. Additionally the gain per stage is higher which results in lesser number of overall stages and this lowers the total power consumption. For example, operating at an IF greater than 100 GHz results in a maximum gain of 4 dB per stage excluding the matching network losses.

As an example, let us consider the generation of 240 GHz output current of 6.3 mA (corresponding to an output power of 0 dBm for a 50 Ω load) using 80 GHz and 120 GHz IF. This would require a harmonic multiplication of three in the former and two in the latter case. Fig. 3.5 shows the maximum harmonic current that can be generated (and the corresponding required input power) using the two multiplication factors as a function of the gate bias voltage. For the 80 GHz IF, a current of 6.3 mA can be generated with an input power of 7 dBm. This would require an amplifier chain of at least two stages and a total power consumption of around 34 mW with an overall gain of 12 dB. Here, we assumed the last stage to be operating close to saturation (operating at 2 dBm input power) and the driver stage is impedance scaled by a factor of two (operating at -5 dBm input power). In the case of a 120 GHz IF, 4 dBm of input power suffices to generate 6.3 mA of current. However, due to the low gain and efficiency at this frequency, a minimum of three stages of amplification is required with a total power consumption of 70 mW and an overall gain

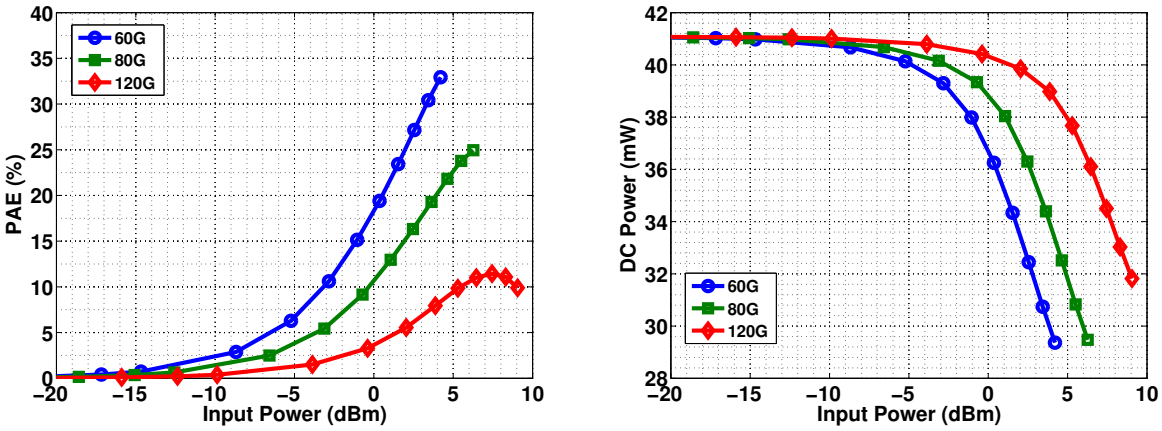


Figure 3.4. Simulated power added efficiency [left] and DC power consumption [right] as a function of input power at 60 GHz, 80 GHz and 120 GHz for a 10 μm device

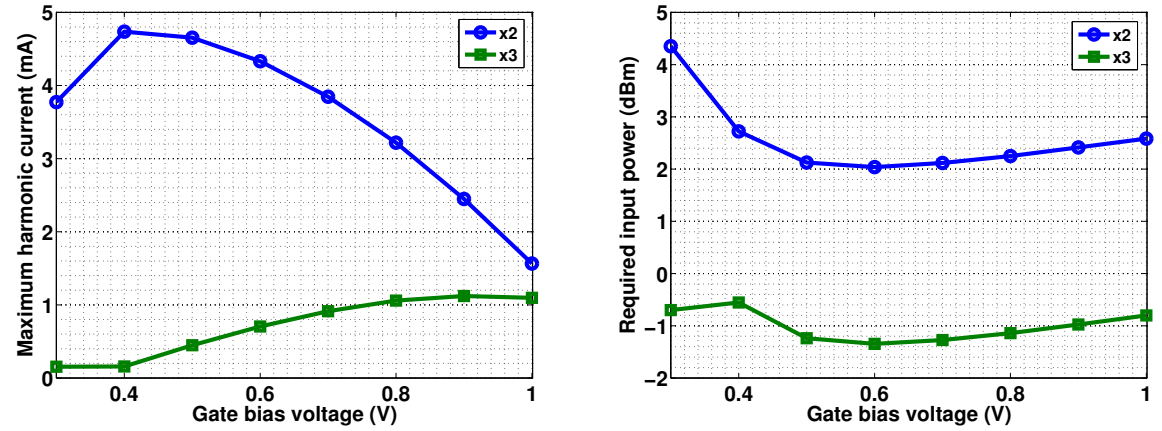


Figure 3.5. Maximum harmonic current [left] and the corresponding required input power [right] as a function of the gate bias voltage for a $\times 2$ (doubler) and $\times 3$ (tripler)

of 12 dB. The operation at 120 GHz also leads to additional passive and matching network losses that aren't considered in the above calculation. Due to this, the IF operation is kept below 100 GHz in both the designs.

The non-linear operation of carrier generation also affects the modulated signal at IF. With a BPSK/QPSK modulation scheme, an even order frequency multiplication ($\times 2$, $\times 4$) distorts the constellation completely. This effect can be avoided by modulating the signal at IF using local oscillators with non-quadrature phase shifts. For example, in the case of a doubler, a BPSK constellation requires modulation with 0°, 90° phase shifted LO waveforms and a QPSK constellation needs 0°, 45°, 90° and 135° phase shifts. This would therefore require phase rotators at the IF which are power inefficient and also difficult to implement. However, a multiplication factor of 3 is beneficial in this case as the BPSK/QPSK constellation is unaffected by this action.

In the first design, a non-coherent OOK scheme is used with an IF of 60 GHz. Multiple power amplifier paths have been implemented to perform envelope detection. This design served as a prototype for verification of modeling approaches and reused the design blocks and expertise at 60 GHz. The second design uses coherent QPSK modulation scheme with 80 GHz as IF and a frequency multiplication of three. This design is four times more efficient and demonstrates the first completely functional link at these frequencies in CMOS technology.

3.6 Local Oscillator (LO) Phase Noise

The local oscillator (LO) phase noise also affects the performance of the transceiver system and distorts the constellation diagram. Due to the frequency multiplication, any spread in the constellation at the IF stage gets magnified further due to the multiplication action. For example, with an 80 GHz IF and $\times 3$ multiplication, the phase error in the constellation at the IF gets amplified three times when observed at the carrier frequency of 240 GHz. This places stringent constraints on the non-linearity of the IF stage namely AM to PM and PM to PM distortions. Additionally, the effect of phase noise on the system performance must be analyzed.

There are various techniques to estimate the phase noise in oscillators [34][35]. For analysis purposes, we use Leeson's phase noise model to simplify the calculations. The phase noise of an oscillator at a frequency offset $\Delta\omega$ is given as

$$L(\Delta\omega) = 10\log\left[\frac{2k_BT}{P_{sig}}.\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \tag{3.9}$$

where ω_0 is the center frequency, Q the quality factor, P_{sig} the output power of the oscillator, k_B the Boltzmann constant and T the temperature. Another important metric that is important is the jitter of the LO clock. If the phase noise of the oscillator is represented as S_ϕ (in magnitude), the variance of the jitter $< \phi(t)^2 >$ can be computed as

$$< \phi(t)^2 >= \int_{-\infty}^{\infty} S_\phi(f)df \tag{3.10}$$

The jitter normalized to the carrier frequency (J_{PER}) is given as

$$J_{PER} = \frac{\sqrt{< \phi(t)^2 >}}{2\pi f_0} \tag{3.11}$$

where f_0 is the carrier frequency.

To estimate the phase noise requirements on the LO, system level simulations were performed using SystemVue for the coherent QPSK modulation scheme based transceiver. The block diagram of the system is shown in Fig. 3.6. Data bits are generated in a random pattern and are then mapped to a QPSK constellation. The data is then up-sampled by a

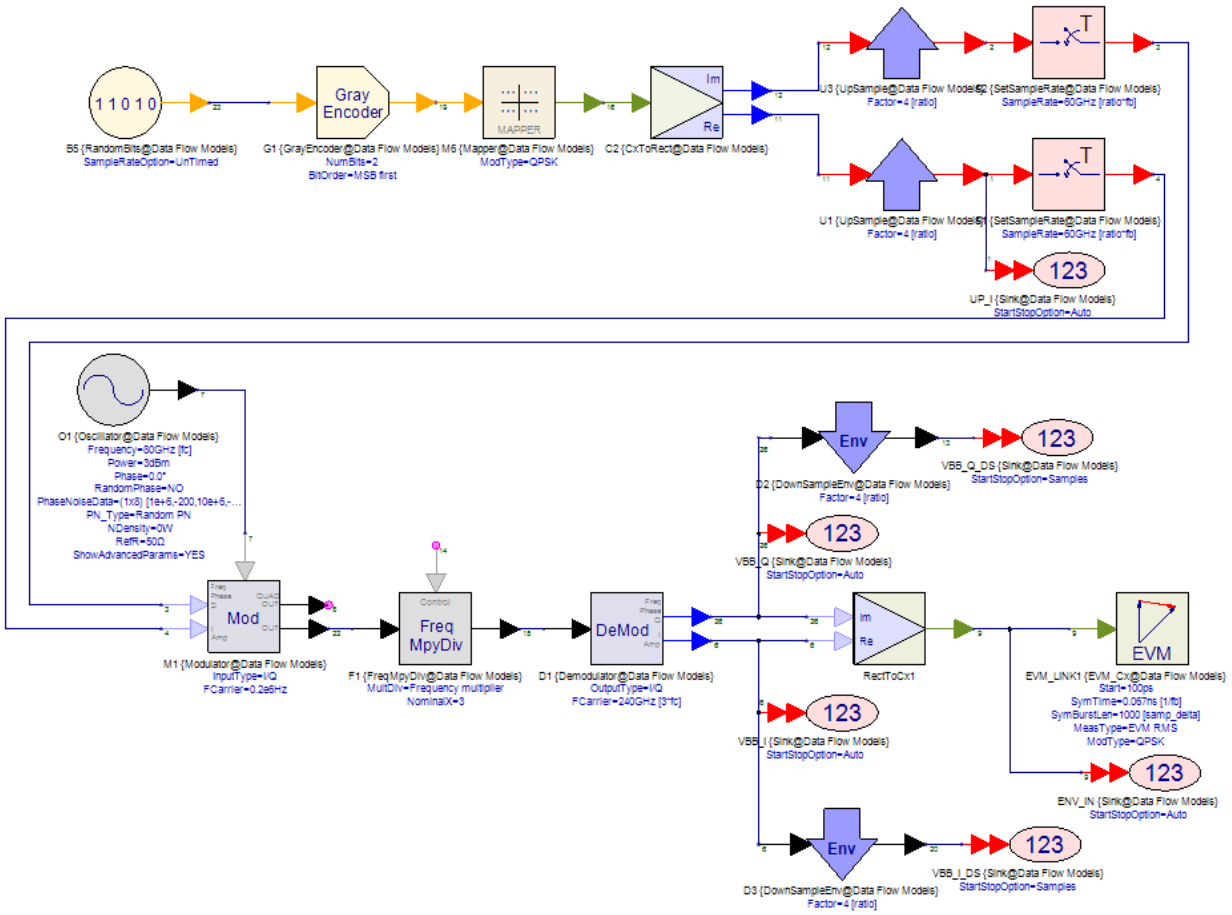


Figure 3.6. Block diagram of the transceiver with LO phase noise

factor of four and mapped on to the continuous time domain with a sampling rate of 60 GHz. This gives an effective data rate of 15 Gbps per channel. The data is then modulated on to the 80 GHz carrier using an oscillator which has a certain phase noise profile. The modulated waveform is then frequency tripled to generate the transmitted signal. The transmitted waveform is then demodulated using an ideal LO clock to obtain the baseband signals. These outputs are then used to evaluate the error vector magnitude (EVM) for QPSK modulation.

In order to determine the phase noise profile, we consider the oscillator design in this work. The 80 GHz oscillator has an output power of -3 dBm. The quality factor of the tank is determined mainly by the loss in the varactor and is around 4 for this design. Using (3.9), we can determine the phase noise at a 1 MHz offset (i.e. $\Delta\omega = 1$ MHz) and this is calculated to be -88 dBc/Hz. The phase noise profile then decays at a slope of 20 dB/decade with frequency. Fig. 3.7 shows the two phase noise profiles used for the system level simulation. The first profile assumes -90 dBc/Hz phase noise at 1 MHz offset and then decays at a slope of 20 dB/decade. The integrated jitter in this case is calculated using (3.11) to be 90 fs at 80 GHz. The integration bandwidth in this case was 1 GHz. The LO clock waveforms used for the transmitter and receiver have certain correlation at lower offset frequencies. This is

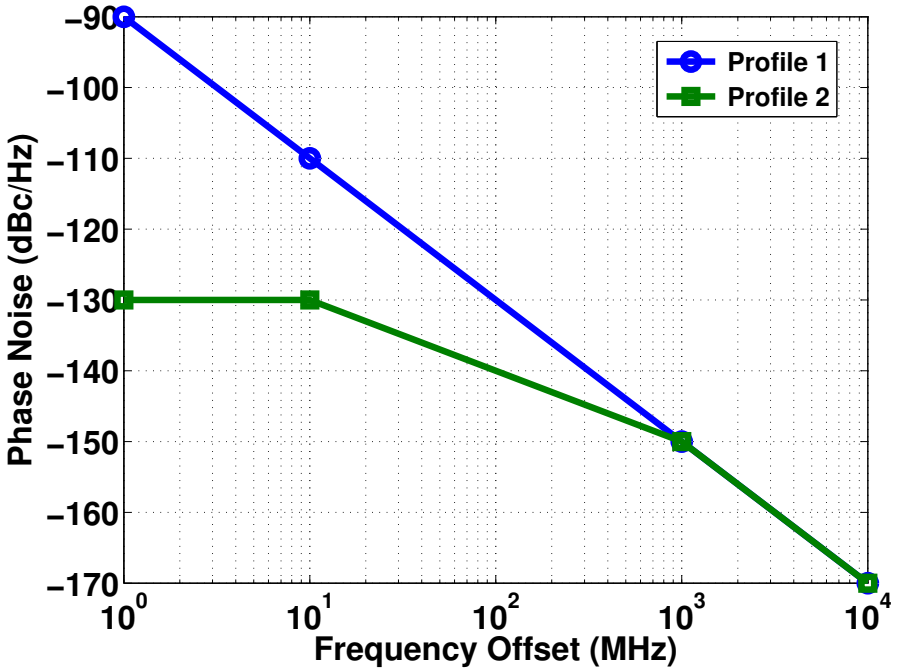


Figure 3.7. Phase noise profiles for the 80 GHz oscillator

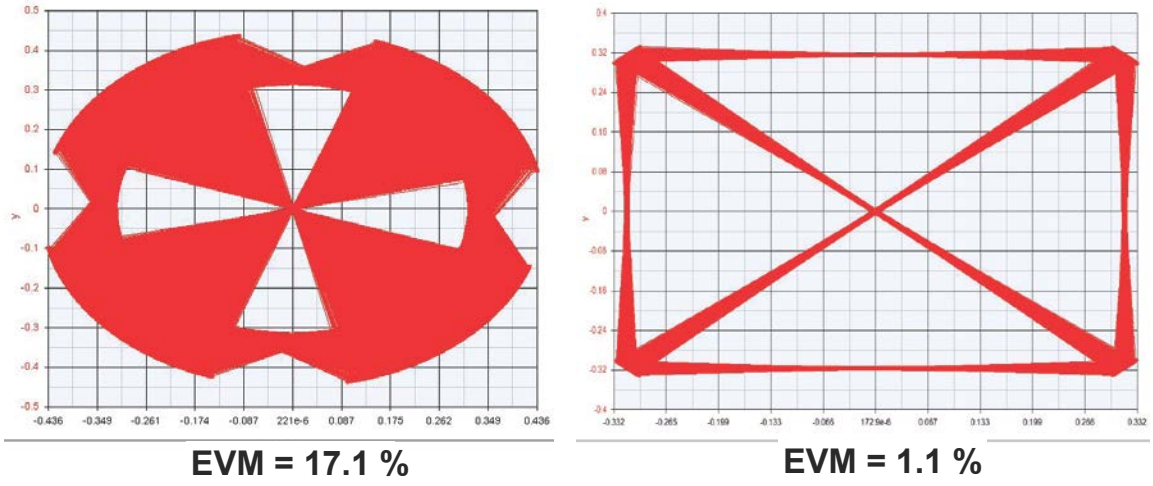


Figure 3.8. Simulation constellation diagram and error vector magnitude (QPSK modulation) with the two phase noise profile - profile 1 [left] and profile 2 [right]

true when the clocks are reference locked to each other or when the receiver clock is recovered from the data using a carrier recovery loop. The second profile mimics this effect by reducing the phase noise at lower frequencies as shown. The integrated jitter in this case is 6.6 fs at 80 GHz.

Fig. 3.8 shows the simulation results with both the profiles for the overall system. The

simulated EVM for the first phase noise profile is 17.1 % and for the second one is only 1.1 %. In order to understand this result, we need to consider the effect of frequency multiplication on the phase noise and jitter of the LO clock. We also need to know the effect of LO clock jitter on the EVM of the received QPSK constellation. From (3.9), we observe that frequency tripling by a factor of three results in a phase noise increase of 9.54 dB. However, the jitter remains unaffected as the carrier frequency also triples as is evident from (3.11). Therefore, in our example, the jitter values calculated at 80 GHz remain the same after frequency tripling. The QPSK constellation of the received data is therefore phase shifted by an amount corresponding to the jitter at this frequency. For a QPSK modulation scheme, if we consider the constellation point $(A/\sqrt{2}, A/\sqrt{2})$, the output power is given by A^2. With a phase shift Φ, the constellation is shifted to $(A\cos(\Phi)/\sqrt{2} - A\sin(\Phi)/\sqrt{2}, A\cos(\Phi)/\sqrt{2} + A\sin(\Phi)/\sqrt{2})$. The EVM is thus given as

$$\text{EVM} = 2\sin(\Phi/2) \tag{3.12}$$

Assuming that the phase noise is small and using the approximation that $\sin(\theta) \approx \theta$ when θ is small, (3.12) becomes

$$\text{EVM} \approx \Phi \tag{3.13}$$

Hence, the EVM is approximately equal to the rms phase shift due to the jitter in the LO clock. For the first phase noise profile with a jitter of 90 fs at 80 GHz and also at 240 GHz, the phase shift is equal to 7.77°. This results in a calculated EVM of 13.44 % which is close to the simulated value. With the second phase noise profile, the calculated phase shift is 0.57° and this results in an EVM of 1 % matching well with simulation as shown in Fig. 3.8.

For any modulation scheme, the bit error P_b and the EVM are related as [36]

$$P_b \approx \frac{2(1-\frac{1}{L})}{\log_2 L} Q\left[\sqrt{\left(\frac{3\log_2 L}{L^2-1}\right)\frac{2}{\text{EVM}^2 \log_2 M}}\right] \tag{3.14}$$

where L is the number of levels in each dimension of the M-ary modulation scheme and Q is the error function. For a QPSK modulation scheme, $L = 2$ and $M = 2$. Hence (3.14) simplifies as

$$P_b \approx Q\left[\sqrt{\frac{1}{\text{EVM}^2}}\right] \tag{3.15}$$

For a BER of $\sim 10^{-12}$, the required EVM is calculated to be -16.7 dB or 14.62 %. This results in a maximum calculated phase shift of 8.37° or a maximum theoretically calculated jitter of 97 fs. We must note that in these calculations the correlation between the transmitter and receiver clocks is not taken into account. However, it still gives us an estimate of the maximum tolerable jitter in the LO clock waveform. For measurement purposes, the Agilent 8267D Vector Signal Generator was used to supply the reference clock. The jitter of this source is 15 fs at 13.33 GHz or 15 fs at 240 GHz (since frequency multiplication does not affect the jitter) which is much lower than the maximum allowed jitter level.

3.7 Other issues

The design of the sub-terahertz system is also affected by several other issues. Since the transceiver design involves a high carrier frequency of operation, several frequency multiplication stages are employed in the design. Additionally, the frequency locking of the transmitter and the receiver requires an external reference which is usually only available at lower frequencies. Hence, multiple blocks need to be designed to lock the high carrier frequency to the external low reference clock. The usage of various frequencies leads to coupling issues between the different blocks and can potentially generate spurious tones that could distort the demodulated waveform. Hence, special care must be taken during layout of sensitive blocks such as usage of extra guard rings and triple well devices for better isolation.

The choice of the external LO reference and data clock frequency also play a critical role in the system functionality. While choosing this frequency, transmitter to receiver board leakages must be taken into account. Since the grounds of the SubMiniature Version A (SMA) connectors are not ideal, the tones can directly leak into the receiver output and corrupt the data signals. Hence, in the second design the external reference frequency has been chosen outside the band of interest.

3.8 Conclusion

We discussed various system level considerations in the design of the sub-terahertz system. The choice of carrier frequency is based on the die area. However, as technology scales this frequency can be increased further to reduce the area occupied by the antennas. Various challenges in the transmitter and receiver design pertaining to the technology node were discussed. Simple modulation schemes such as OOK, BPSK and QPSK can be utilized for communication and the link budget shows their feasibility for centimeter range links. The choice of the IF frequency is also discussed and a $\times 2$ or $\times 3$ frequency multiplication is more favorable in this technology node. Finally, other issues related to LO phase noise and frequency plan were discussed.

Chapter 4

A 260 GHz Wireless Transceiver in 65 nm CMOS

In this chapter, we discuss the design of a sub-terahertz transceiver using on-off keying non-coherent modulation scheme and multiple antennas for beam-forming [37]. Due to the high frequency of operation, the modeling of active and passive devices becomes a critical component determining the overall performance of the transceiver. As modeling techniques are pretty well understood at 60 GHz, this design utilizes the V-band as its intermediate frequency (IF). This allows the design to serve as a prototype to verify the modeling strategies and feasibility of terahertz transceivers in CMOS technology. We first describe the transceiver architecture and then the individual blocks. Even though the final chip was operating at a shifted IF frequency of 65 GHz or a carrier of 260 GHz, the individual blocks would be discussed based on the designed frequency i.e. 60 GHz.

4.1 Transceiver architecture

The block diagram of the transceiver architecture is shown in Fig. 4.1. The block diagram is color coded to indicate the various frequencies.

The transmitter employs a V-band voltage controlled oscillator (VCO) whose output is coupled to an amplification chain consisting of a driving amplifier (DA) and a power amplifier (PA). The outputs from the PA are fed to passive hybrids in two channels as shown. In each channel, the generated in-phase and quadrature (I/Q) signals from the hybrid are amplified further using a similar DA/PA amplification chains. The OOK modulation is performed by integrating a distributed modulator as part of this amplification chain. To test the feasibility of the link, a 7-bit on-chip pseudo random sequence generator (PRBS) is integrated with

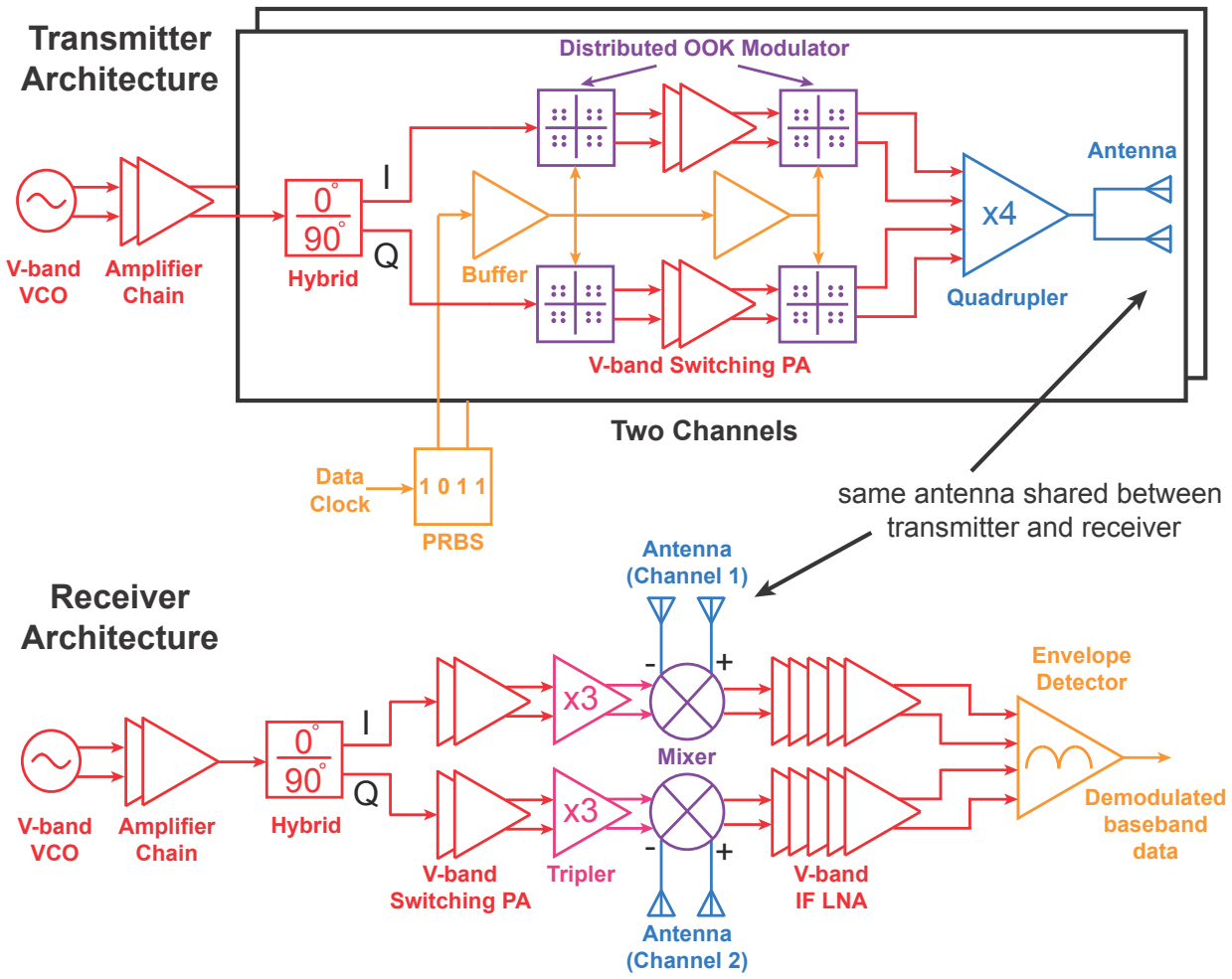


Figure 4.1. Block diagram of transceiver architecture

the design. The outputs from the PRBS drive the voltage mode OOK modulator thereby modulating the data onto the 65 GHz carrier. The modulator is implemented in a distributed fashion to achieve a high on-to-off ratio in the modulated waveform. The 0°, 90°, 180° and 270° modulated phase paths are then combined using a quadrupler to generate the 260 GHz modulated carrier. Two channels of the modulated signals are fed to a leaky wave array antenna structure which combines them spatially to achieve a high equivalent isotropic radiated power (EIRP).

On the receiver side, the same antenna is used to receive the transmitted signal. As the antenna is a leaky wave structure, there is sufficient isolation between the transmitter and the receiver chains and this allows one to avoid a transmit/receive (T/R) switch in this design. The received signal from the antenna is converted to differential using a $\lambda/2$ delay line. As the operating frequency is greater than the maximum oscillation frequency of the device, an upfront low noise amplifier (LNA) is not feasible. Hence, a mixer first architecture is employed to down-converted the received signal to V-band. The mixer is driven by 195 GHz LO signals that are generated in a manner similar to the transmitter. A V-band VCO generates the required LO which is then used to generate the in-phase and quadrature (I/Q) signals using a passive hybrid. These I/Q LO signals are further amplified and drive an active tripler. The non-linear action of the tripler then generates the required 195 GHz LO signal. The down-converted 65 GHz IF signal from the mixer is then amplified using low noise, wideband, high gain IF amplifiers to the desired levels. The noise figure of the IF amplifiers plays a critical role in determining the performance of the receiver as the mixer has conversion gain less than 0 dB. Therefore, the noise figure of the mixer and the IF amplifiers must be minimized to improve the performance of the receiver. The outputs from the IF amplifiers in the two channels with phases 0°, 90°, 180° and 270° are combined using an envelope detector to generate the demodulated signal. The envelope detector is similar in design to the quadrupler except that it generates the 0^{th} harmonic instead of the 4^{th} harmonic in the transmitter case.

4.2 Millimeter-Wave Inverse Class-D Switching Power Amplifier

The theory presented in [38][39] provides an estimate of achievable output power and efficiency given the component parameters of the inverse class-D switching power amplifier. It also qualitatively describes the various trade-offs in the design process thereby allowing the designer an intuition into the design process. However, the actual design process involves Spice level simulation models that accurately predict the required performance metrics. In this section, we describe the design process of the 60 GHz inverse class-D switching power amplifier with measurement results.

4.2.1 Modeling of active devices

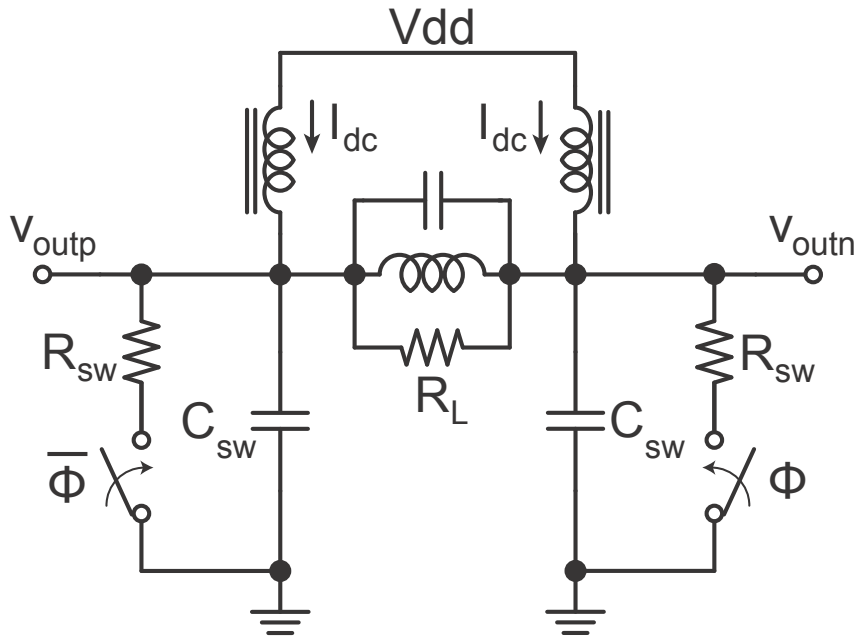


Figure 4.2. Inverse class-D amplifier with the switch model

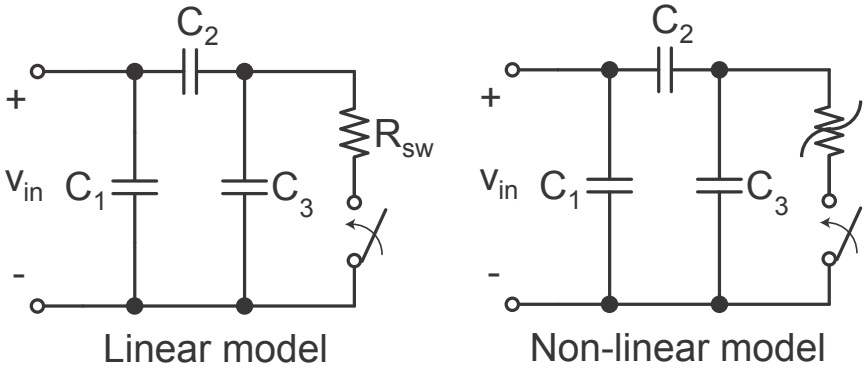


Figure 4.3. Linear and non-linear switch models with device parasitics

Fig. 4.2 shows the circuit of the inverse class-D switching power amplifier. In this circuit, the transistors are modeled as an ideal switch with a series resistance R_{sw} and a capacitance C_{sw}. Fig. 4.3 shows the linear switch model of the transistor. Here C_1, C_2 and C_3 model the total gate-to-source capacitance, gate-to-drain capacitance and drain-to-source capacitance of the transistor respectively. The switch function is controlled using the input v_{in} and as v_{in} is assumed to be a 50 % duty cycle square wave drive, it is grounded in a small signal sense. Thus, the effective switch capacitance C_{sw} is equal to $C_2 + C_3$. Using the linear switch model, the output power and the efficiency of the power amplifier are simulated as

a function of the capacitance ratio and is shown in Fig. 4.4. Here C_{tank} is the explicit tank capacitance excluding the switch capacitance and C_{nom} is the total capacitance required to resonate the tank inductance at the fundamental frequency. The simulation results using the BSIM model is also plotted for comparison. The model predicts grossly incorrect results for the output power and efficiency numbers and the trend of the waveforms is also incorrect.

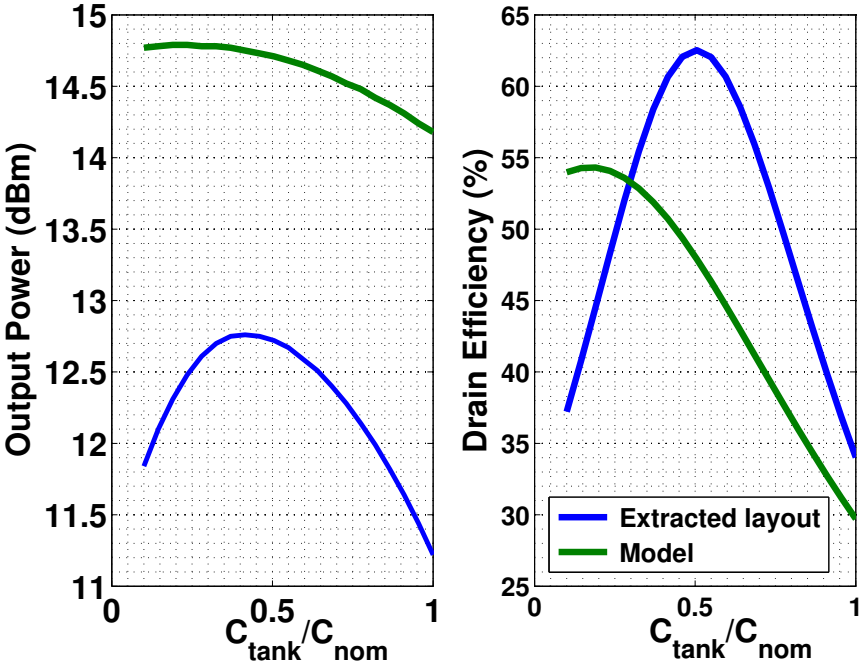


Figure 4.4. Comparison between linear switch model and BSIM model

One of the reasons for this inconsistency is the input drive waveform. Compared to the analysis in [39], the drive waveform at 60 GHz is sinusoidal. This causes the resistance of the switch to vary with the input drive voltage and this dependence is not captured in the linear model. There are two more effects namely the non-linearity of the switch resistance and its dependence on the drain-source voltage and the non-linearity of the capacitance. Simulations reveal that the capacitance of the transistor does not vary significantly as a function of the input drive voltage and the drain-source voltage of the transistor. However, the resistance of the switch is a strong function of the drain-source voltage. To find the non-linear relation, the gate-source voltage was fixed at 1 V (the peak value) and the drain-source voltage was varied from 0 V to the maximum value it could achieve in the circuit. A quadratic equation was empirically fitted to this curve and the resistance R_{sw} can then be expressed as

$$R_{sw} = \left(\frac{a_2 {V_{ds}}^2 + a_1 V_{ds} + a_0}{sf}\right)\left(\frac{1 - V_{th}}{V_{gs} - V_{th}}\right) \tag{4.1}$$

where a_0, a_1 and a_2 are constants, V_{gs} the gate to source voltage, V_{ds} the drain to source voltage, V_{th} the threshold voltage of the transistor and sf the switch scaling factor. Using the above model for the switch resistance and capacitance values calculated as in the case of

the linear switch model, the output power and the efficiency of the switching power amplifier are simulated and the result is shown in Fig. 4.5. The results show a clear match between the non-linear model and the BSIM model with less than 5 % error. The trend of the plots also match accurately as can be seen by the prediction of the maximum efficiency point.

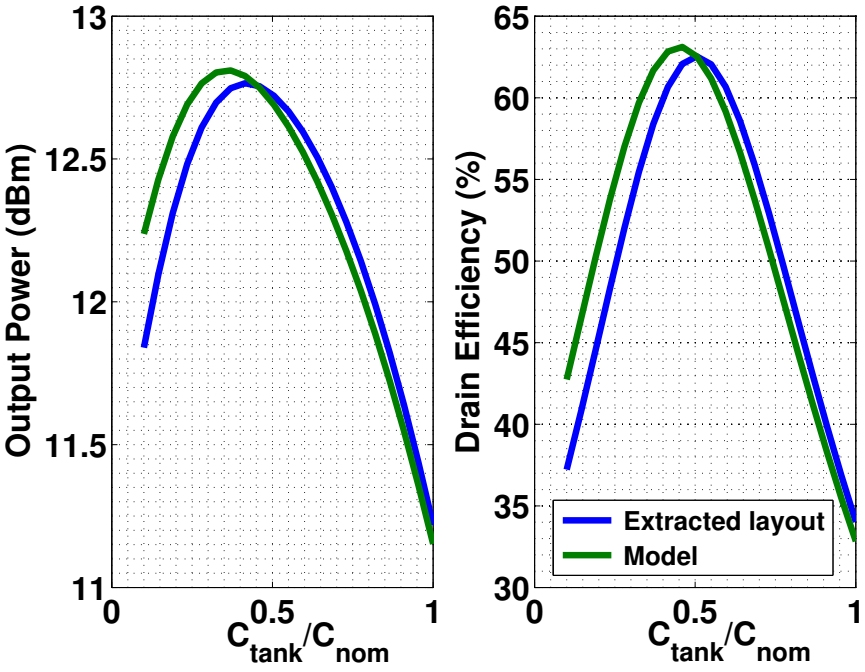


Figure 4.5. Comparison between non-linear switch model and BSIM model

Using the non-linear switch model, the efficiency of the switching power amplifier is simulated for different switch scaling factors and tank capacitance. The efficiency contours are shown in Fig. 4.6. From the simulation results, we observe that the maximum efficiency point occurs when the explicit tank capacitance is zero. Since the device size is modest at these frequencies (due to device capacitance which needs to be resonated by the tank capacitance), the loss due to the switch resistance dominates. Hence, if most of the tank capacitance is contributed by the switches then its resistance can be reduced. We also observe that there exists an optimum switch scaling factor which maximizes the efficiency. This is the point where the capacitance from the switches approximately resonates with the tank inductance. The tank inductance for this design is 96 pH. If a lower switch size is used, then the resistive loss dominates and a large device results in a larger capacitance thereby shifting the resonant point of the tank.

Another technique by which the switch size can be increased is to change the tank inductance accordingly, so that the resonant frequency is kept constant. A plot of the output power and efficiency without any explicit tank capacitance (maximum efficiency point) is shown in Fig. 4.7. As the device size is increased the switch resistance reduces and the efficiency of the amplifier increases. After reaching the maximum point, it starts decreasing gradually due to the second harmonic loss through the switch resistance. In practice however,

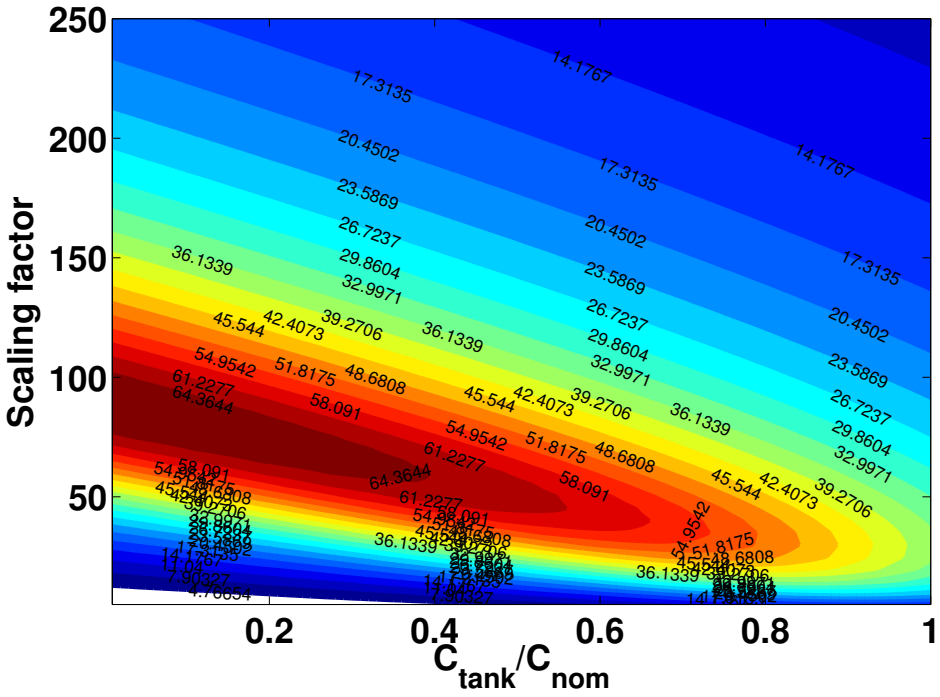


Figure 4.6. Drain efficiency contours using ideal output match for 100 Ω load and quality factor of 3

there is a bound on the minimum achievable tank inductance and this restricts the maximum device size. Furthermore, the tank inductance is usually implemented using a transformer network which matches the amplifier to the output load. The optimal inductance of the transformer does not necessarily coincide with the switching power amplifier optimal point.

The prediction of the switching power amplifier performance also requires accurate prediction of the gate resistance. The gate resistance of a transistor at these frequencies includes two components namely the resistance due to the poly and the other being the non-quasi static (NQS) resistance. The poly resistance is estimated using extraction. The typical way to model the NQS resistance is to add a resistance with a value $1/(5g_m)$ in series with the poly resistance of each transistor [40][41]. Here g_m is the transconductance the device at the DC bias point. However, this is valid only when the device operates in the small signal regime. Switching power amplifiers have large input drives with high drain voltage swings and thus cannot be treated in the same way. In order to estimate the NQS resistance, we find the average channel resistance across one cycle of the power amplifier operation [42]. The waveforms of the inverse class-D switching power amplifier are shown in Fig. 4.8.

The PA is first simulated without the NQS resistance to obtain the approximate voltage waveforms. Then, for each point on the time axis, the channel resistance $R_{channel}$ is calculated as follows.

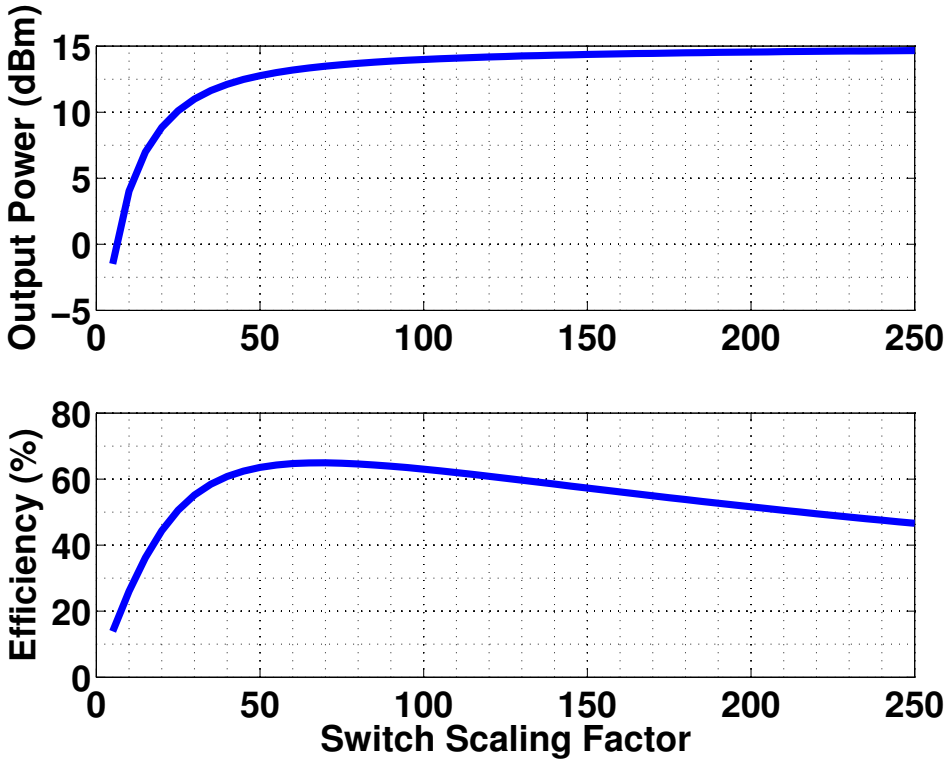


Figure 4.7. Output power and drain efficiency with the tank inductance tuned to the switch capacitance

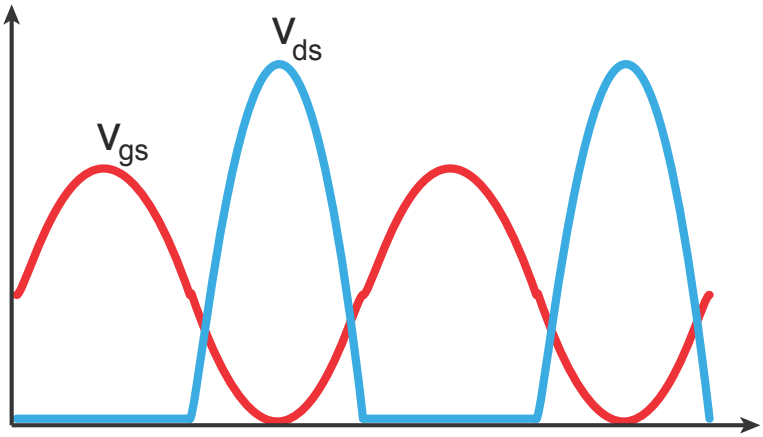


Figure 4.8. Inverse class-D waveforms

$$R_{channel} = \begin{cases} V_{dsat}/I_{ds} & \text{, if } V_{gs} \geq V_{th} \text{ and } V_{ds} \geq V_{dsat} \\ V_{ds}/I_{ds} & \text{, if } V_{gs} \geq V_{th} \text{ and } V_{ds} < V_{dsat} \\ 0 & \text{, if } V_{gs} < V_{th} \end{cases}$$

where V_{gs} is the gate-source voltage, V_{ds} is the drain source voltage, V_{dsat} is the drain-source saturation voltage and V_{th} the threshold voltage. The average channel resistance for a cycle of time period T_0 is then calculated to be

$$\overline{R_{channel}} = \frac{1}{T_0} \int_{T_0} R_{channel} dt \tag{4.2}$$

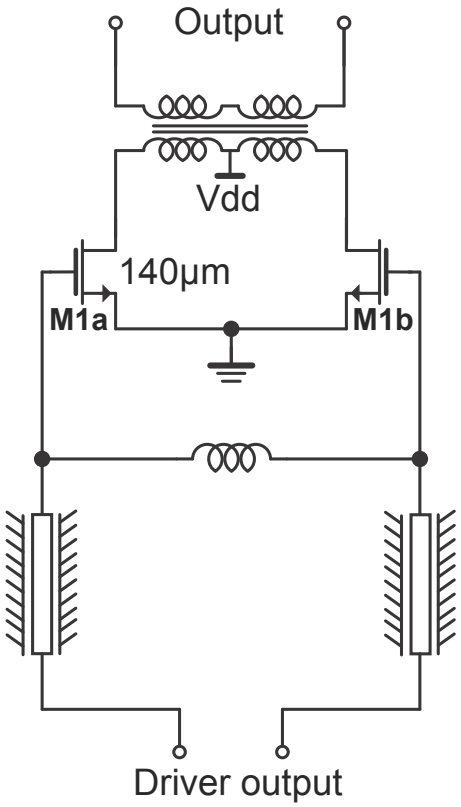


Figure 4.9. Schematic of the Inverse class-D power amplifier

With the above modeling techniques, the switching power amplifier is designed as follows. The conductance and the inductance of the load are estimated from the transformer admittance for a 1 : 1 transformation. The output power and the achievable efficiency for the power amplifier are calculated using the switch model. The PA is made to operate at the maximum efficiency point and the corresponding switch scaling factor is calculated. The circuit is then scaled to resonate the transformer inductance taking into account the output power. However, the efficiency of the PA remains unchanged due to scaling. The intrinsic

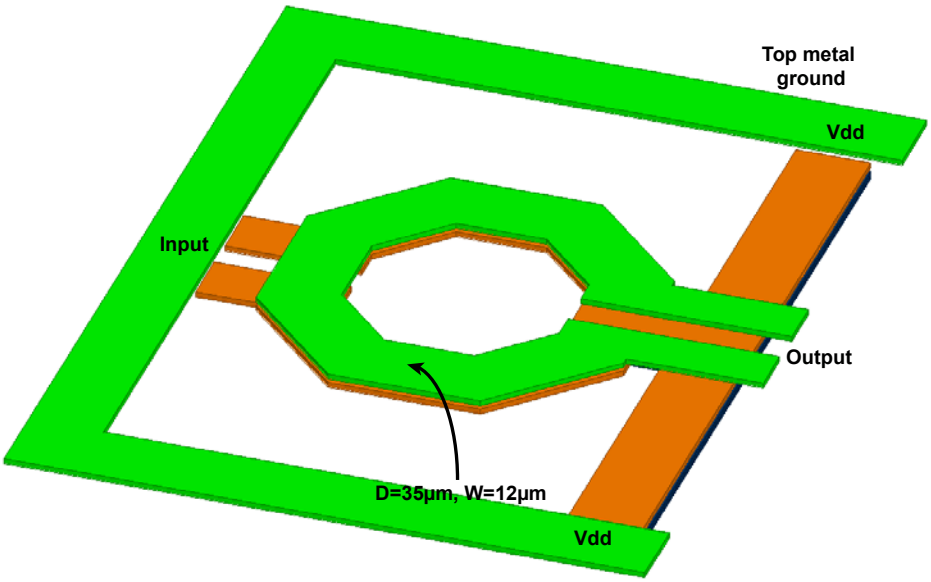


Figure 4.10. Output transformer matching network

efficiency of the PA is then combined with the output transformer power gain (G_p) and the overall maximum efficiency point is calculated.

4.2.2 Switching Power Amplifier Design

The circuit diagram of the inverse class-D switching power amplifier is shown in Fig. 4.9. It consists of a pseudo differential pair M1a and M1b operating in the large signal regime. The transistors are biased at 0.5 V and are nominally driven using a sinusoid of amplitude 0.5 V. The device is sized at $140(1\,\mu\text{m}/0.06\,\mu\text{m})$ using the procedure highlighted above. The PA is interfaced to the load using a 1 : 1 transformer shown in Fig. 4.10. The transformer consists of two vertically coupled inductors. The center tap of the transformer is used to provide the require supply voltage. One would observe that compared to a conventional inverse class-D architecture, no choke is used in this design. This is because there exists an optimum choke inductance that resonants the tank capacitance at the second harmonic of the operating frequency [39]. However, when the tank capacitance consists entirely of the switch capacitance, this optimum occurs at zero choke inductance.

The driver consists of a Class-A amplifier stage for high gain. The output power of the driver stage is determined by the required switching power amplifier input power and the loss through the interstage matching network. The design procedure of the driver is as follows. First, a suitable device size is chosen and load pull simulations are performed. For these simulations the device is biased at its maximum gain region (highest f_{max}). The constant power and gain contours are plotted on the Smith chart as shown in Fig. 4.11. Based on the required power level, an optimal load impedance is chosen. The load impedance must also

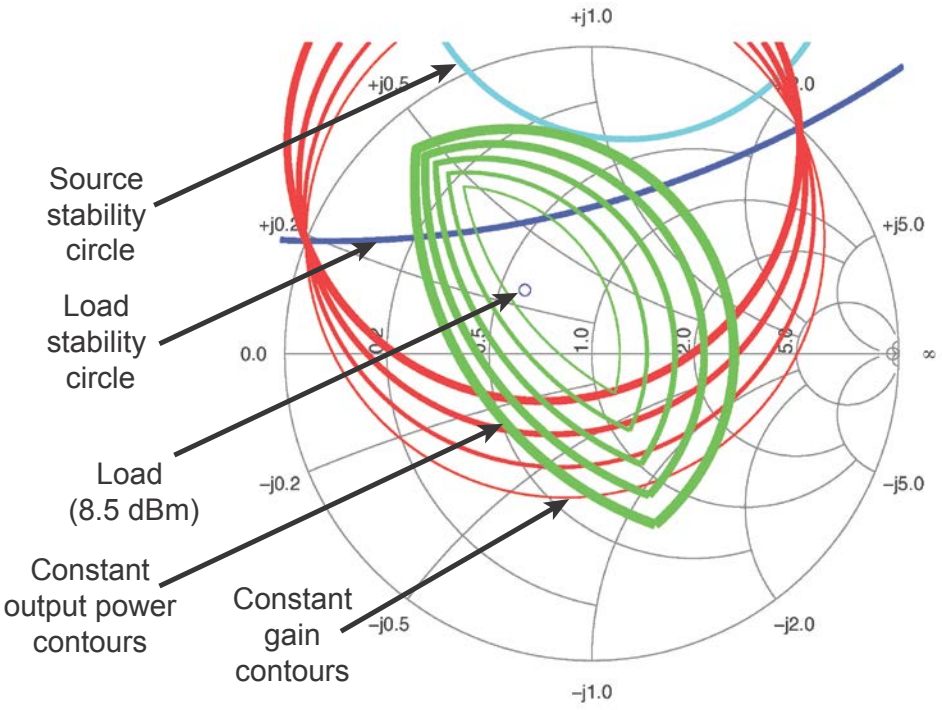


Figure 4.11. Driver stage design - output power and gain contours, load stability circle and source stability circle

be chosen to be far away from the load stability circle. Once the required load impedance is known, a matching network is designed to interface the switching PA to the driver stage. As the loss through the matching network is not known *a priori*, the above procedure must be iterated. In this design the required input power by the switching PA is 3.73 mW. The driver circuit is shown in Fig. 4.12. It consists of a pseudo differential pair M2a and M2b operating in class-A mode. The devices are sized at $54(1\,\mu\text{m}/0.06\,\mu\text{m})$ based on the required output power. The output of the driver stage is coupled to the switching PA stage using the structure shown in Fig. 4.13. Due to the large device size of the switching PA stage, an inductor is added near the gate nodes to resonate the capacitance. The gate nodes are then tapped using microstrip lines as shown. A vertically coupled transformer then performs the final match to the driver stage. The loss of this structure at 60 GHz is simulated to be 2.2 dB. Hence, the driver stage needs to supply 6.2 mW of output power.

The final driver input matching network is shown in Fig. 4.14. It consists of series half inductors followed by a transformer matching network. The dimensions of the transformer are chosen to transform the impedance to $50\,\Omega$ and also to resonate the pad capacitance. The insertion loss of this match is 1.22 dB at 60 GHz.

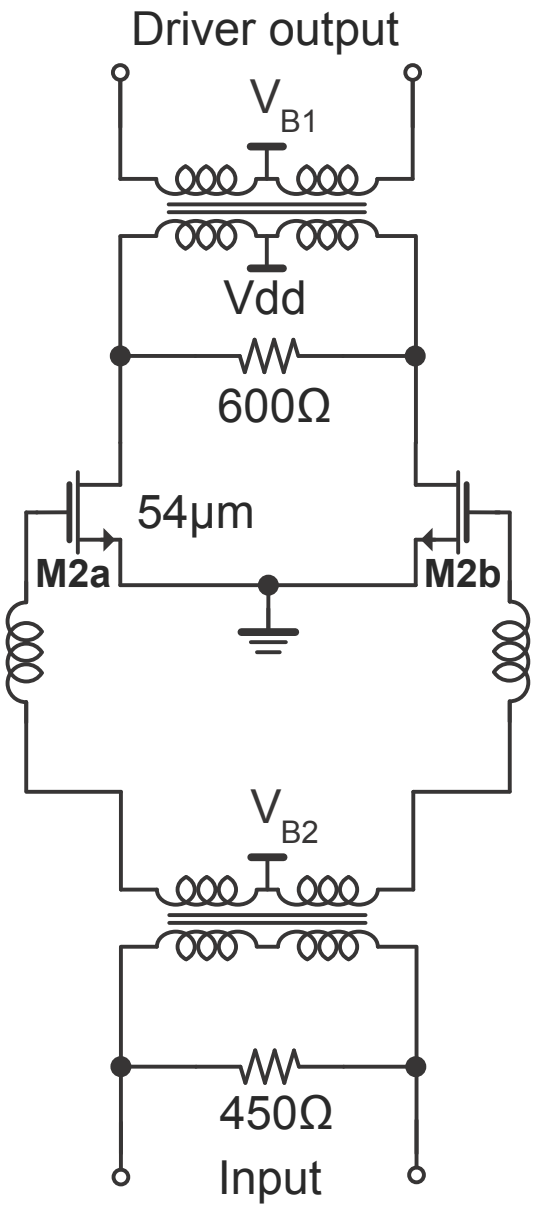


Figure 4.12. Schematic of the Inverse class-D power amplifier driver stage

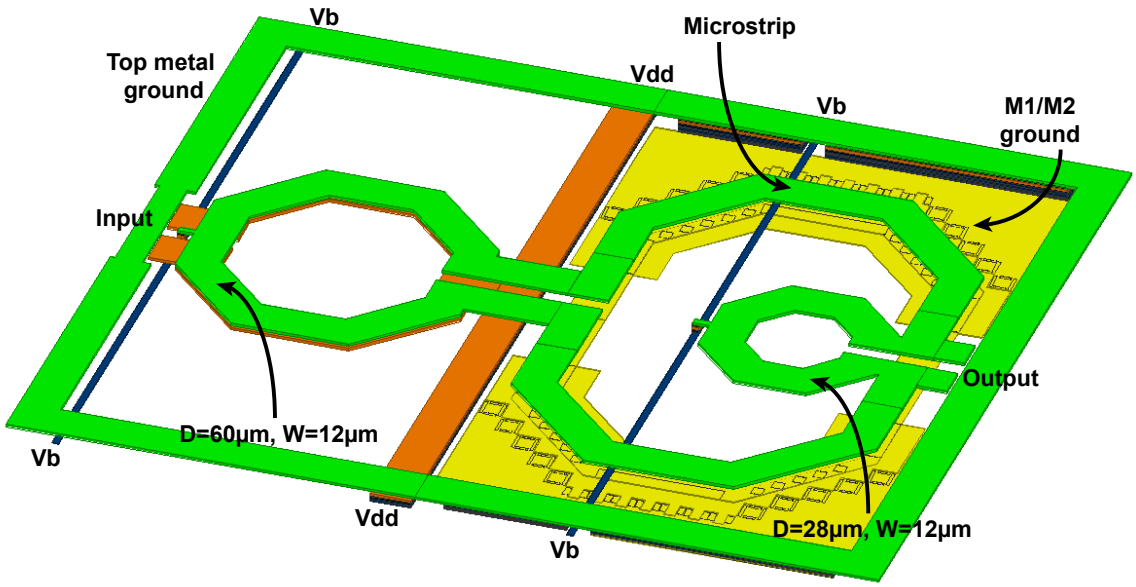


Figure 4.13. Interstage inductor, microstrip, transformer based network

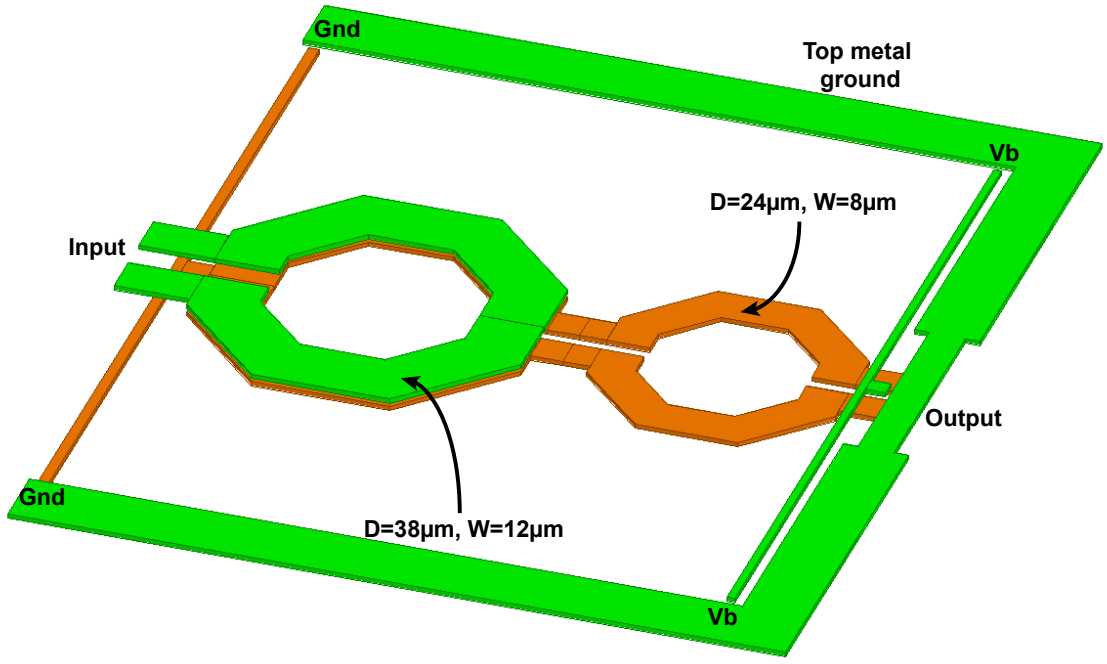


Figure 4.14. Input transformer matching network

4.2.3 Standalone Measurement Results

The switching power amplifier is fabricated in 65 nm bulk CMOS process without any special options. Fig. 4.15 shows the die photo. The chip occupies a total area of 0.39 mm^2 and is pad limited. The chip is characterized using wafer probing.

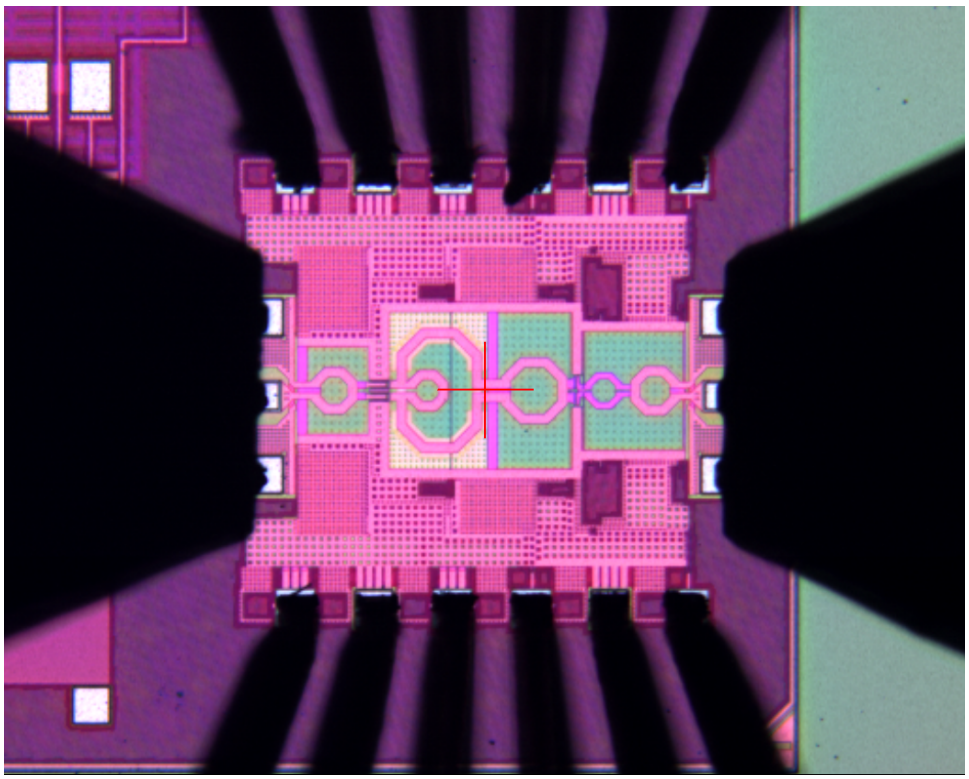


Figure 4.15. Chip microphotograph of the switching power amplifier with probe landing

Fig. 4.16 shows the measured gain of the amplifier as a function of frequency. The PA achieves a gain of 12 dB from 55 GHz to 67 GHz which is close to the simulated gain of 13 dB. The maximum frequency is limited by the measurement equipment capability.

Fig. 4.17 shows the measured output power of the PA as a function of frequency. The PA achieves an average power of 12 dBm across the band of interest. This value is close to the simulated result of 13 dBm. Fig. 4.18 shows the measured power added efficiency (PAE) of the amplifier as a function of frequency. The PA achieves an average efficiency of 21.5 % compared to the simulation result of 23 %. The variation of the output power and PAE of the PA is measured as a function of the supply voltage at 60 GHz. Fig. 4.19 and Fig. 4.20 shows the measured results. The PA achieves a peak power of 13.6 dBm with a PAE of 24 % at a supply voltage of 1.2 V.

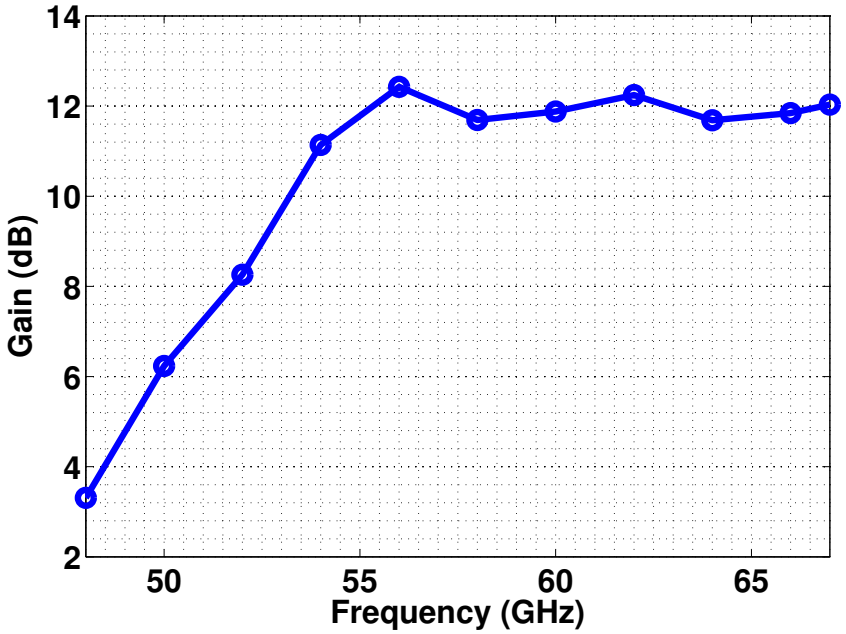


Figure 4.16. Measured gain of the switching power amplifier as a function of frequency

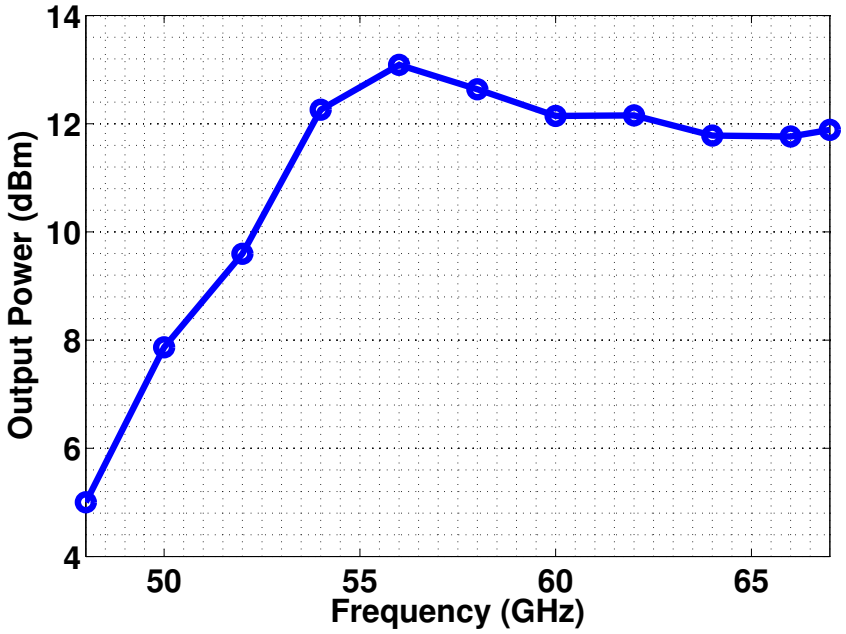


Figure 4.17. Measured output power of the switching power amplifier as a function of frequency

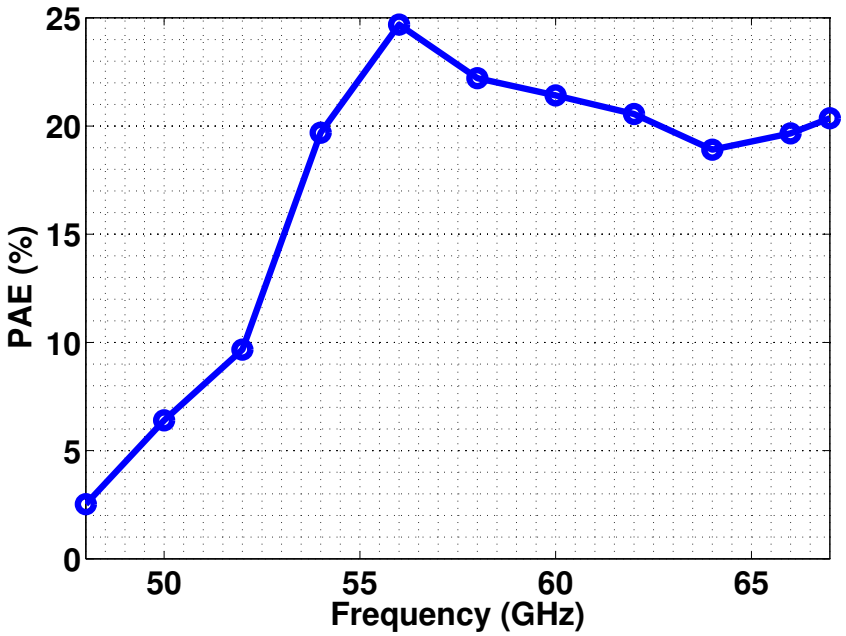


Figure 4.18. Measured power added efficiency (PAE) of the switching power amplifier as a function of frequency

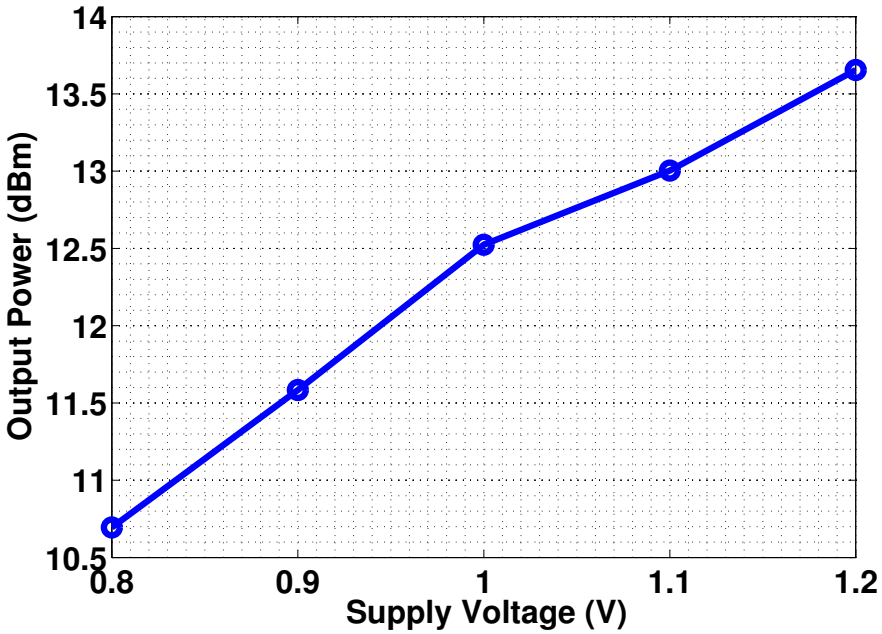


Figure 4.19. Measured output power of the switching power amplifier as a function of the supply voltage

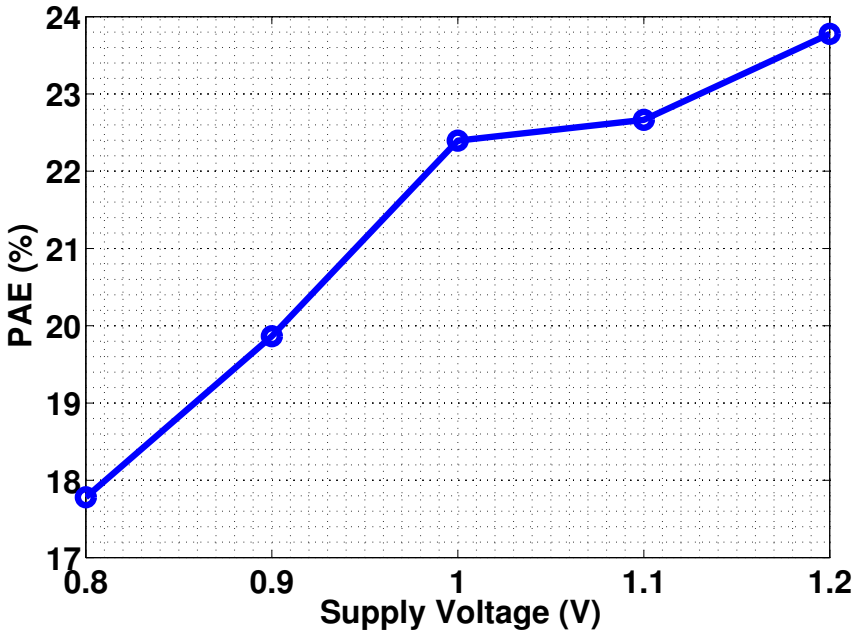


Figure 4.20. Measured PAE of the switching power amplifier as a function of the supply voltage

4.2.4 PA design in the sub-terahertz transceiver

The PA discussed in this section was incorporated into the building blocks of the sub-terahertz transceiver for amplification of the IF signals. The input stage matching network was modified to interface the PA to various other driver stages. On the transmitter side, the distributed modulator was embedded as part of the output transformer matching network and was therefore modified to include the switch capacitance.

4.3 Modulator Design

The schematic of the modulator is shown in Fig. 4.21. It consists of four transistors that operate in voltage mode to perform the OOK modulation. The transistors are driven by inverters whose inputs are fed by the PRBS data. When $\Phi = 1$, the signal path is turned on and the carrier signal from the hybrid is fed to the power amplifier (PA) stage. When $\Phi = 0$, the carrier signal is passed to a dummy load which has the same input impedance as that of the PA. Therefore, the impedance seen by the hybrid stage remains constant in both the on and off cycles of the data. This is required as the hybrid is a resonant structure and changes in the load impedance can cause standing waves in the hybrid which could degrade its operation. In order to achieve high conversion gain, the resistance of the transistors must be minimized which requires a larger device size. However, this results in additional capacitance that increases the required drive power. Additionally, an increased capacitance

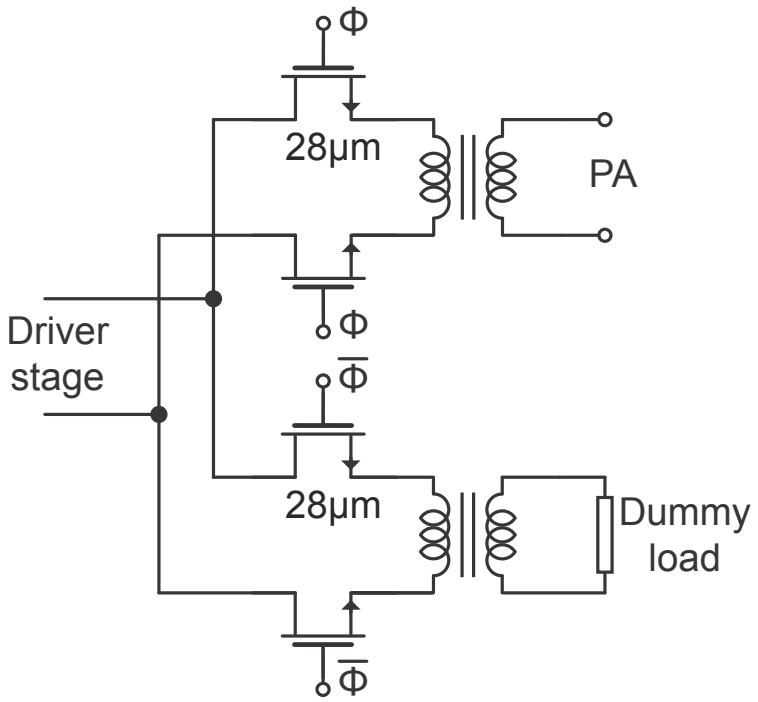


Figure 4.21. Schematic of the voltage mode modulator

needs a lower inductance for resonance. The devices are therefore sized considering all these factors and each device has a size of $28(1\,\mu\text{m}/0.06\,\mu\text{m})$. As the PA has a resonant structure of its own with a modest quality factor around 2, switching the modulator off ($\Phi = 0$) does not turn off the input signal to the quadrupler completely. Therefore, in order to achieve a high on-to-off ratio, another shunt switch is incorporated at the output of the switching PA. As the secondary of the PA sees a lower load resistance, the swing on the secondary side is lesser. Hence, the switch is incorporated in the secondary side to minimize the device stress.

Fig. 4.22 shows the simulated modulator output waveform with PRBS inputs for 20 Gbps OOK modulation. The output of the modulator has a good on-to-off ratio. The resonant structure of the PA slightly degrades the output waveform. However, due to the presence of the shunt switch, the achieved on-to-off ratio is better than 40 dB.

4.4 IF Amplifier Design

In this section, we discuss the design of the intermediate frequency (IF) amplifier operating at 60 GHz. As mentioned earlier, as the operating frequency of the receiver is greater than the maximum oscillation frequency (f_{max}) of the device, a low noise amplifier (LNA) cannot be used in the front-end of the receiver chain. Additionally, as the mixer has no conversion gain, the noise figure of the amplifier plays a critical role in determining the

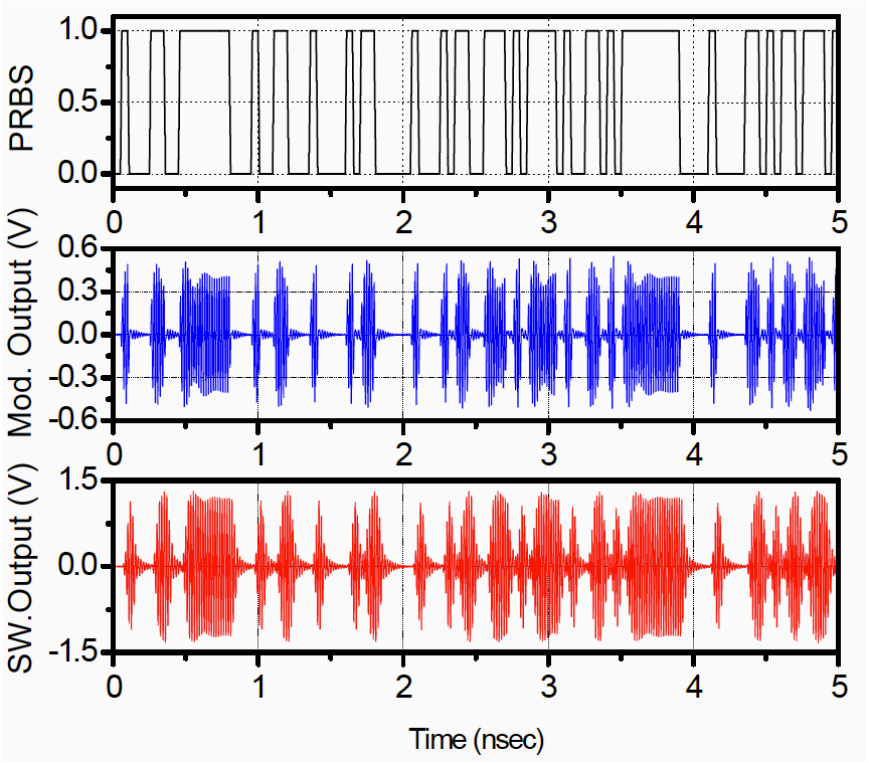


Figure 4.22. Simulated modulator output and PA output with PRBS input waveform

overall noise figure of the receiver chain. Due to the high path loss at this frequency, the receiver signal power level is around −31 dBm for a transmit EIRP of 5 dBm at a distance of 1 cm. Since the mixer has no conversion gain, the IF amplifier must provide high gain around the V-band to boost the signal to detectable levels. The required gain is around 27 dB for this design. The IF amplifier must also be wideband in nature to allow high data rate communication. For data rates upto 20 Gbps, the required theoretical bandwidth is 40 GHz. However, most of the energy is within the 3 dB point of the main lobe or within 20 GHz. Hence, the main challenge in this design has been to maximize the bandwidth of the IF amplifier with high gain while minimizing the noise figure.

One of the direct ways of realizing this amplifier is to build a cascade of second order systems. For a cascade of identical biquads with a quality factor Q_P and center frequency $\omega_P = 1$, the bandwidth of the cascade BW_{casc} can be derived to be

$$BW_{casc} = \frac{\sqrt{2^{1/n} - 1}}{Q_P} \tag{4.3}$$

where n is the number of stages.

We can rewrite (4.3) as

$$BW_{casc} = GBW_{stage} \frac{\sqrt{2^{1/n} - 1}}{A_{casc}^{1/n}} \tag{4.4}$$

where GBW_{stage} is the gain-bandwidth per stage and A_{casc} is the gain of the cascade or the required overall gain. Using (4.4) with a required power gain of 33 dB accounting for low quality factor matching networks, the bandwidth of the cascade of the amplifiers is calculated to be 10.5 GHz with a quality factor of 2 per stage. The total number of required stages is 6. Even though the above design is viable, it leads to a higher power consumption due to a larger number of stages and this is due to the fact that the high bandwidth is being achieved using second order biquads. A more efficient way of realizing the amplifier is by using higher order transfer functions where the poles can be placed in an optimal manner to achieve the required bandwidth. A similar approach was followed using capacitive coupling in [14]. Here, two resonators are coupled using capacitors. As the coupling is electric (rather than magnetic), the inductors in the resonators must be uncoupled and therefore occupy a larger area. The inductors were realized using transmission lines that further increased the die area. In this design, we use a low coupling coefficient transformer to achieve the higher order transfer functions. By magnetically coupling the inductors, the implementation is more compact. Additionally, the center taps of the transformer provided can be used to conveniently provide the supply and DC biasing. The same idea was used for the design in Chapter 2. Here, we discuss it in further detail.

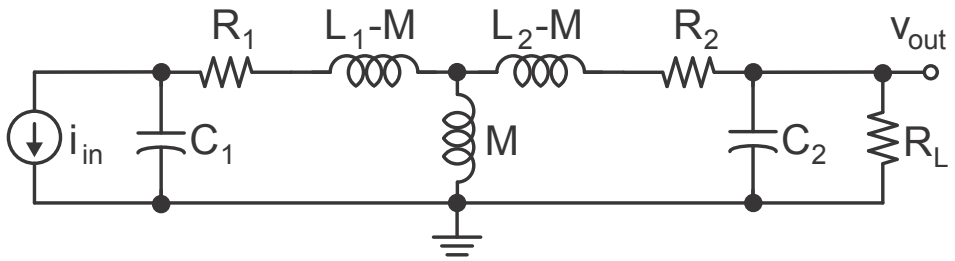


Figure 4.23. Transformer equivalent model

Fig. 4.23 shows the transformer model with the transistor being modeled as a current source i_{in}. Here, L_1 and L_2 are the inductances of the primary and the secondary coils and M is the mutual inductance between them. The quality factor of the inductors is modeled using resistors R_1 and R_2. C_1 models the device capacitance of the input transistors and the parasitic capacitance between the leads of the primary. C_2 models the device capacitance of the subsequent stage and the parasitic capacitance between the leads of the secondary. R_L models the gate resistance seen into the subsequent stage. The coupling coefficient k is given by $k = M/\sqrt{L_1 L_2}$.

A transformer has two modes of operation namely resonance and anti-resonance. In the resonant mode, the current flows in phase in the primary and secondary and increases the overall magnetic field. This is the case when the coupling coefficient is high. In the anti-resonance mode, the currents flow in opposite phases and reduce the magnetic field. Under this condition, the coupling coefficient is low and the transformer behaves mainly as a a fourth order system. The transfer function between the output voltage v_{out} and input current i_{in} can be derived to be

$$\frac{v_{out}}{i_{in}} = -R_L \frac{sM}{s^3M^2C_1(1+sR_LC_2) - (1+sR_1C_1+s^2L_1C_1)[R_L+(R_2+sL_2)(1+sR_LC_2)]} \tag{4.5}$$

Under a low coupling case i.e. $M \ll 1$, (4.5) becomes

$$\frac{v_{out}}{i_{in}} = \frac{sM}{[1+sR_1C_1+s^2L_1C_1][1+\frac{R_2}{R_L}+s(\frac{L_2}{R_L}+R_2C_2)+s^2L_2C_2]} \tag{4.6}$$

Fig. 2.12 shows the normalized magnitude response of the transformer as a function of the coupling coefficient. For the high coupling coefficient case, the second pole pair occurs at a higher frequency and the two pole pairs of the fourth order system are well separated. As the coupling coefficient is reduced, the second pole pair is moved in-band and one could then use filter techniques to achieve the required passband response. For example, when $k = 0.01$, the transformer has a maximally flat response as shown. There are many possible filter responses for the transfer function namely Butterworth, Chebyshev, Inverse-Chebyshev, Elliptic, etc. Of these, the Butterworth response is maximally flat and has an almost constant group delay in-band. This is essential for an OOK modulation scheme as a non-constant group delay spreads the bits apart and reduces the on-to-off ratio. For this reason, a Butterworth response is selected in this design.

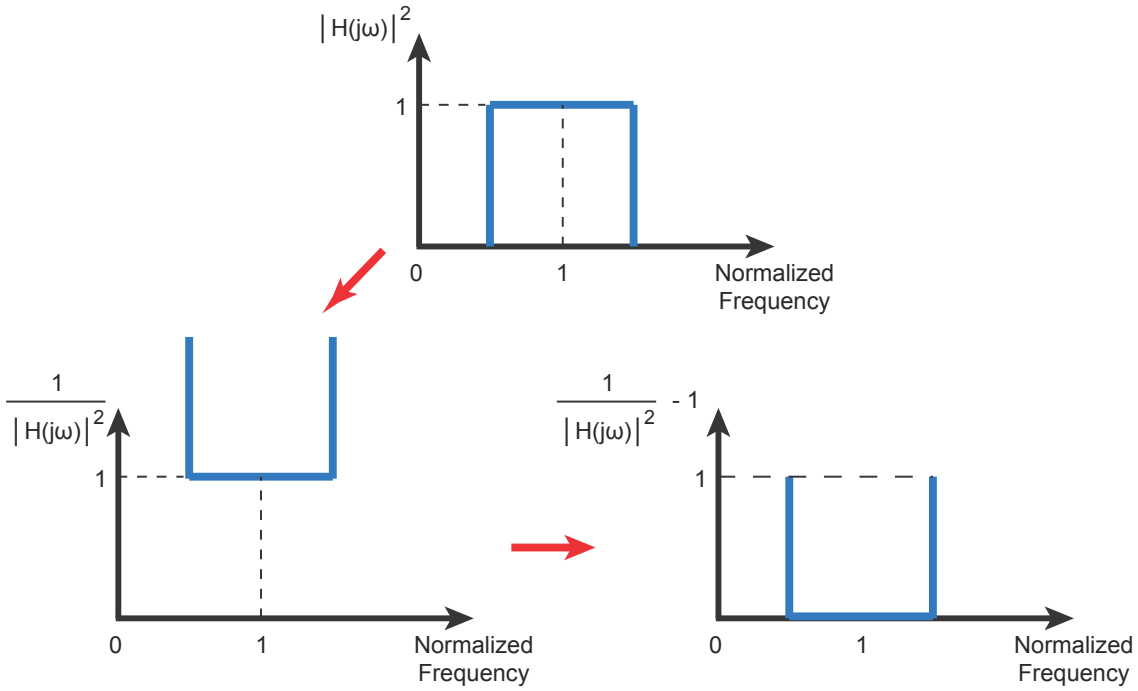


Figure 4.24. Procedure to obtain maximally flat bandpass response

To calculate the conditions required to satisfy the Butterworth response, we write the generalized transfer function $H(s)$ of the transformer i.e.

$$H(s) = \frac{\sqrt{[(a_0 - a_2 + 1)^2 + (a_1 - a_3)^2]}s}{s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{4.7}$$

where a_0, a_1, a_2, a_3 and a_4 are coefficients related to the transformer parameters. The square of the frequency response is given as

$$|H(j\omega)|^2 = \frac{[(a_0 - a_2 + 1)^2 + (a_1 - a_3)^2]\omega^2}{(a_0 - a_2\omega^2 + \omega^4)^2 + (a_1\omega - a_3\omega^3)^2} \tag{4.8}$$

Fig. 4.24 shows the procedure required to obtain maximally flat bandpass response. The required frequency response $|H(j\omega)|^2$ must be maximally flat across the normalized unity frequency. As evident from the figure, this is equivalent to setting maximum number of derivatives of $1/|H(j\omega)|^2 - 1$ to zero near the normalized unity frequency. As there are only four coefficients, the maximum number of derivatives that can be set to zero is three. We therefore have

$$\frac{1}{|H(j\omega)|^2} - 1 = \frac{(a_0 - a_2\omega^2 + \omega^4)^2 + (a_1\omega - a_3\omega^3)^2 - [(a_0 - a_2 + 1)^2 + (a_1 - a_3)^2]\omega^2}{[(a_0 - a_2 + 1)^2 + (a_1 - a_3)^2]\omega^2} \tag{4.9}$$

and we need to set

$$\left| \frac{\partial^i \left[\frac{1}{|H(j\omega)|^2} - 1 \right]}{\partial \omega^i} \right|_{\omega=1} = 0 \tag{4.10}$$

for $i = 1, 2, 3$. The solution for the above set of equations is given in Table 4.1. There are three possible sets of solution each with a single degree of freedom. The root locus of the poles of the system for the first case (with varying a_1) is shown in Fig. 4.25. For a second order system with a normalized center frequency, the quality factor of the poles is given by one-half of the inverse of its real value. Hence, from the root locus plot there exists a solution where the quality factor of the pole pairs are the same. This is the solution given in (4.6), where the quality factors of both the poles pairs are chosen to be the same and the coupling coefficient $k = 1/Q$ [26].

We now discuss the design of the IF amplifier using the above theoretical analysis. The IF amplifier consists of five stages with the input stage matched for low noise figure. By considering only the first stage to be the dominant noise contributer, the noise factor of the IF amplifier is given as

$$F = 1 + \frac{R_g}{R_s} + 2g_m R_s \left(\frac{\omega}{\omega_T} \right)^2 \tag{4.11}$$

where R_g is the gate resistance of the input transistor, R_s the source resistance, g_m the transconductance of the amplifier, ω the operating frequency and ω_T the transition frequency of the device.

Table 4.1. Calculated coefficients of the transfer functions for maximally flat response

$\mathbf{a_0}$	$\mathbf{a_1}$	$\mathbf{a_2}$	$\mathbf{a_3}$
1	a_1	2	0
1	$a_3 + {a_3}^3/8$	$2 + {a_3}^2/2$	a_3
-1	$a_3 + {a_3}^3/8 - 2/a_3$	$2 + {a_3}^2/2$	a_3

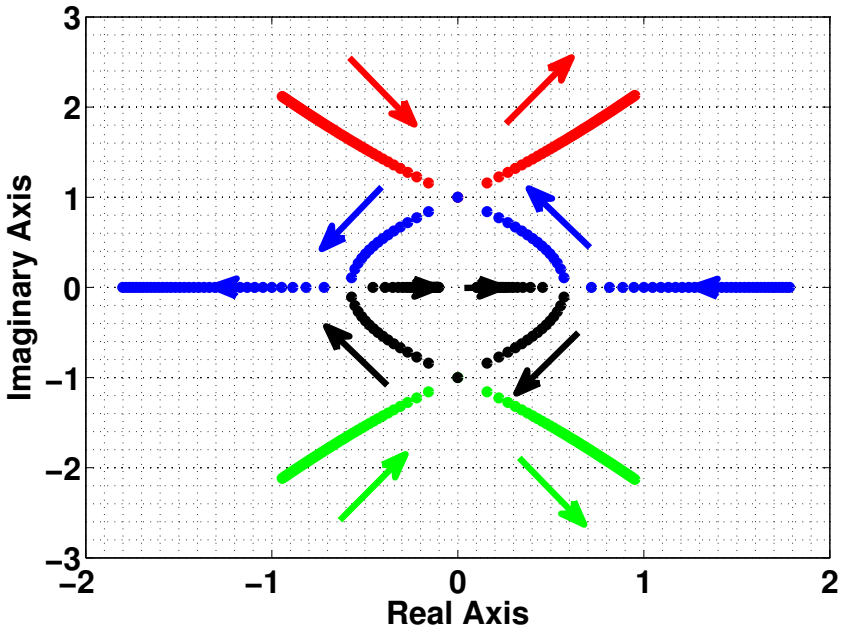


Figure 4.25. Root locus plot of the maximally flat transfer function

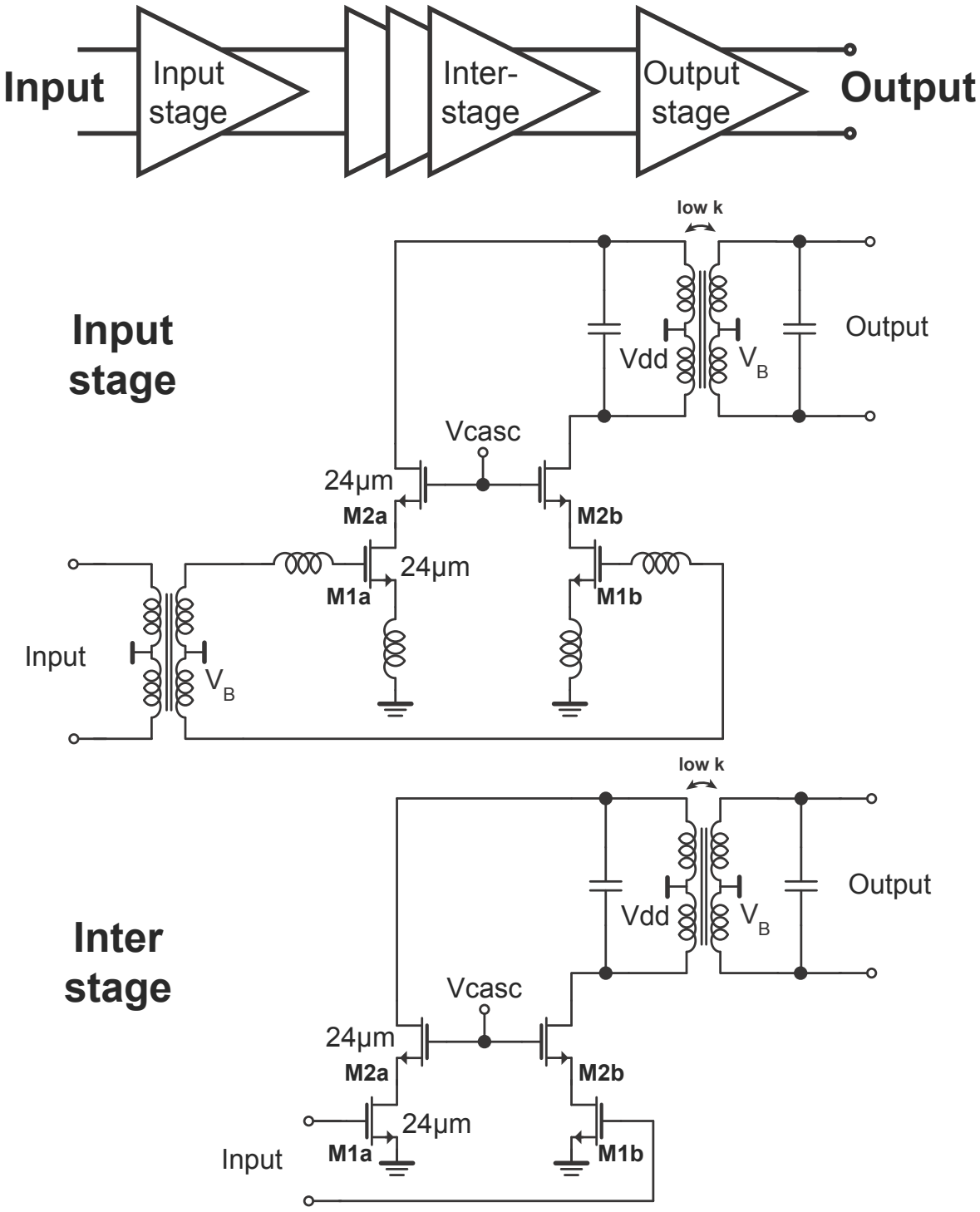


Figure 4.26. Schematic of tthe five stage IF amplifier with the input and interstage networks

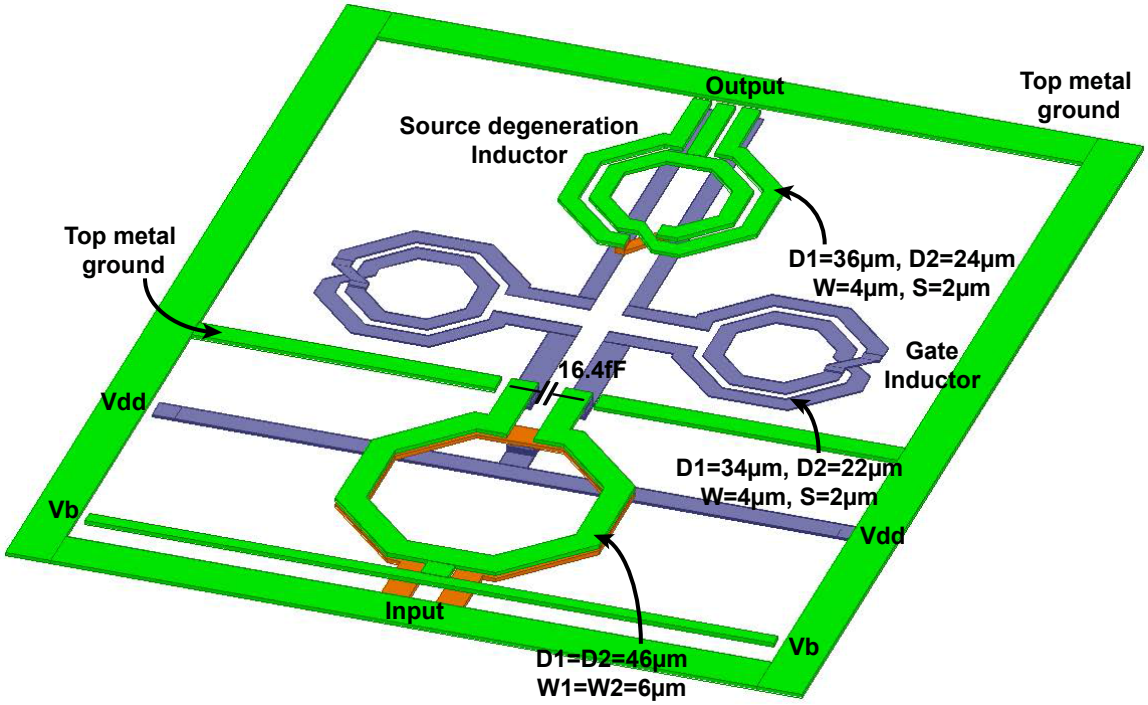


Figure 4.27. Layout of the input matching network with degenerating inductors

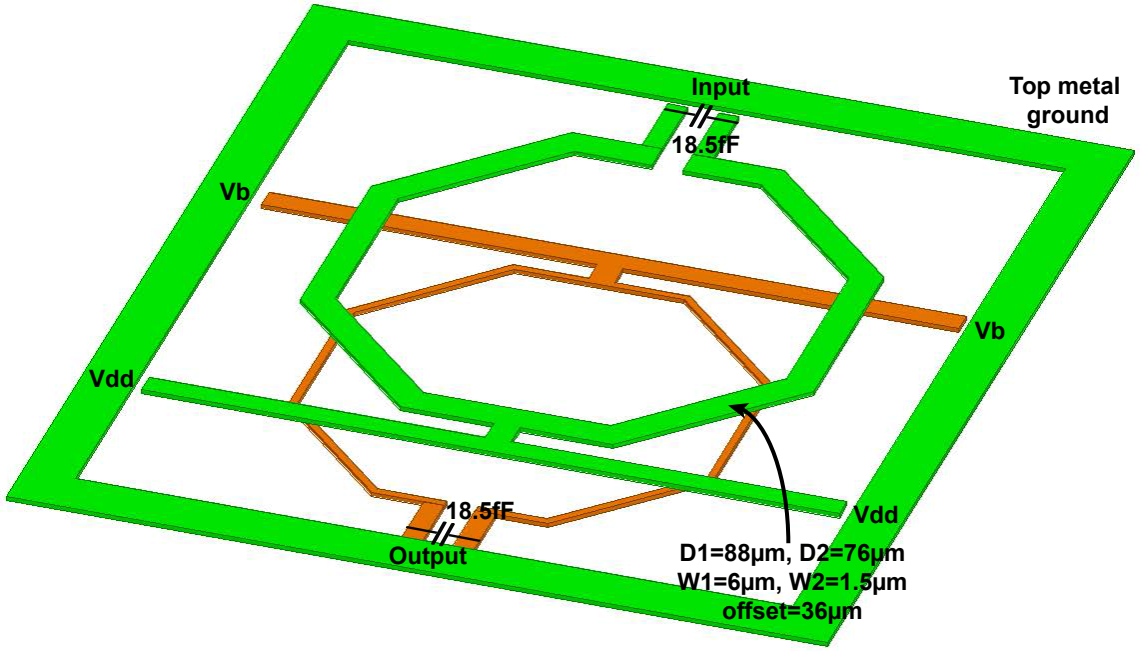


Figure 4.28. Layout of the low-k transformer matching network

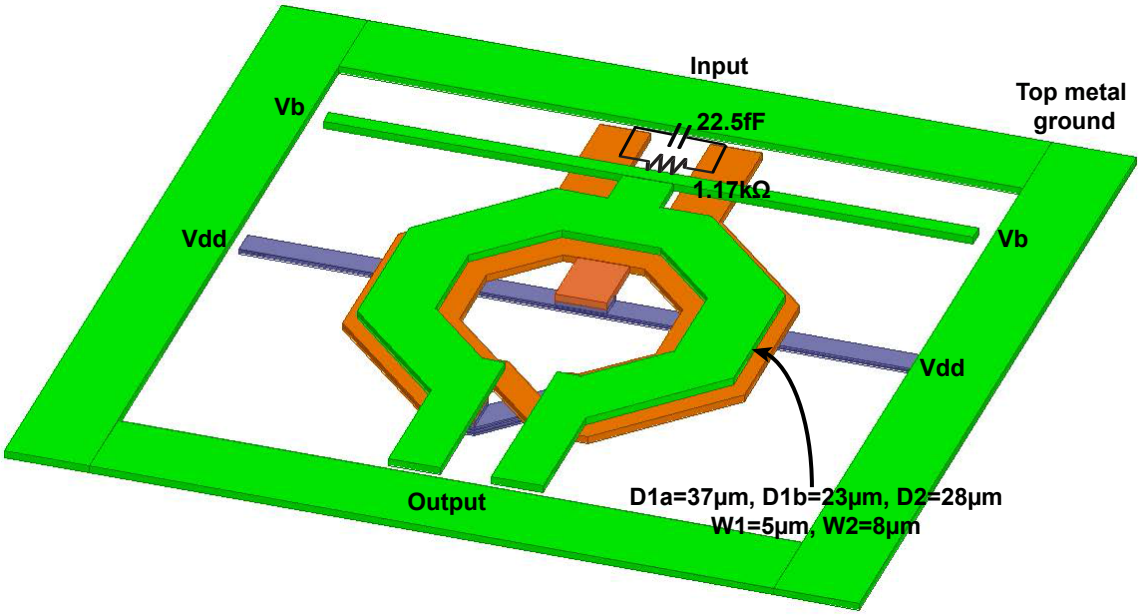


Figure 4.29. Layout of the output transformer matching network

The mixer requires an impedance termination of 100 Ω, which places the constraint for the optimal noise resistance to be 100 Ω. This leads to a required g_m of 30 mS. Fig. 4.26 shows the schematic of the IF amplifier with the input and interstage networks. In order to obtain an input power match, the input stage is degenerated using inductors [43]. Each transistor leg requires a degenerating inductance of 71 pH. The device is then biased at the maximum f_{max} point which is a gate-source voltage bias of 600 mV. The size of the device is then selected based on the calculated g_m. The IF amplifier consists of differential pairs M1a and M1b and uses cascode stages M2a and M2b for added stability and higher gain. Each device in the amplifier has a size of $24(1\,\mu\text{m}/0.06\,\mu\text{m})$. and consumes 6 mA of current. Fig. 4.27 shows the layout of the input matching network. The degenerating inductors are implemented as a two turn inductor with its center tap tied to the ground node as shown. The gate traces are run on a lower metal below the degenerating inductor. Since the lower metal layers have a higher resistance, the length of the line is minimized and its width maximized to avoid further losses as these directly affect the noise figure of the amplifier. The series gate inductors are implemented on the lower metal layer. Each gate requires a series inductance of 460 pH. However, the gate traces below the degenerating inductor transforms the impedance so that each leg requires only 170 pH to resonate the capacitive portion of the input impedance. The final match between the mixer and the IF amplifier is performed using a 1 : 1 transformer network. The DC bias for the IF amplifier is provided using the center tap of the transformer. The interstage networks of the IF amplifier are similar to the input stage and their outputs are coupled to the subsequent stages using low coupling coefficient transformer networks discuss previously.

Fig. 4.28 shows the layout structure of the interstage matching networks. It consists of two loop inductors that are coupled vertically. The inductors are offset from their centers

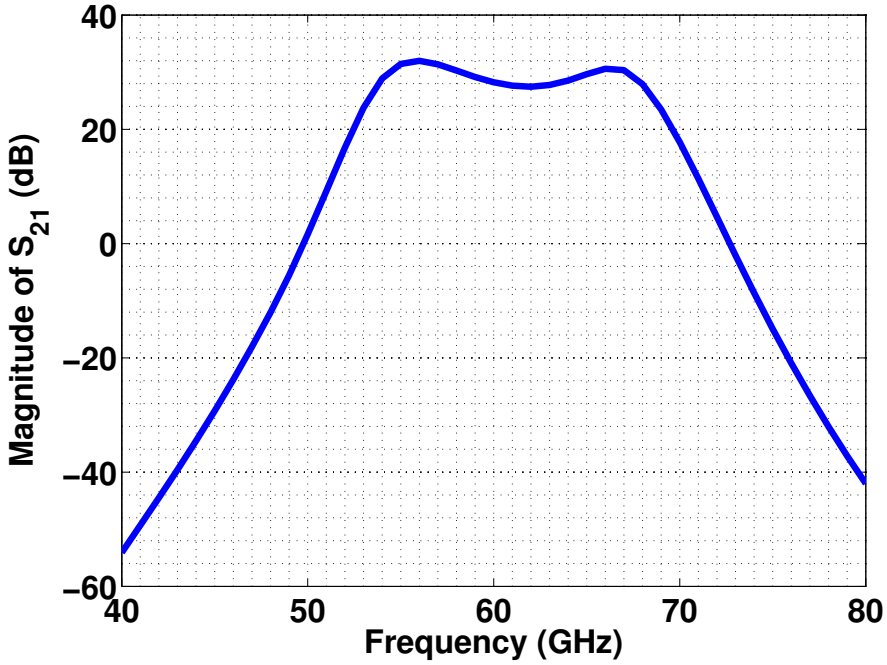


Figure 4.30. Simulated gain (S_{21}) of the IF amplifier

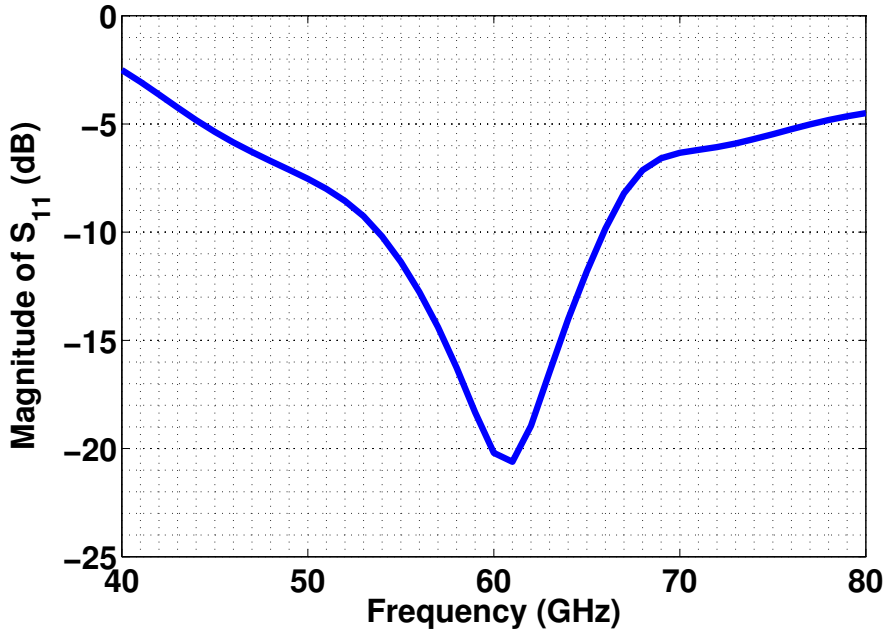


Figure 4.31. Simulated gain (S_{11}) of the IF amplifier

and the offset distance controls the achieved coupling coefficient of the transformer. In order to achieve the required effective resistance on the primary and the secondary side, the width of the loop inductors is varied to change the quality factor of the inductors. Additionally, external capacitors are added to achieve the desired resonance frequencies. In this design each inductor value is 220 pH and an external capacitance of 18 fF is added. The coupling coefficient between the loops is 0.19.

The output stage of the transformer is similar in design to other stages except that the output matching network is a high coupling coefficient $2:1$ transformer. A high coupling coefficient structure was used as the output load resistance was low (around $30\,\Omega$) which lowered the quality factor of the match. Additionally, $2:1$ transformers are more lossy than $1:1$ transformer and this further leads to a low quality factor match. Fig. 4.29 shows the output matching network structure.

Fig. 4.30 shows the simulated gain (S_{21}) of the amplifier. The IF amplifier has a gain of 27 dB at the center frequency and an overall bandwidth of 13 GHz. The poles are slightly offset from the maximally flat response to achieve a slightly higher bandwidth.

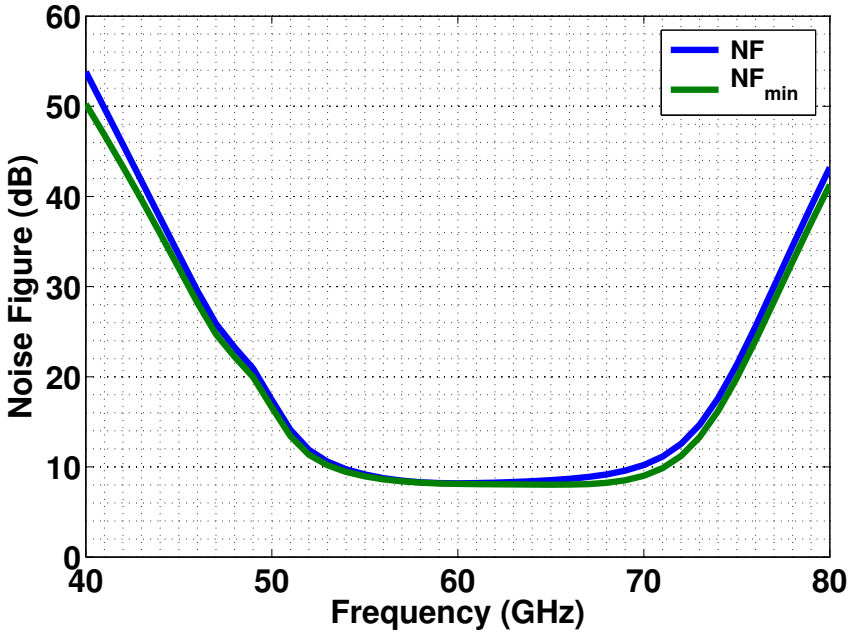


Figure 4.32. Simulated noise figure of the IF amplifier

Fig. 4.31 shows the input match of the IF amplifier. The S_{11} is better than -20 dB at the center frequency and the input match bandwidth is 13 GHz. The simulated and the minimum achievable noise figure of the amplifier is shown in Fig. 4.32. The overlap of the two curves indicates proper match for low noise figure. The minimum noise figure of the IF amplifier is 8 dB. The integrated noise from 40 GHz to 80 GHz is 153.2 μV.

4.5 Other blocks

The circuit blocks described earlier were part of this thesis work. We now briefly describe some of the other blocks.

The antenna consists of two arrays and uses the leaky wave structure. A leaky wave antenna is similar to a transmission line except that its width is one quarter the wavelength of operation. This excites the first higher mode as the radiation mode. As the wave travels through the line, it is radiated into space. The quadrupler uses a push-push circuit with the input being excited at 0°, 90°, 180° and 270° phases of the carrier. Due to the non-linearity of the device, the fourth harmonic signal is produced at the output. The hybrid consists of a capacitively loaded structure with single ended outputs generating the required in-phase and quadrature signals. The tripler consists of a pseudo differential pair with a microstrip hair pin filter at the output. The filter is essential to reject the strong fundamental signal. The demodulator is similar in operation to the quadrupler except that the baseband signal is extracted at the output using a low pass filter i.e. terms of the form $4k\omega_0$ with $k = 0$, where ω_0 is the intermediate frequency. The mixer consists of a double balanced architecture with the RF signal coupled directly at the source. The voltage controlled oscillator on the transmitter and receiver side is an LC architecture with varactor tuning. The pseudo random bit sequence (PRBS) implements a 7-bit pseudo random sequence using a loop unrolled architecture. The PRBS can operate in continuous wave (CW) and on-off keying (OOK) modes.

4.6 Measurement Results

The sub-terahertz transceiver was fabricated in 65 nm bulk CMOS process without any special options. The microphotograph of the chip is shown in Fig. 4.33. The chip occupies a die area of 4 mm × 1.5mm. The supply voltages and the bias signals are provided through DC pads. The required PRBS data clock is supplied using GSG pads. The chip is attached to the FR-4 board using conductive epoxy and all the pads are wire bonded onto it. Two different transceiver chips are mounted vertically using PCI buses onto a regular board and are placed in line of sight for link measurement.

The transmitter EIRP measurement setup is shown in Fig. 4.34. The transmitter output is captured by a WR-3.4 horn antenna and fed into the calorimeter sensor through a WR-3.4 to WR-10 waveguide transition. The measured power from the calorimeter is then noted on the Erickson calorimeter. The transmitter is first turned on and the PRBS is set in continuous wave (CW) mode. The measured EIRP is 5 dBm at 246 GHz.

Fig. 4.35 shows the measured normalized antenna pattern on the H-plane. The antenna pattern matches well with the simulation results except for the extra lobes in one direction. This is suspected to be the measured third harmonic of the 60 GHz blocks which occurs at 180 GHz and is close to the cut-off frequency of the WR-3.4 waveguide.

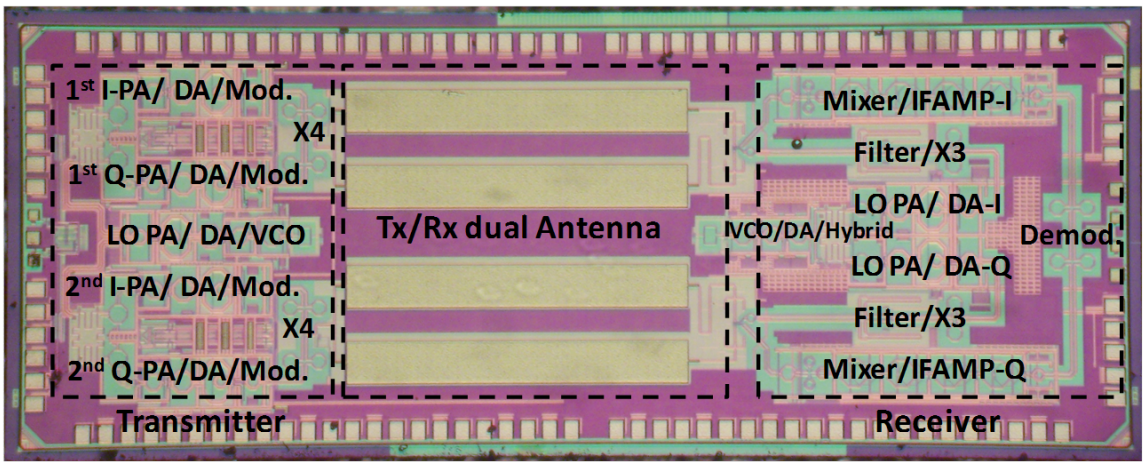


Figure 4.33. Chip microphotograph of the transceiver

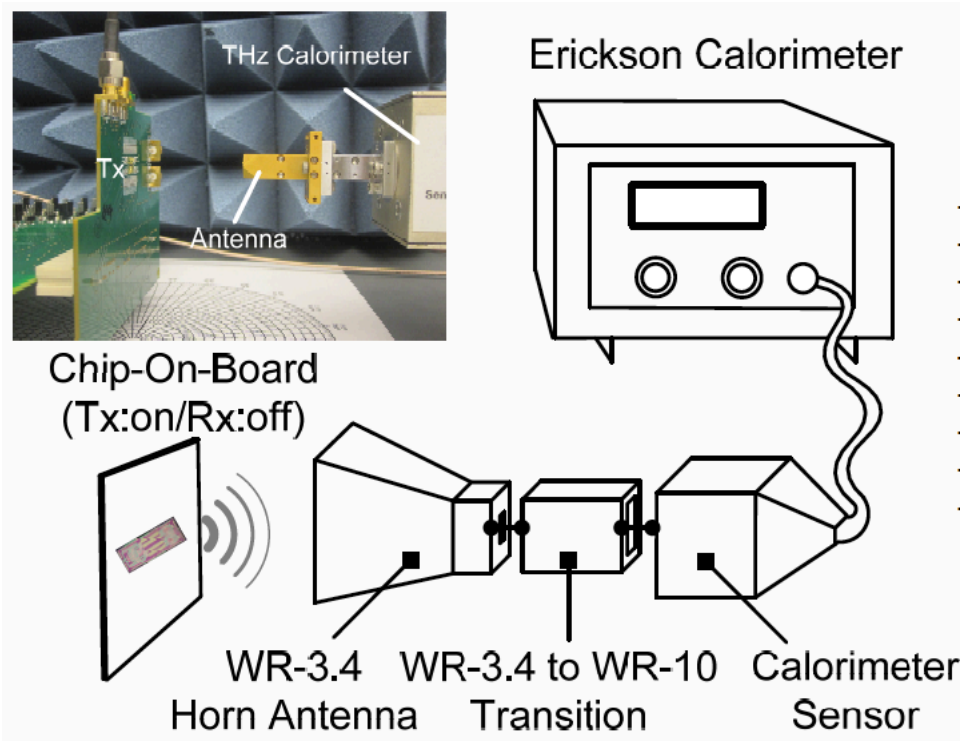


Figure 4.34. Equivalent isotropic equivalent power (EIRP) measurement setup using calorimeter

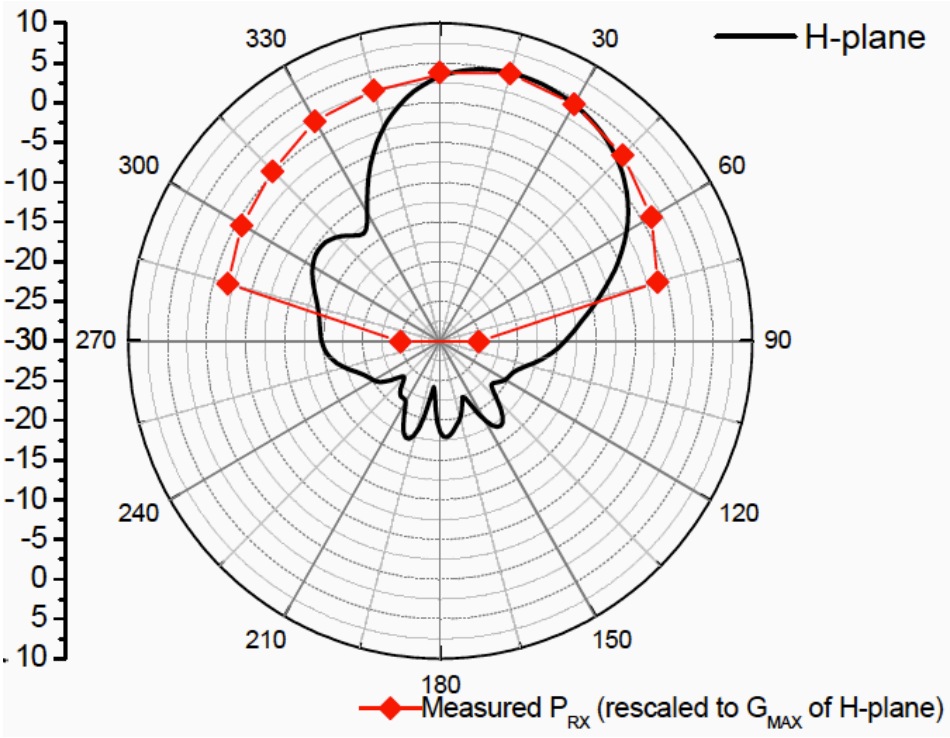


Figure 4.35. Measured and simulated antenna pattern

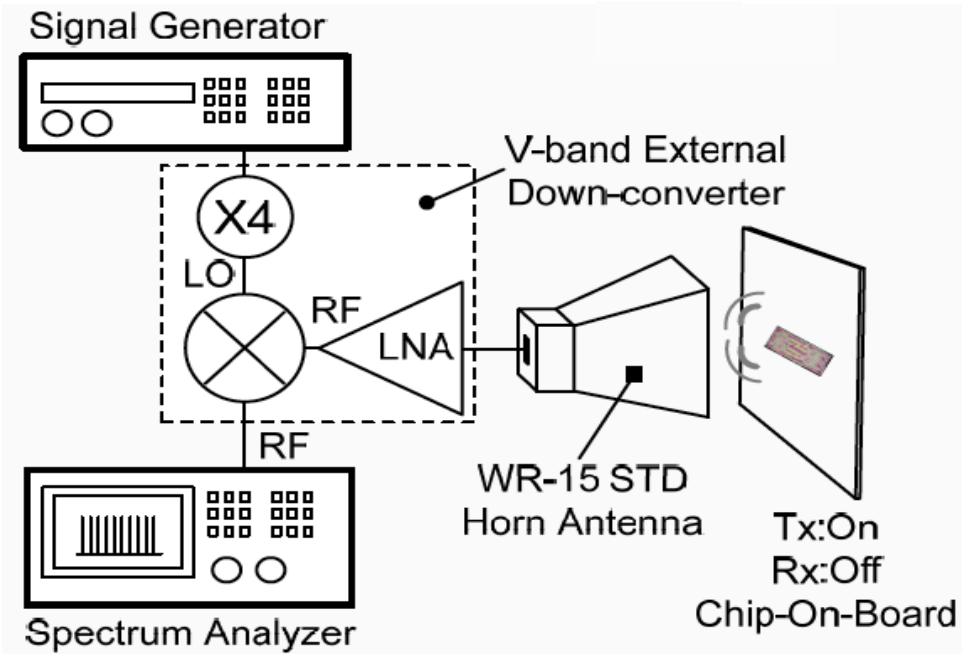


Figure 4.36. Transmitter spectrum measurement setup using an external down-converter

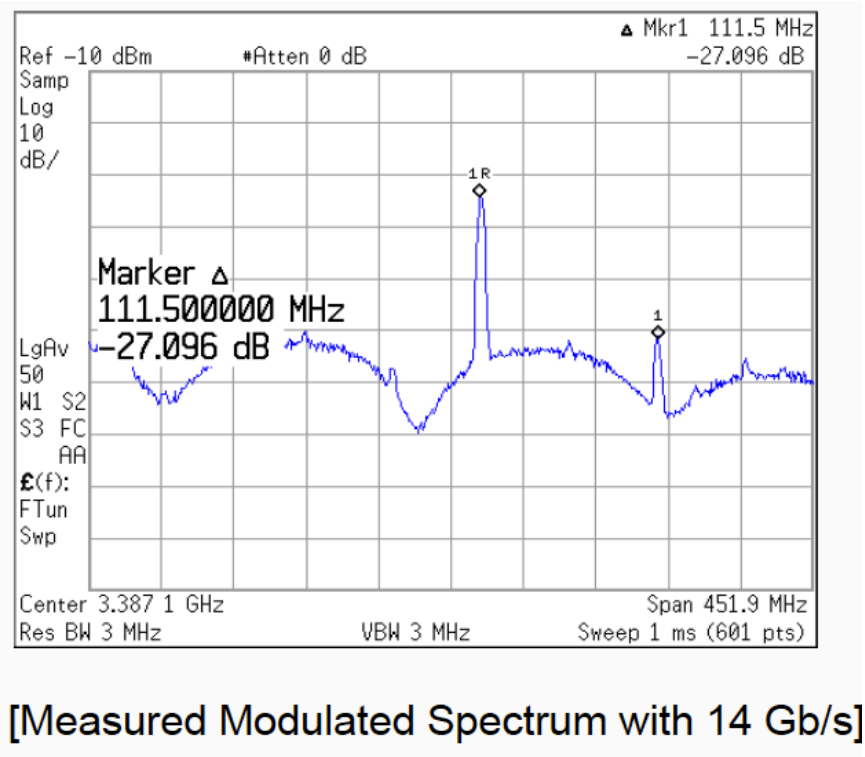


Figure 4.37. Down-converted transmitter spectrum for 14 Gbps data

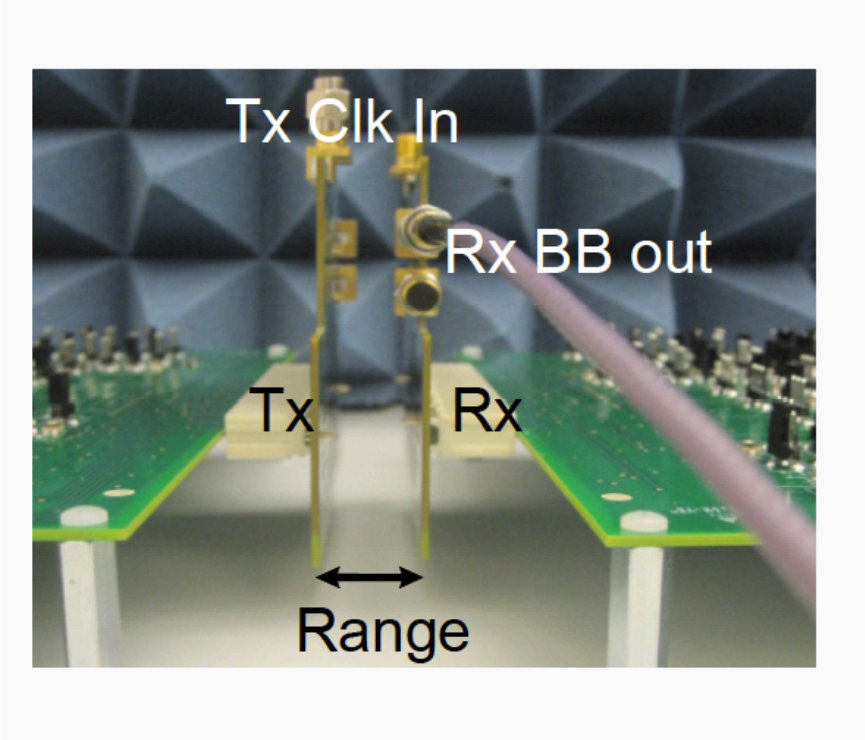


Figure 4.38. Link measurement setup

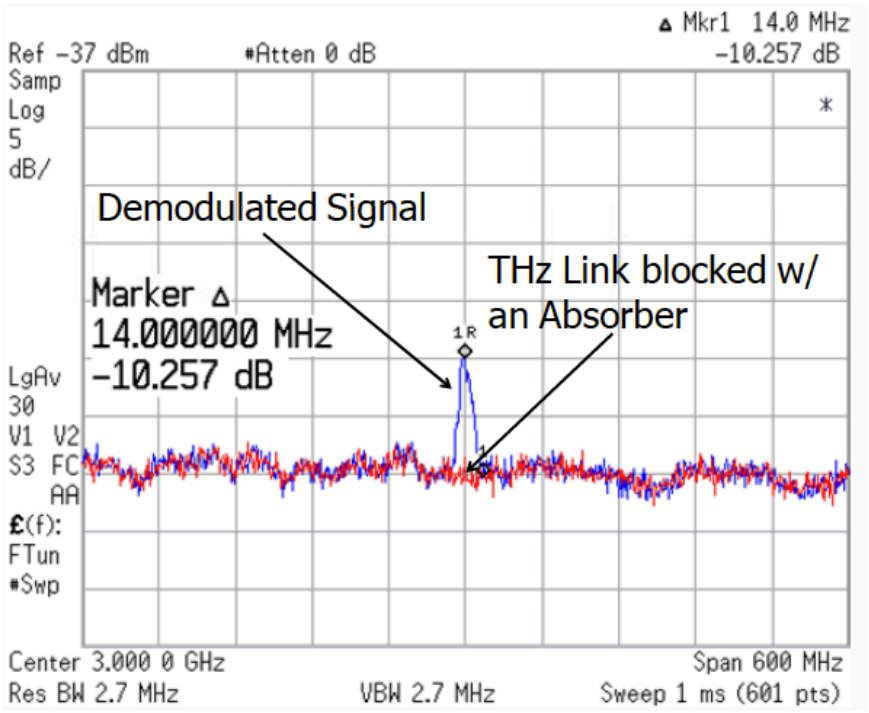


Figure 4.39. Link measurement for a continuous wave (CW) signal with and without absorber

The transmitter setup for the spectrum measurement is shown in Fig. 4.36. It consists of a WR-15 horn antenna whose output it fed to a V-band LNA. The LNA output is then down-converted using an external mixer to baseband. This setup measures the leakage modulated spectrum around the 60 GHz band which is essentially up-converted to the sub-terahertz frequency by the quadrupler.

Fig. 4.38 shows the measured down-converted spectrum for 14 Gbps data. The beat frequency of 111.5 MHz matches well with the theoretical PRBS repetition rate of 110.24 MHz indicating operation of the modulator block and the subsequent amplification stages.

The link measurement setup in shown in Fig. 4.38. Here the two chips are placed vertically in line of sight for link measurement. A continuous wave (CW) tone is generated and captured by the receiver as shown in Fig. 4.39. With an absorber, the link is cut-off and no signal is received by the receiver. Up to 10 Gbps of toggling data has been verified in CW mode.

4.7 Conclusion

In this chapter, we discussed the design of a 260 GHz OOK wireless transceiver for chip-to-chip communication. The transceiver employs a 260 GHz carrier and a 60 GHz intermediate frequency (IF) stage to perform the OOK modulation. The transmit EIRP was measured to be 5 dBm. The power consumption is 1.173 W. The receiver comprises of a mixer first

architecture with a simulated gain of 17 dB and a noise figure of 19 dB. The wireless link comprising of the transmitter and receiver works in continuous wave (CW) mode with a toggling signal at 10 Gbps. Due to the coupling of the LO signal to the demodulator (through the substrate) and the implementation of a non-coherent scheme, tones within the data bandwidth are observed at the beat frequency between the oscillators. This distorts the received waveform and prevents eye diagram and spectrum measurement of modulated data.

Chapter 5

A 240 GHz QPSK Wireless Transceiver in 65 nm CMOS - Part I

In this chapter, we discuss the design of a sub-terahertz transceiver using complex modulation schemes. As discussed in Chapter 3, communication in the terahertz regime involves numerous challenges both in the system and block level design. The previous design discussed in Chapter 4 served as a prototype to verify the modeling strategies and the feasibility of sub-terahertz transceivers in CMOS technology. The design employed a simplified modulation technique (On-Off Keying or OOK) and multiple antennas for beam-forming. However, due to the choice of the architecture and lower data rate, the energy efficiency of the design was $\approx 120\,\text{pJ/bit}$. In order for the design to be competitive with wired links, the efficiency metric (pJ/bit) must be comparable or at least be only a magnitude of order higher. In this design, we strive to achieve this target by employing a new architecture and a complex QPSK modulation scheme.

5.1 Transmitter Architecture

The block diagram of the transmitter is shown in Fig. 5.1. The transmitter [44] employs an 80 GHz local oscillator (LO) frequency generated using an on-chip injection-locked oscillator (IL-VCO). The required in-phase (I) and quadrature (Q) signals at 80 GHz are generated from the 80 GHz LO signal using a differential hybrid. Using a differential hybrid allows one to maintain the balance of the circuit and avoids the usage of lossy baluns which are required in conventional hybrid designs. In order to minimize the mismatch between the I and Q signal, the differential hybrid is implemented as the last stage in the LO chain. The baseband I and Q data are generated using an on-chip PRBS circuity $(2^7 - 1)$. A QPSK

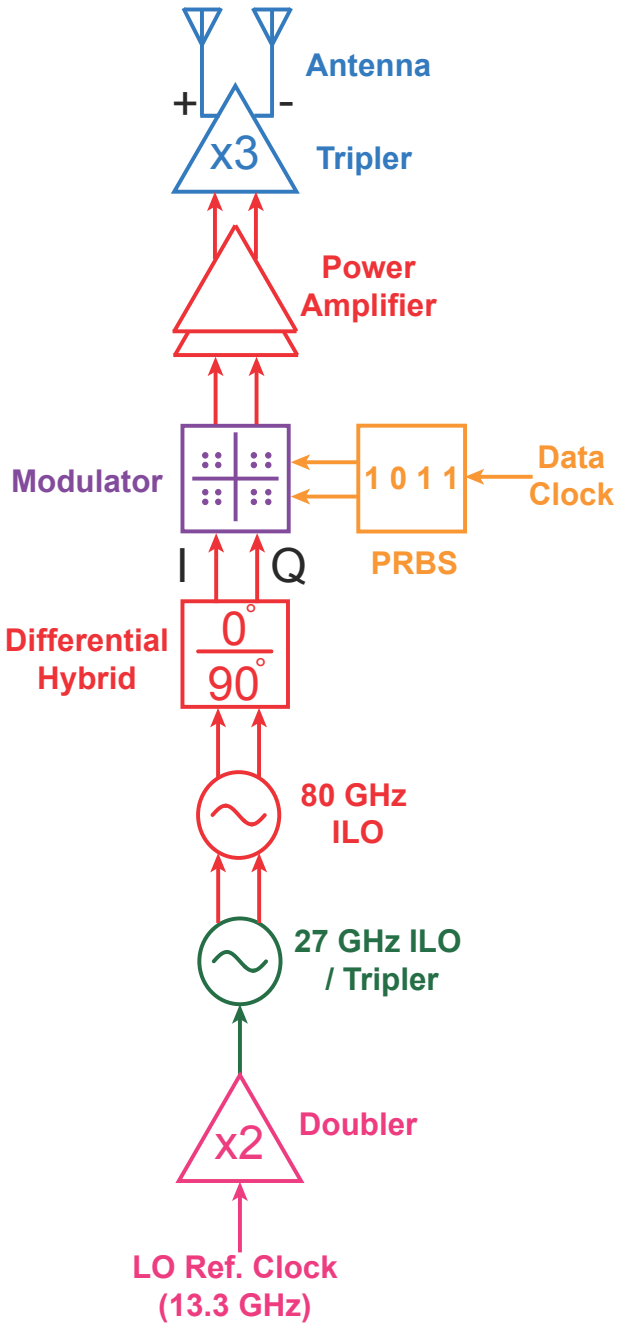


Figure 5.1. Transmitter architecture

modulator then modulates this data onto the 80 GHz carrier using the generated 80 GHz I/Q LO signals. The modulated signal at 80 GHz is then amplified using a four-stage power amplifier (3-stage Class A drivers and a Class-E output stage) to an output power level of 13 dBm. A 240 GHz tripler then generates the required sub-terahertz carrier by frequency multiplying the 80 GHz modulated QPSK waveform (as the carrier frequency is greater than f_{max} of the technology). Due to phase rotation of the tripler, each I/Q constellation point

is rotated but the entire constellation maintains its phase quadrature. The 240 GHz tripler drives the differential on-chip slotted loop antennas to radiate the sub-terahertz frequency into air. In order to detect the coherent modulation scheme, an external reference clock at 13.3 GHz is used. This reference clock is multiplied using an on-chip doubler and is employed to injection lock a 27 GHz IL-VCO. The output from the 27 GHz IL-VCO is tripled using a tripler whose output is coupled to the 80 GHz IL-VCO. In this manner, the LO frequency on the transmitter and the receiver are locked to an external reference at 13.3 GHz.

5.2 Receiver Architecture

The block diagram of the receiver [45] is shown in Fig. 5.2. The transmitted 240 GHz signal is received using an antenna structure similar to the transmitter. Each channel (I or Q) uses a separate slotted loop antenna to achieve better isolation. As the operation frequency is greater than the f_{max} of the technology, a front-end low noise amplifier (LNA) is not feasible in this design. Hence, the receiver employs a direct conversion mixer first architecture. A voltage mode differential passive mixer down-converts the received signal directly to baseband. The differential RF signals for the I/Q mixers are generated from the antenna using a coplanar waveguide (CPW) to a coplanar stripline (CPS) transition as described later. The baseband output is then amplified using high gain, wide bandwidth, low noise IF amplifiers to obtain the demodulated data. As the mixer is passive and has no gain, the noise of the baseband amplifiers contributes significantly to the overall noise figure of the receiver. Hence, a reasonable amount of power is spent in the first stage of the baseband amplifier to obtain an overall low noise figure for the receiver. The required 240 GHz LO frequency is generated in a manner similar to the transmitter. Compared to the transmitter, the LO chain does not utilize any modulator and operates at a single frequency. The required 240 GHz I/Q LO signals are generated using delay line structures. The in-phase and quadrature generation is performed at the last stage of the LO chain to minimize any mismatch between the two channels.

5.3 Antenna Design

In this section, we discuss the design of the antenna used in the transmitter and the receiver. The size of the antenna is inversely proportional to the frequency of operation. Therefore, the operation at sub-terahertz frequencies allows one to integrate the antennas onto the silicon die thereby alleviating packaging costs. There are various antennas popular in literature with the dipole, the loop and the patch antennas being the common ones. Antennas such as the traveling wave, the helical and yagi-uda array are broadband in nature. However, the die area occupied by them is significantly large and in some cases they aren't feasible for implementation in the planar integrated circuit process.

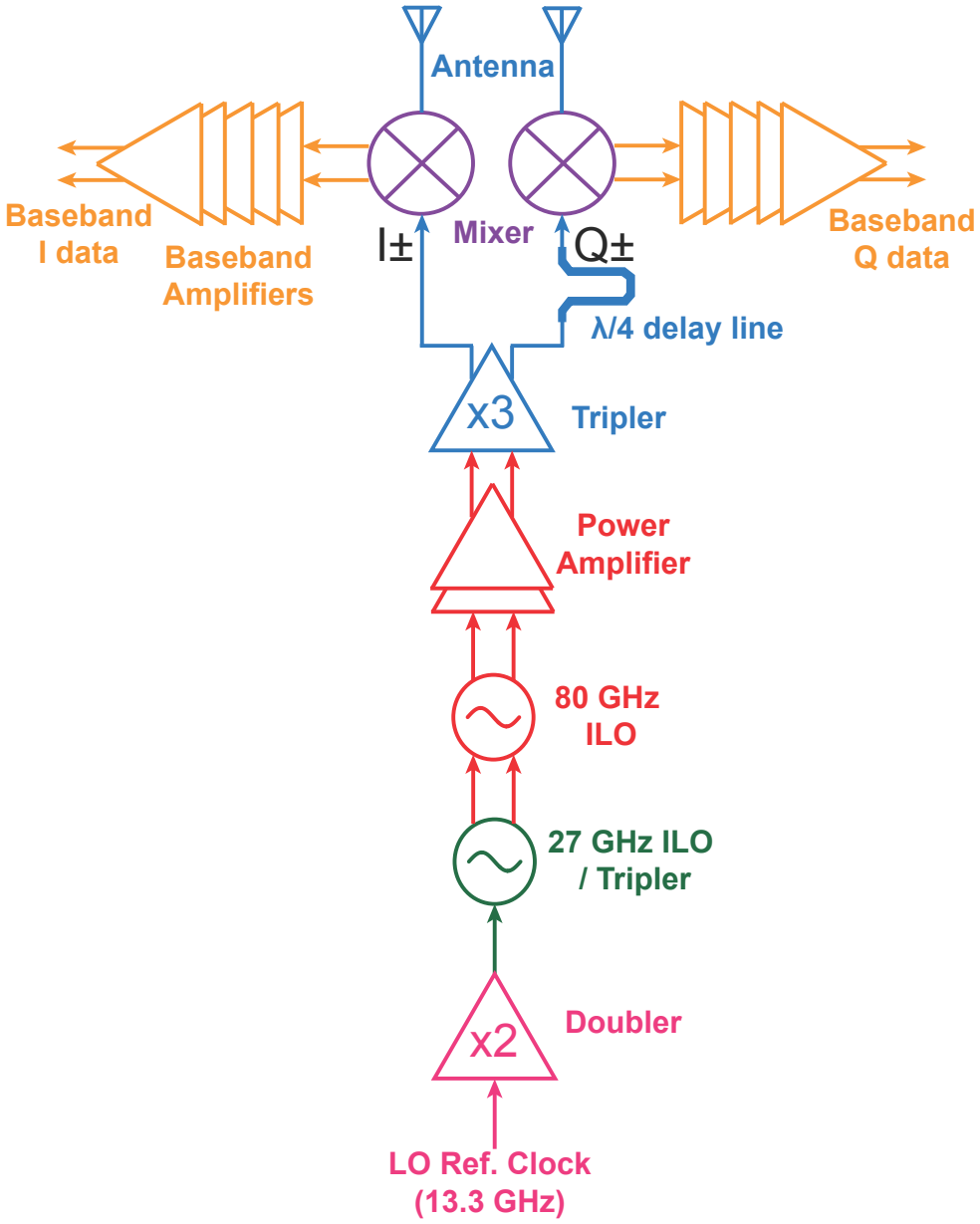


Figure 5.2. Receiver architecture

In order to analyze these antennas, we first calculate the vector potential $\mathbf{A}$ from the electrical current density. For electrical structures that can be quantified by current densities per unit length (like a dipole or a loop antenna), the vector potential is given as

$$\mathbf{A} = \frac{\mu}{4\pi} \int_C I_C(x, y, z) \frac{\exp(-jkR)}{R} dl \tag{5.1}$$

where C is the curve defined on the structure, I_C the current density per unit element, R the distance at which the potential is calculated, dl the unit element on the structure and

$k^2 = \omega^2\mu\epsilon$. Here, ω is the frequency of operation, μ the permeability of the medium and ϵ the permittivity.

For a structure with surface current J_S or volume current J_V, the vector potential is calculated as

$$\mathbf{A} = \frac{\mu}{4\pi}\iint_S J_S(x,y,z)\frac{\exp(-jkR)}{R}dS \tag{5.2}$$

$$\mathbf{A} = \frac{\mu}{4\pi}\iiint_V J_V(x,y,z)\frac{\exp(-jkR)}{R}dV \tag{5.3}$$

Once the vector potential is known, the electrical field $\mathbf{E}$ and magnetic field $\mathbf{H}$ can be calculated as

$$\mathbf{E} = -j\omega\mathbf{A} - \frac{j}{\omega\mu\epsilon}\nabla(\nabla.\mathbf{A}) \tag{5.4}$$

$$\mathbf{H} = \frac{1}{\mu}(\nabla \times \mathbf{A}) \tag{5.5}$$

Once the $\mathbf{E}$ and the $\mathbf{H}$ fields are known, the Poynting vector can be calculated and hence the antenna pattern can be found by assuming a far field region where $kR \gg 1$ and higher order terms of $1/R^n$ are neglected. In this design, the dipole, patch and loop antennas were considered as they occupy a lesser die area. Using the above equations, we can show that the dipole antenna with a length equal to half the wavelength of operation has a peak directivity of 2.156 dB. The typical bandwidths of the dipole antenna is 8 % of the center frequency. A similar procedure can be used for the loop antenna and a loop with a circumference equal to the wavelength (corresponding to the frequency of operation) has a directivity of 3.27 dB. The achievable bandwidth of typical loop antennas is 10-12 %. For the patch antenna, a cavity model [46] analysis is required to obtain its radiation pattern. For feed widths much lesser than the wavelength of operation, the directivity of a patch can be shown to be equal to 5.2 dB. However, typical bandwidths are only 3 %. In this design, the loop antenna was considered due to its smaller edge length (compared to dipole) which allows easy layout of the structure while using arrays. Additionally, the bandwidth attainable from a loop antenna makes it a better choice while comparing it with the patch antenna.

5.3.1 Transmitter Antenna Structure

Standard integrated circuit (IC) processes have stringent requirements and require designs to support metal density rules for chemical mechanical polishing (CMP) of wafers. To conform to these rules, a slotted loop antenna has been used in this design. Using Babinet's principle [46], a slotted loop antenna has the same radiation pattern as that of a loop antenna except that the fields are dual of each other or the electrical field is replaced by the magnetic field and vice versa. Fig. 5.3 shows an array of two slotted loop antennas used for beam-forming. If the feed points of the antenna are assumed to be at the same location and they are fed using signals of the same phase, the electrical field adds up constructively in

space for an appropriate diameter and spacing (usually $\lambda/2$). The feed points to the antenna are driven using the tripler whose outputs are differential. This would require a delay line of half the wavelength to drive the feed points in the same phase. Not only would the line be lossy, it would also make the structure asymmetric and the asymmetric would affect the antenna pattern. To make the structure symmetric, we observe the following. If the loop circumference is adjusted to one wavelength, then the feed point can be shifted spatially by half the wavelength as shown. The feed points can then be excited by anti-phase signals to attain beam-forming. Hence, in this design the feed point was shifted and the diameter and spacing of the loop were optimized to maximize the gain under anti-phase excitement.

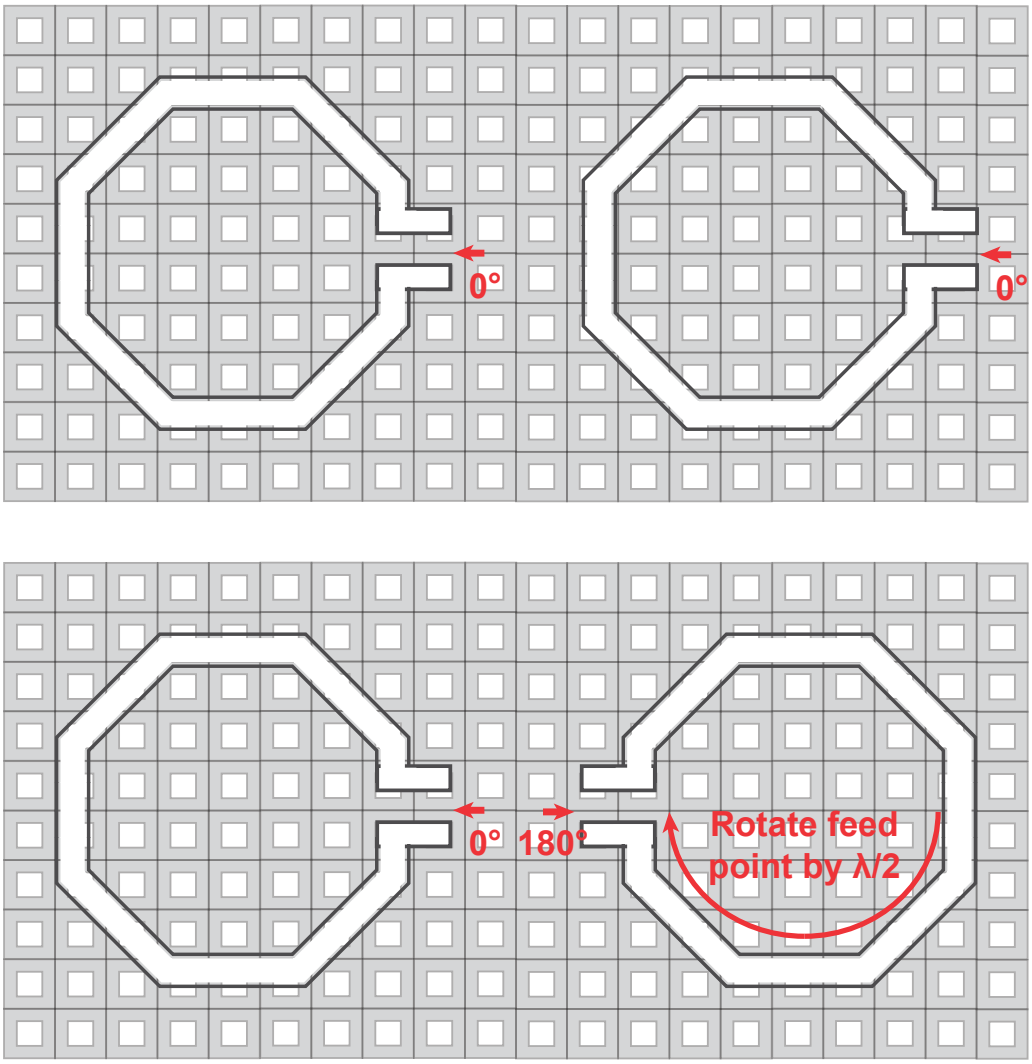


Figure 5.3. Beam forming with feed point rotation and input phase shift for a slotted loop antenna array

Fig. 5.4 shows the layout structure of the transmitter antenna. It consists of two slotted loop antennas driven differentially at feed points spatially separated by half the wavelength resulting in beam forming. As most of the radiation from the antenna is coupled into

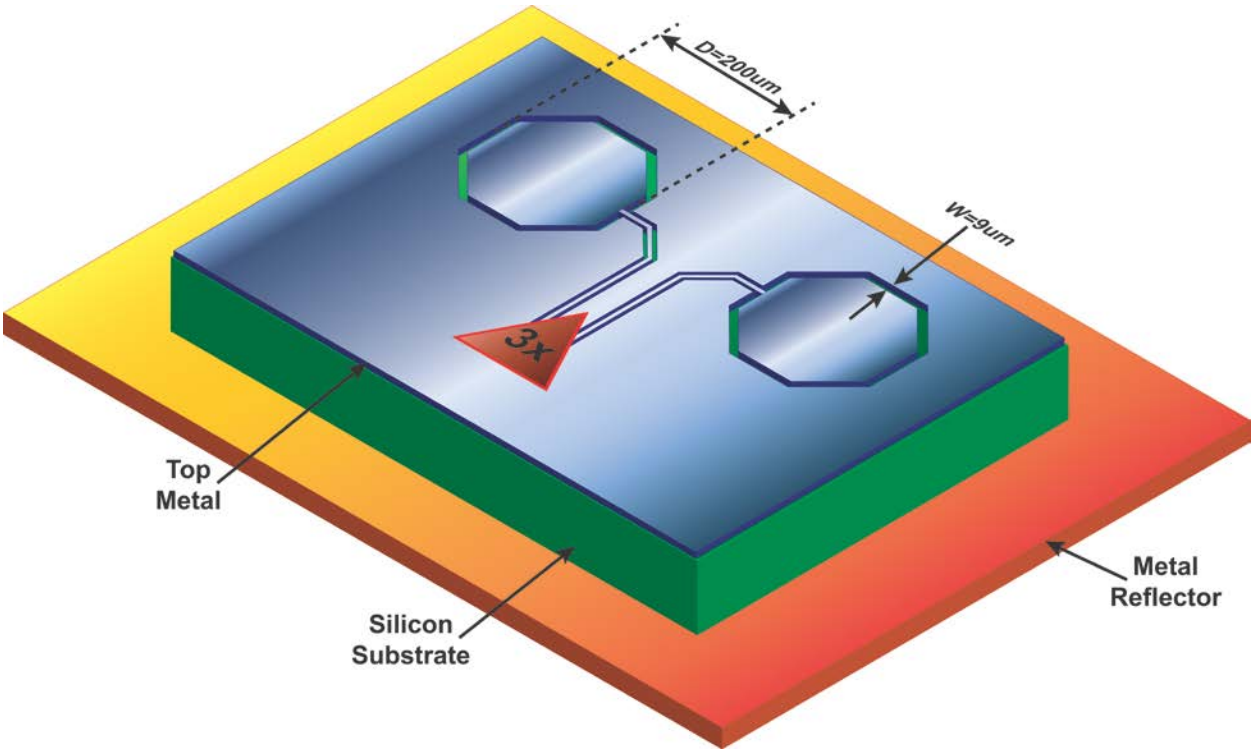


Figure 5.4. Structure of transmitter slotted loop antenna

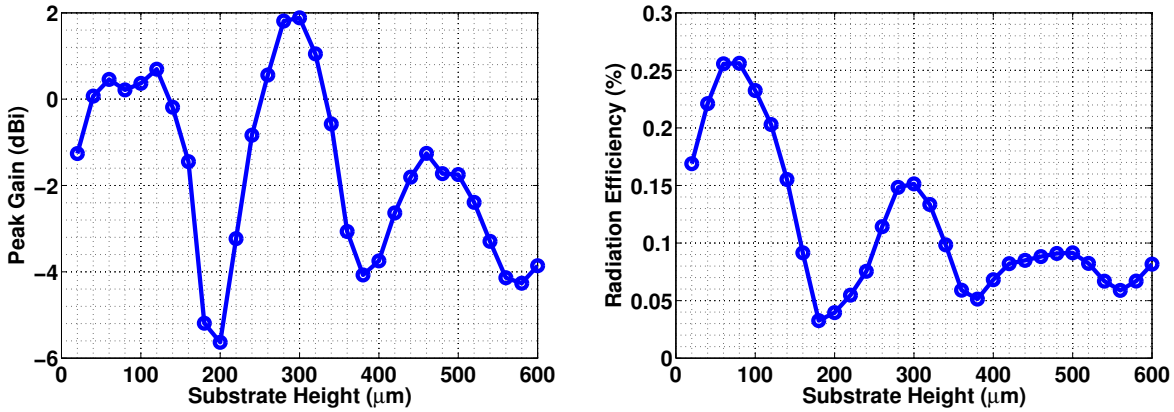


Figure 5.5. Simulated peak gain [left] and radiation efficiency [right] as a function of the substrate height

the substrate (in the ratio $\epsilon^{1.5}$: 1) [47], a broadside pattern cannot be achieved and the radiation pattern has multiple lobes. Therefore, a copper metal reflector is used between the silicon substrate and the FR-4 printed circuit board interface. This metal reflector creates an image antenna whose fields add up constructively or destructively (depending on the substrate height) to yield a broadside radiation pattern. The antenna is interfaced to the 240 GHz tripler using coplanar waveguide (CPW) lines as shown.

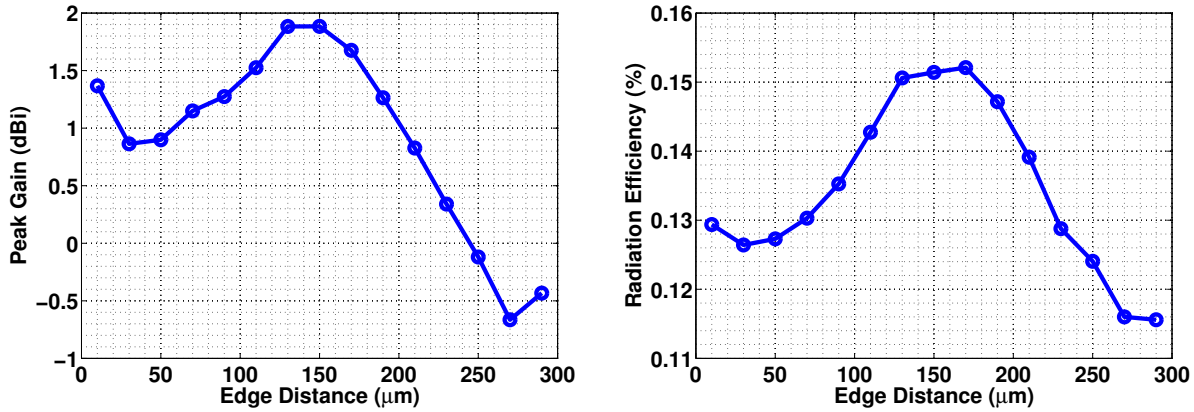


Figure 5.6. Simulated peak gain [left] and radiation efficiency [right] as a function of the edge distance

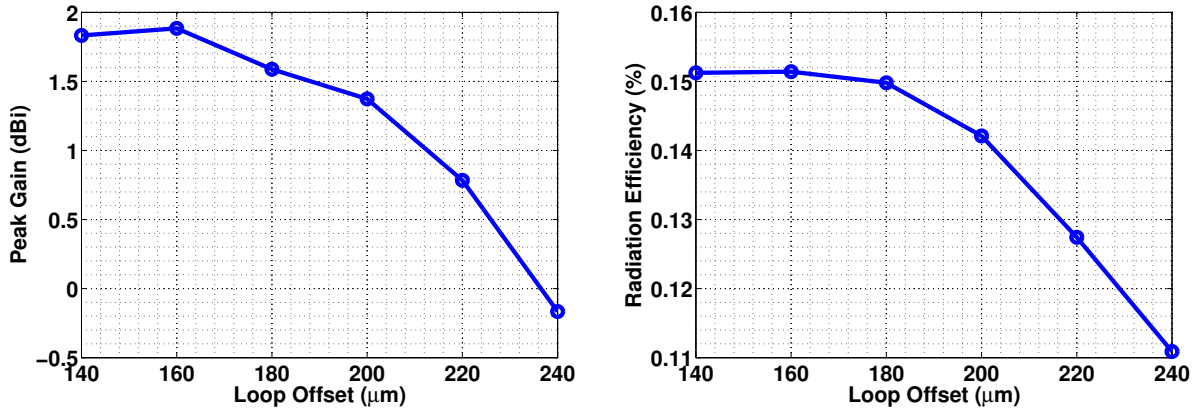


Figure 5.7. Simulated peak gain [left] and radiation efficiency [right] as a function of the loop offset from the center of symmetry

The antenna is optimized for performance by finding the optimal design parameters namely the loop diameter, the loop width, the substrate dimensions, the offset between the loops and the optimal placement of the structure on the substrate. As described earlier, due to the use of the copper reflector, an image antenna is created and this helps one to achieve a broadside radiation pattern. To find the optimal substrate height, the peak gain and radiation efficiency of the antenna are varied as a function of the substrate height. Fig. 5.5 shows the simulation results. The antenna achieves a peak gain at 300 μm which is the default substrate thickness. The radiation efficiency however peaks at 100 μm. As the distance of the ground plane is increased (with increase in substrate height), there is an optimum point at which the directivity of the antenna is increased. However, as the propagation distance through the silicon substrate is increased, the radiation efficiency reduces. One must note that the optimal substrate height is a function of the lateral dimensions of the substrate which affects the surface wave propagation in the medium and hence the optimum height need not be the theoretical value of half the wavelength.

The antenna is also optimized with regard to the substrate dimensions. The lateral dimensions of the substrate are constrained due to area requirements. However, given a loop diameter, it is optimal to use smaller substrate dimensions as this allows standing wave patterns to be formed in the substrate [48][49]. Using a larger substrate results in outward propagation of the energy as surface waves and results in a lower efficiency. Hence, the three edges of the substrate need to be placed at an optimal point from the antenna. In accordance with this theory, the loop antenna had to placed at an optimal distance from the edge of the substrate. Fig. 5.6 shows the simulated peak gain and radiation efficiency as a function of the edge distance. As expected, there is an optimal point and this happens at 150 μm. To optimize the loop positions in the lateral dimensions, the loop offset from the center of symmetry of the structure was varied. The optimal distance between the center of the loops is 320 μm. The final substrate dimensions were 2 mm $\times$ 1 mm.

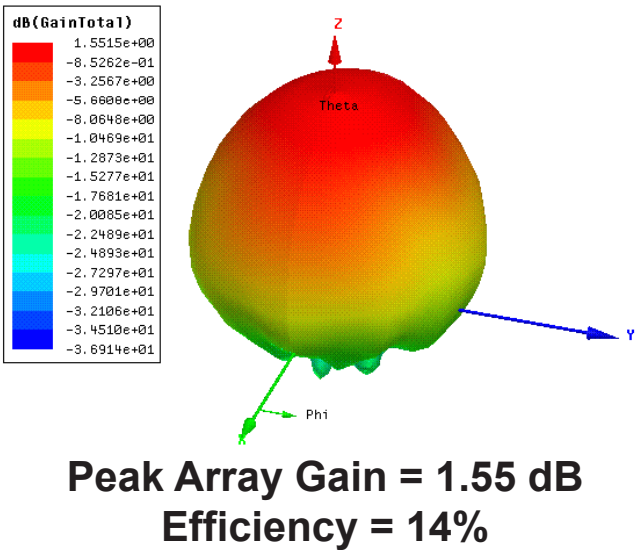


Figure 5.8. Simulated gain pattern of the transmitter antenna

The slotted loop antenna array was designed using the above optimization process. The final structure has a loop diameter of 200 μm and a slot width of 9 μm. Fig. 5.8 shows the simulated antenna pattern. The achieved array gain is 1.55 dBi with an efficiency of 14 %. Fig. 5.9 shows the input reflection coefficient of the transmitter antenna. The S_{11} is less than -10 dB from 220 GHz to 250 GHz. Thus the bandwidth of the antenna is 30 GHz.

5.3.2 Receiver Antenna Structure

The structure of the receiver antenna is similar to that of the transmitter and consists of two slotted loop antennas as shown in Fig. 5.10. The in-phase (I) and quadrature (Q) channels each use a single antenna. The antennas are interfaced to the mixer using CPW lines as in the case of the transmitter. However, as the mixer is a fully balanced structure,

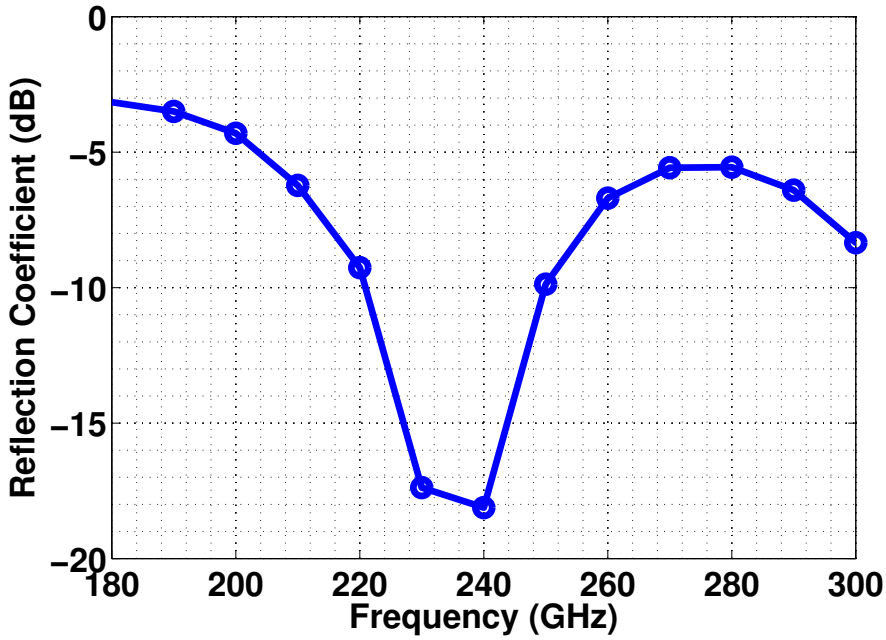


Figure 5.9. Simulated input reflection coefficient (S_{11}) of the transmitter antenna

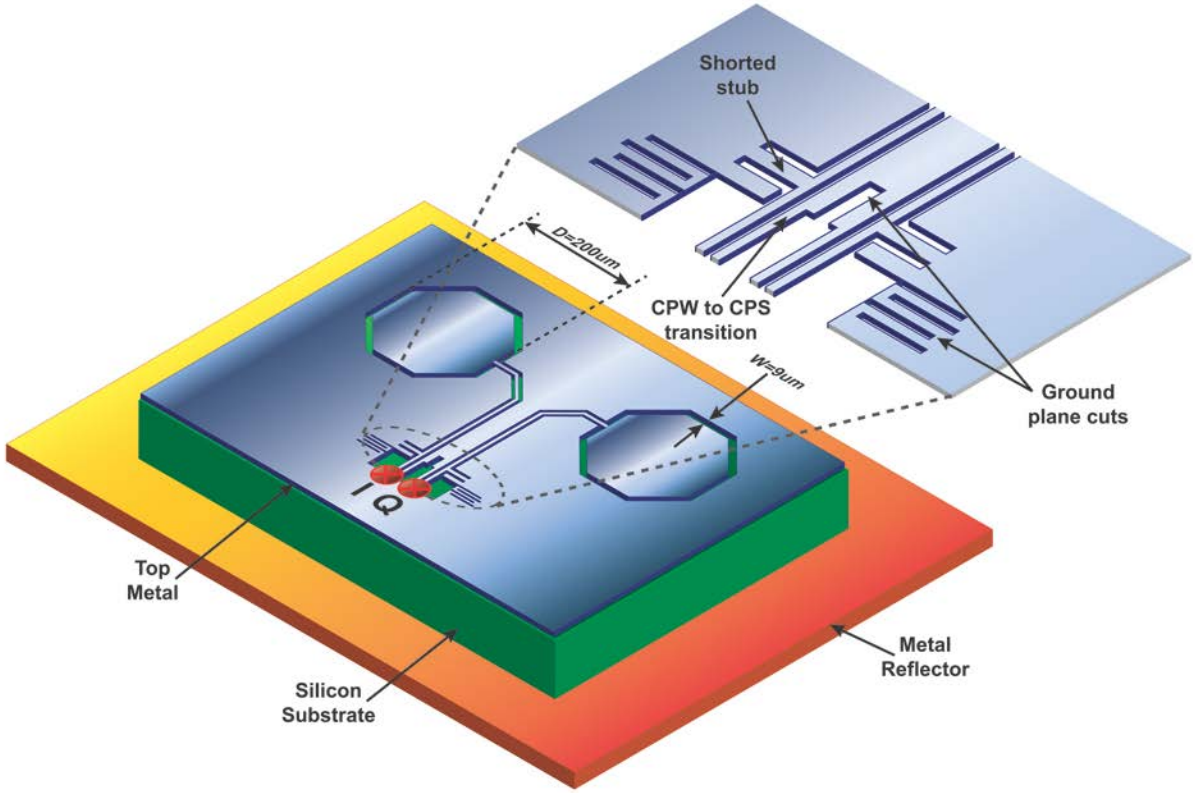


Figure 5.10. Structure of the receiver slotted loop antenna

it needs to be driven using fully differential RF signals. To generate the required differential signals from the CPW lines, a CPW to coplanar stripline (CPS) transition is made. In order to efficiently convert the CPW mode to the odd mode of the CPS (which is the desired mode), the common mode impedance of the CPS lines needs to be increased in comparison to the differential mode impedance. To achieve this, multiple cuts are introduced in the ground plane. Serpentine ground plane cuts are also introduced along the periphery of the ground plane to increase the return path length thereby increasing the common mode inductance. Therefore, a 10° line is sufficient to generate the required differential signals. For the proper operation of the mixer, the RF or the IF port must also be grounded for DC purposes. In this case, the RF port is biased to the ground node. One of the signals of the CPS line is already grounded as it is the ground node of the CPW line. To ground the other signal trace, a shorted stub is used that simultaneously achieves both impedance match and DC biasing.

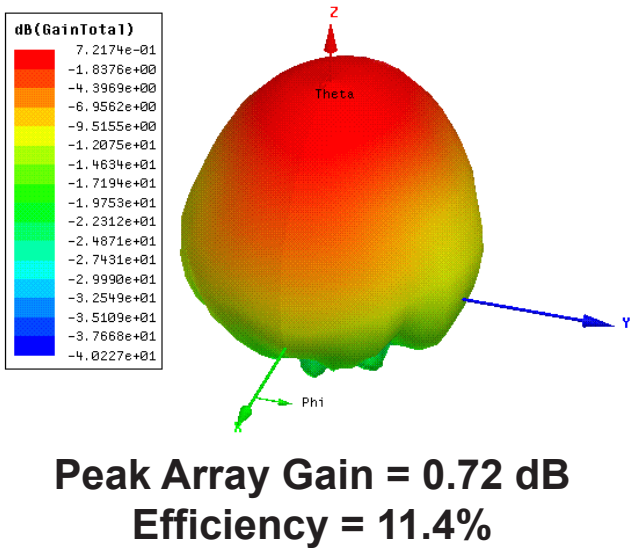


Figure 5.11. Simulated gain pattern of the receiver antenna

Fig. 5.11 shows the simulated antenna pattern. The achieved array gain is 0.72 dBi with an efficiency of 11.4 %. Fig. 5.12 shows the input reflection coefficient of the receiver antenna. The S_{11} is less than −10 dB from 210 GHz to 250 GHz.

5.3.3 Transmitter/Receiver Combined Link

The complete link comprising of the transmitter and receiver was simulated in HFSS for link length of 1 cm. Fig. 5.13 shows the simulation result of the antenna mixer interface. The plot shows the differential and common mode output of the RF ports of the fully balanced mixer. Due to the efficient mode conversion and careful layout of the ground plane, the common mode component is only 5 % or −26 dB below the differential signal.

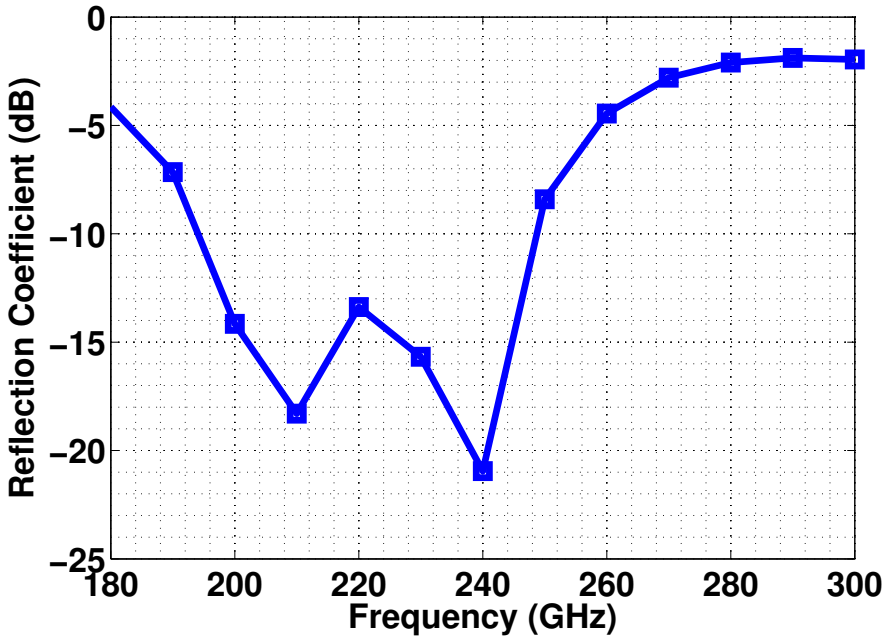


Figure 5.12. Simulated input reflection coefficient (S_{11}) of the receiver antenna

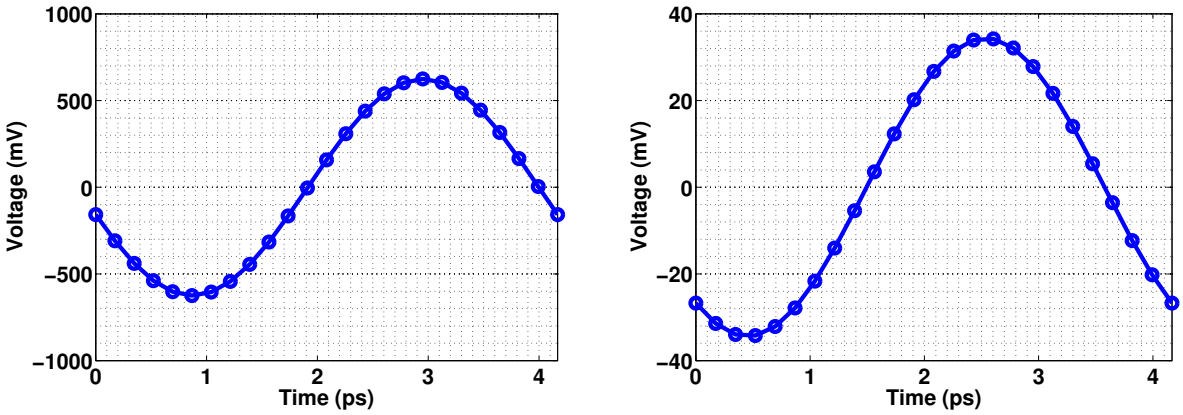


Figure 5.13. Antenna-mixer interface - Simulated differential signal [left] and common mode signal [right] at the mixer RF ports

Fig. 5.14 shows the simulated gain from the transmitter to both the channels of the receiver. For a 1 cm link, the path loss at this frequency is −40 dB. Including the antenna gain of 1.55 dB on the transmitter and −2.3 dB on the receiver (not used as an array), the gain is calculated to be around −42 dB at 240 GHz, which is close to the simulated value. This confirms the Friis equation assumption. The isolation between the receiver antennas is also plotted as a function of the frequency. The antennas have an isolation of −30 dB at 240 GHz. If some of the LO signal potentially leaks from the I channel to the Q, as they are generated from the same source, they appear as DC at IF. As the IF outputs are capacitively

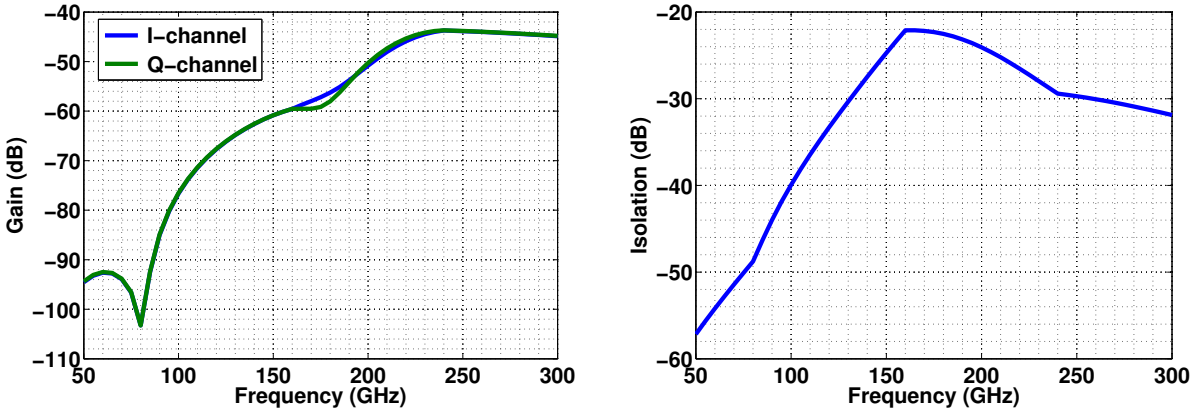


Figure 5.14. Antenna-mixer interface - Simulated gain from Tx to Rx [left] and isolation [right] between the Rx antennas

coupled, this is not an issue. The coupling of the I and Q modulated data isn't of much concern as their output magnitudes are low and the 30 dB isolation between the antennas further reduces their effect.

5.4 LO Architecture

As discussed in the previous section, the modulation is performed at 80 GHz carrier frequency and then up-converted to 240 GHz using a tripler. In order to modulate the signal at 80 GHz, we need to generate the required 80 GHz LO signal and the in-phase(I) and quadrature(Q) components.

5.4.1 Comparison of various architectures for 80 GHz LO generation

The generation of the 80 GHz I/Q local oscillator (LO) signal for modulation can be performed in several ways. Fig. 5.15 indicates several possible architectures to achieve the same. In order to make a fair comparison between the topologies, the output power is assumed to be the same and is a total of 0 dBm or -3 dBm per channel. Some of these architectures utilize phased-locked loops (PLLs) to generate the 80 GHz carrier or a sub-harmonic frequency. To estimate the required power consumption for these architectures, Fig. 5.16 shows the power consumption of various PLLs published in literature for different frequencies [13][14][50–57].

In Architecture I, a PLL is designed at 80 GHz and is followed by a passive hybrid to generate the required I and Q signals. From Fig. 5.16, a PLL at 80 GHz requires around

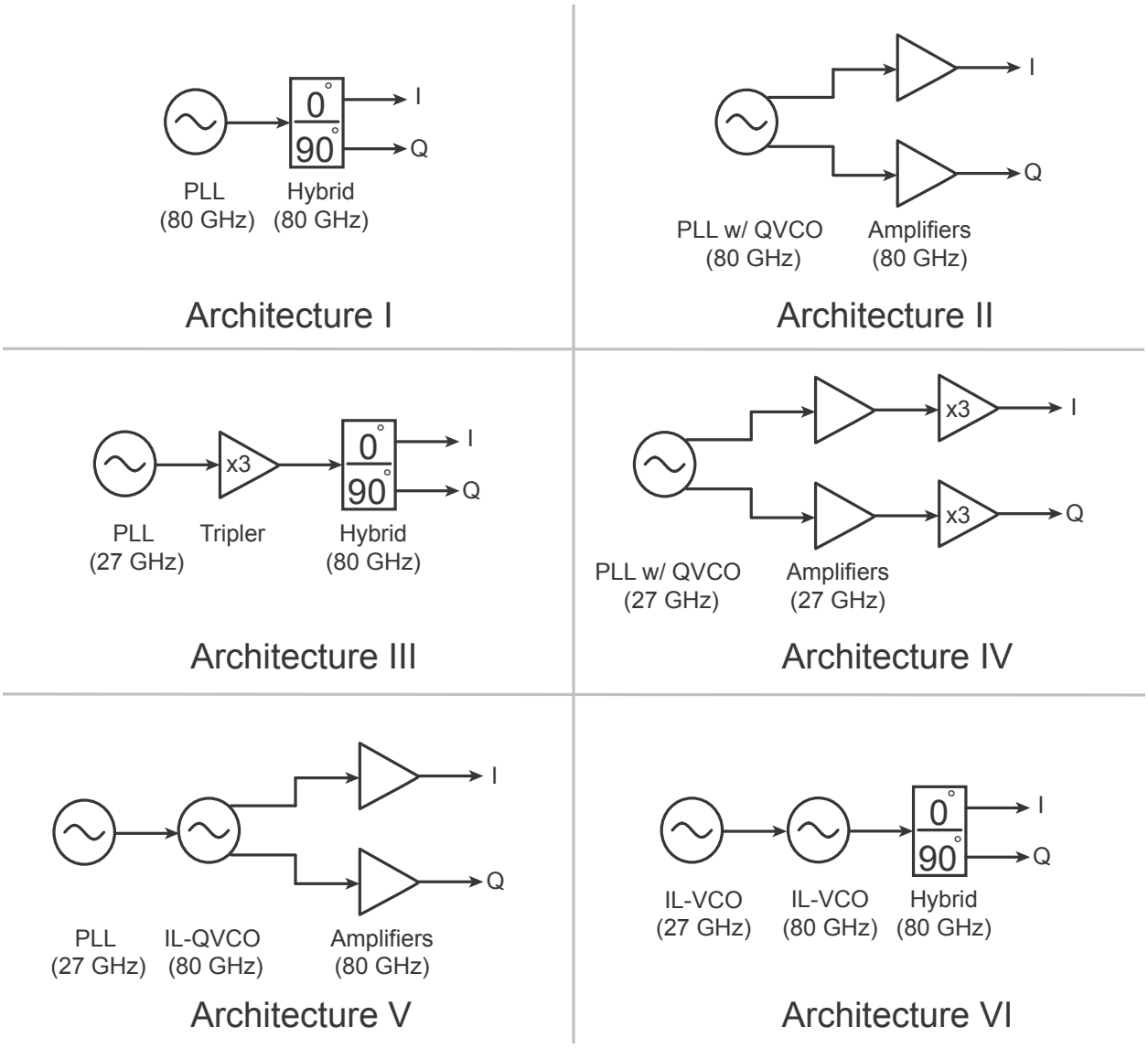


Figure 5.15. Choice of different architectures to generate the 80 GHz LO signals

60 mW to generate 1 dBm of output power. Assuming a 1 dB loss for the passive hybrid, this topology yields the required power level. This architecture has a very low I/Q phase error as the hybrid is at the end of the LO chain. However, the required reference clock frequency for the PLL needs to be relatively high and this suffers from the attenuation through the bond wire of the package. Increasing the reference clock power to offset this attenuation could lead to unwanted leakage through the PCB or from the transmitter to the receiver board. Additionally, in the case of a PLL startup failure, an 80 GHz LO signal cannot be easily fed externally as this required the use of probes. In Architecture II, a PLL is designed with a Quadrature VCO (QVCO) in the loop. This VCO generates the required I and Q signals which are then amplified to deliver the required power levels. This topology has the same merits and demerits of Architecture I and consumes about 60 mW for a −3 dBm output

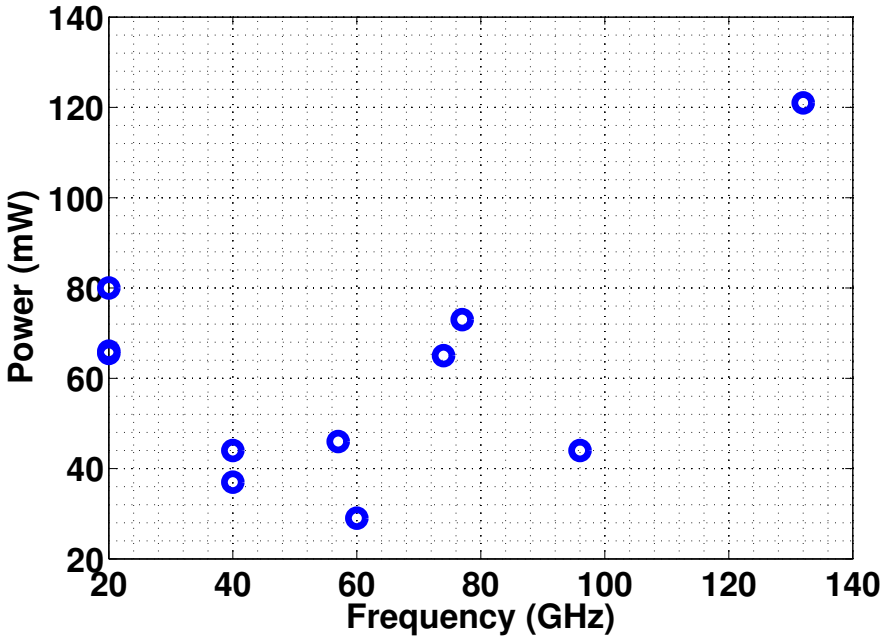


Figure 5.16. Power consumption as a function of operating frequency for published PLL designs in literature

power per channel. However, QVCO's depend on injection locking between two oscillators and weren't considered from a reliability standpoint of the design. In Architecture III, a PLL is designed at 27 GHz followed by a non-linear amplifier which generates the 80 GHz LO signal. This 80 GHz LO signal is then passed through a passive hybrid to generate the required I and Q signals. From the trend in Fig. 5.16, a PLL at 27 GHz can be designed consuming 30 mW of power for an output power of 1 dBm. Additional buffers are required to boost the signal to 4 dBm and require 10 mW of DC power assuming an efficiency of 30%. With a tripler loss of 3 dB and a power consumption of 20 mW, this topology also consumes around 60 mW. The I/Q phase error in this topology is low and the required reference clock frequency is also low. Additionally, in the event of a PLL failure, an LO can be fed externally. In Architecture IV, a similar approach is pursued as in Architecture III. However, we have a PLL with a QVCO as the core and the hybrid is eliminated. The power consumption of a PLL at 27 GHz with a QVCO requires slightly more power and can be accomplished with about 40 mW. With a tripler power of 10 mW (as it handles half the power as in the previous case), this topology also consumes about 60 mW. However, the I/Q phase error is high due to the mismatch in the tripler in the two branches. In Architecture V, a PLL at 27 GHz is injection locked to a VCO at 80 GHz followed by amplifiers. The PLL can be designed with 30 mW of power and the 80 GHz IL-VCO with 25 mW for the required output power level, resulting in a total power consumption of 55 mW. This architecture is very similar to Architecture III except that the PLL at 27 GHz does not need to generate high power to get the required output power levels at 80 GHz. This architecture has the same benefits as Architecture III. Architecture VI is a modified version of Architecture V with the PLL being replaced by a 27 GHz IL-VCO. This is done as an IL-VCO is much easier to design

Table 5.1. Summary of LO architectures

Architecture	DC Power (mW)	I/Q Phase Error	Reference clock frequency	PLL failure backup
I	~ 60	Low	High	Not possible
II	~ 60	Low	High	Not possible
III	~ 60	Low	Low	Possible
IV	~ 60	High	Low	Possible
V	$\sim 50-60$	Low	Low	Possible
VI	$\sim 50-60$	Low	Low	Possible

compared to a PLL and has comparable performance metrics [58][59]. The summary of all the architectures is given in Table 5.1. In this design, Architecture VI has been chosen due to its merits over the other possible topologies.

Fig. 5.17 shows the 80 GHz LO architecture on the transmitter side. A 13.3 GHz reference clock is fed in externally to the chip. Using an on-chip doubler, the 27 GHz signal is generated and locked to a 27 GHz on-chip Injection-locked oscillator (IL-VCO). The signal is then amplified using a buffer stage and fed into a tripler. The output of the tripler locks the generated 80 GHz signal to an 80 GHz IL-VCO. After three stages of amplification, the I and Q signals are generated using an on-chip passive hybrid. We now discuss the individual blocks of the LO chain.

5.4.2 80 GHz Injection-locked voltage controlled oscillator

Fig. 5.18 shows the schematic of the 80 GHz IL-VCO with the injection tripler devices. Transistors M1a and M1b form the core of the oscillator and are cross-coupled to generated the required negative impedance. The output from the VCO is coupled directly using buffer stages. Varactors are used to allow tuning of the VCO center frequency to compensate for process and temperature variations. In this design a MOS varactor operating in depletion/inversion region has been used. The schematic is shown in Fig. 5.19. The design of the VCO is governed mainly by the quality factor of the varactors which is very low at 80 GHz. Fig. 5.20 shows the variation of the quality factor as a function of the control voltage (with the output nodes held at 1 V) for different channel lengths. As the channel length is increased, the maximum to minimum capacitance ration (C_{max}/C_{min}) is increased. However, the quality factor also degrades significantly with 3 being the minimum for a channel length of 150 nm. The injection into the VCO is performed using pseudo differential transistors M2a

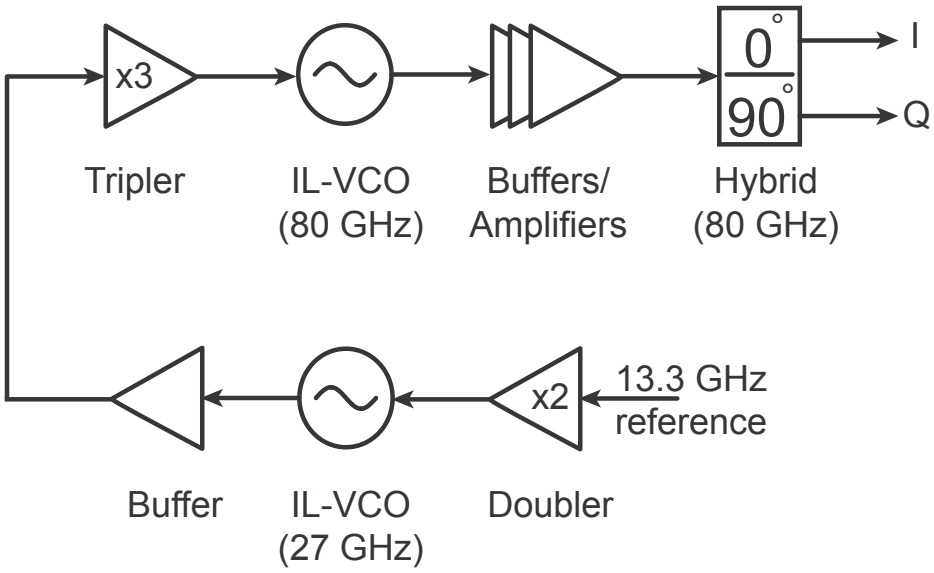


Figure 5.17. 80 GHz LO architecture

and M2b whose inputs are driven by the 27 GHz buffer. The lock range $\Delta\omega$ of an IL-VCO is given by Adler's equation as [60]

$$\Delta\omega = \left(\frac{\omega_0}{2Q}\right)\left(\frac{I_{inj}}{I_{osc}}\right)\left(\frac{1}{\sqrt{1-\left(\frac{I_{inj}}{I_{osc}}\right)^2}}\right) \tag{5.6}$$

where ω_0 is the center frequency of the oscillator, Q the quality factor of the tank, I_{inj} the injected current and I_{osc} the DC current of the oscillator.

From (5.6), to maximize the lock range, the quality factor of the tank must be lowered, the DC current consumption must also be small and the injection current should be maximized. The quality factor of the tank is dominated by the varactors and lowering it further degrades the phase noise of the oscillator [34][35]. Hence, the injection current I_{inj} must be maximized. To achieve this, the devices M2a and M2b are biased in the Class-C regime which maximizes the generated third order non-linearity. The injection signal is then coupled into the oscillator using a transformer network which also provides the required inductance for the oscillation. Fig. 5.21 shows the transformer structure layout. It consists of a 1 : 1 transformer using vertically coupled inductors. The center taps on the primary and secondary side provide the required supply voltage for the VCO and the injection device. Due to the highly non-linear action of the tripler devices, cascode stages M3a and M3b need to be added to improve the quality factor of the tank and to also keep the capacitance of the tank roughly constant during the switching action.

The design of the IL-VCO is as follows. Considering the matching of the subsequent stages, the buffer size of the IL-VCO is fixed. Assuming a reasonable inductance value with

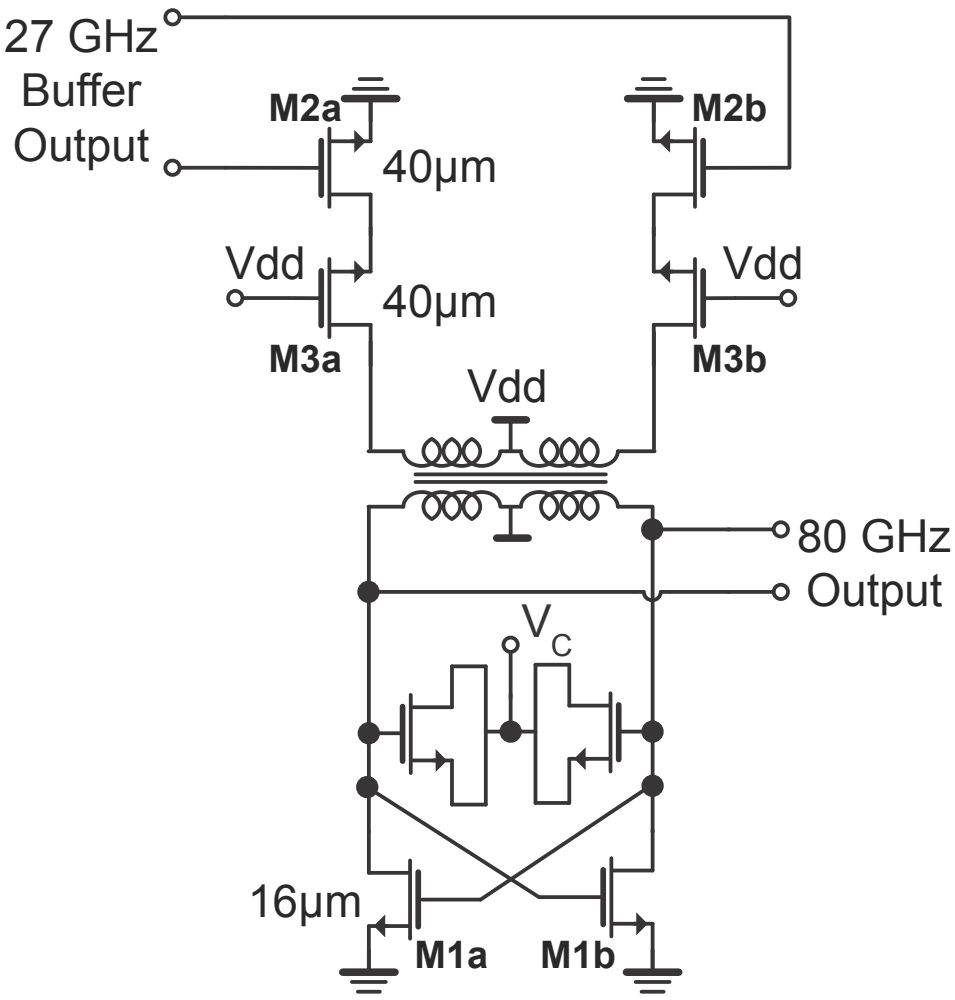


Figure 5.18. Schematic of the 80 GHz Injection-locked oscillator with the injection devices coupled using a transformer

a quality factor of 15 at 80 GHz, the total allowed tank capacitance is calculated. With a required tuning range of 8%, the required fixed and variable capacitances are calculated. Knowing the fixed capacitance, the buffer size, the varactor quality factor (based on the channel length) and assuming an initial loop gain of 3, the size of the cross-coupled pair is varied for a fixed DC current consumption and the loop gain condition is checked. If it is not satisfied, the size of the transistors is increased. Once the fixed capacitance limit is exceeded, the DC current is increased further and the process is reiterated. Various varactor choices are used to determine the optimum operating point. In this design, a MOS varactor with a sizing of $14(1\,\mu\text{m}/0.1\,\mu\text{m})$ was used. The cross coupled pairs have a sizing of $16(1\,\mu\text{m}/0.06\,\mu\text{m})$ each and the devices in the injection tripler have a sizing of $40(1\,\mu\text{m}/0.1\,\mu\text{m})$. The sizing of the tripler devices was limited mainly by the design of the transformer matching network and the maximum capacitance that it could resonate. All the transistors in the IL-VCO were implemented using triple-well devices for better isolation. The IL-VCO operates from

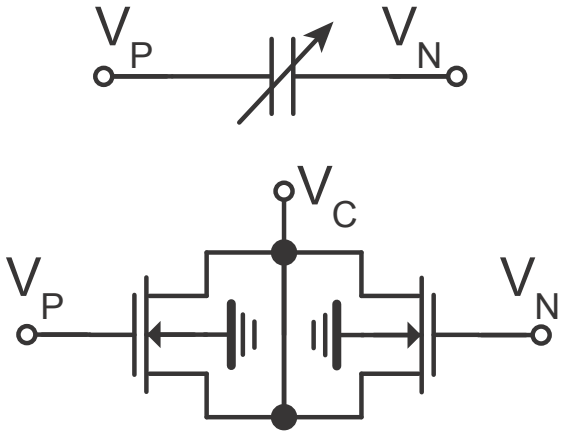


Figure 5.19. Schematic of MOS varactors used in the IL-VCO

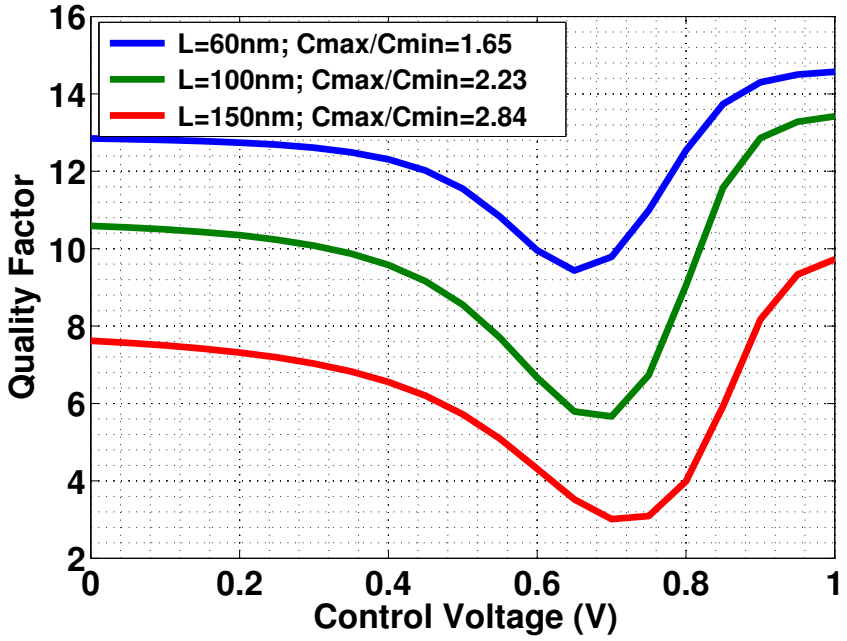


Figure 5.20. Variation of varactor quality factor with the tuning voltage at 80 GHz

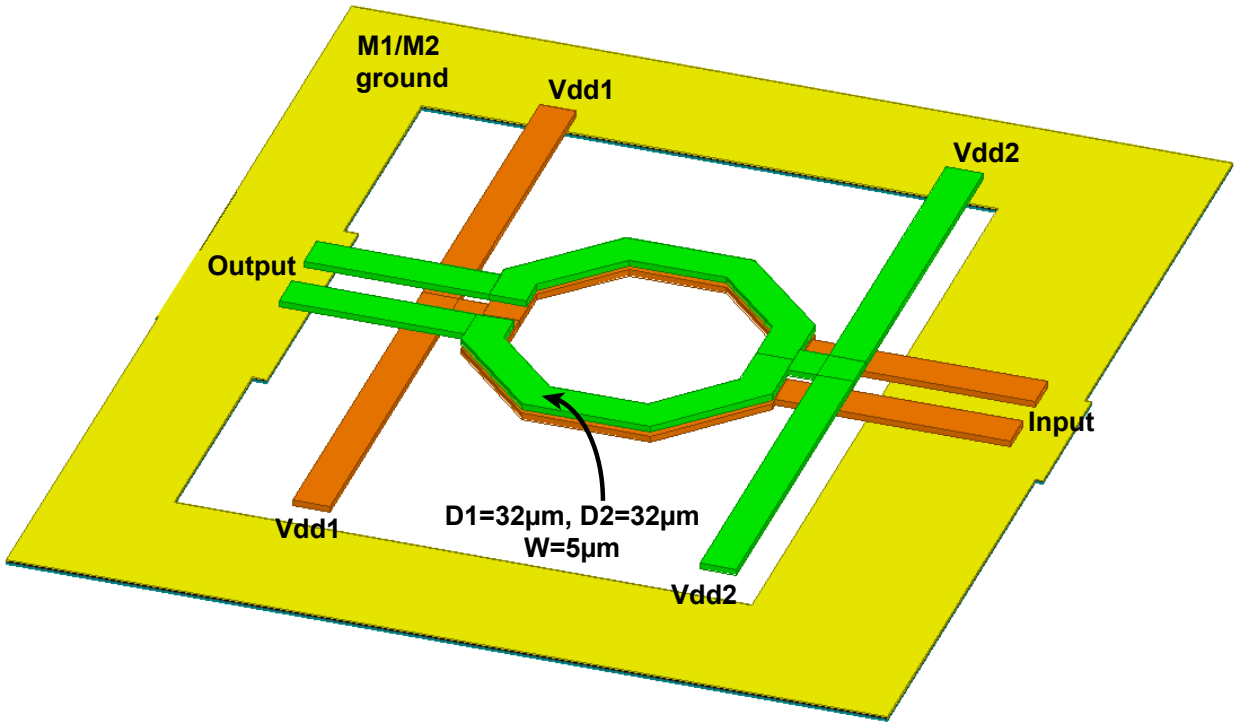


Figure 5.21. Transformer matching network between the 80 GHz IL-VCO and the injection device

a supply voltage of 0.56 V and consumes 7.2 mA while the tripler operates from a supply voltage of 1 V and consumes 11.6 mA.

5.4.3 80 GHz LO chain amplifiers

The output from the IL-VCO is amplified to the desired level using a three-stage amplifier chain. Fig. 5.22 shows the schematic of the 80 GHz LO buffer chain. The first buffer stage is directly coupled to the output of the VCO and is biased at the supply voltage of the IL-VCO. The first buffer consists of a pseudo cascode differential stage for good isolation between the output and the VCO. Each transistor is implemented using triple-well devices for good isolation and have a device size of $4(1\,\mu\text{m}/0.06\,\mu\text{m})$. The device size is selected based on the design of the IL-VCO. The buffer is coupled to the second stage using a $2:1$ transformer network implemented using vertically coupled inductors as shown in Fig. 5.23. This network transforms the input impedance of the second buffer stage to the required optimal impedance of the first buffer. The center taps of the transformers are used for supply and gate biasing.

The IL-VCO along with the buffer (first amplification stage) is simulated separately to verify its performance and oscillation frequency. Fig. 5.24 shows the simulated lock range of the IL-VCO as a function of the tuning voltage. As the tuning voltage is varied from

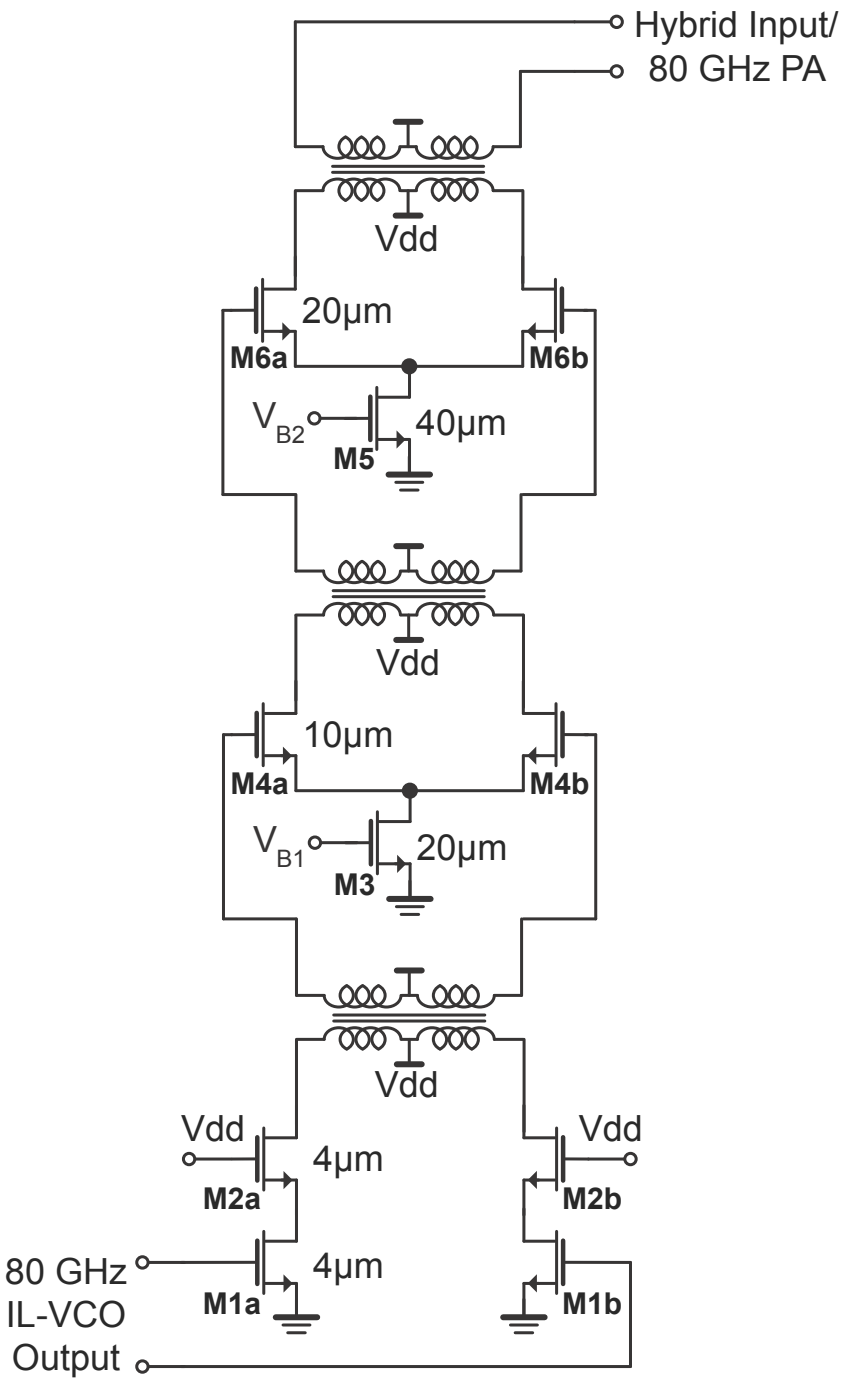


Figure 5.22. Schematic of 80 GHz LO buffer chain

0 to 0.8 V, the IL-VCO can lock to frequencies from 76 to 83 GHz. The generated output power by the buffer for these different settings is shown in Fig. 5.25. The IL-VCO with the buffer generates a peak power of −3.6 dBm and a minimum output power of −4.6 dBm. The required tripler input power for the different tuning voltages and lock conditions is shown

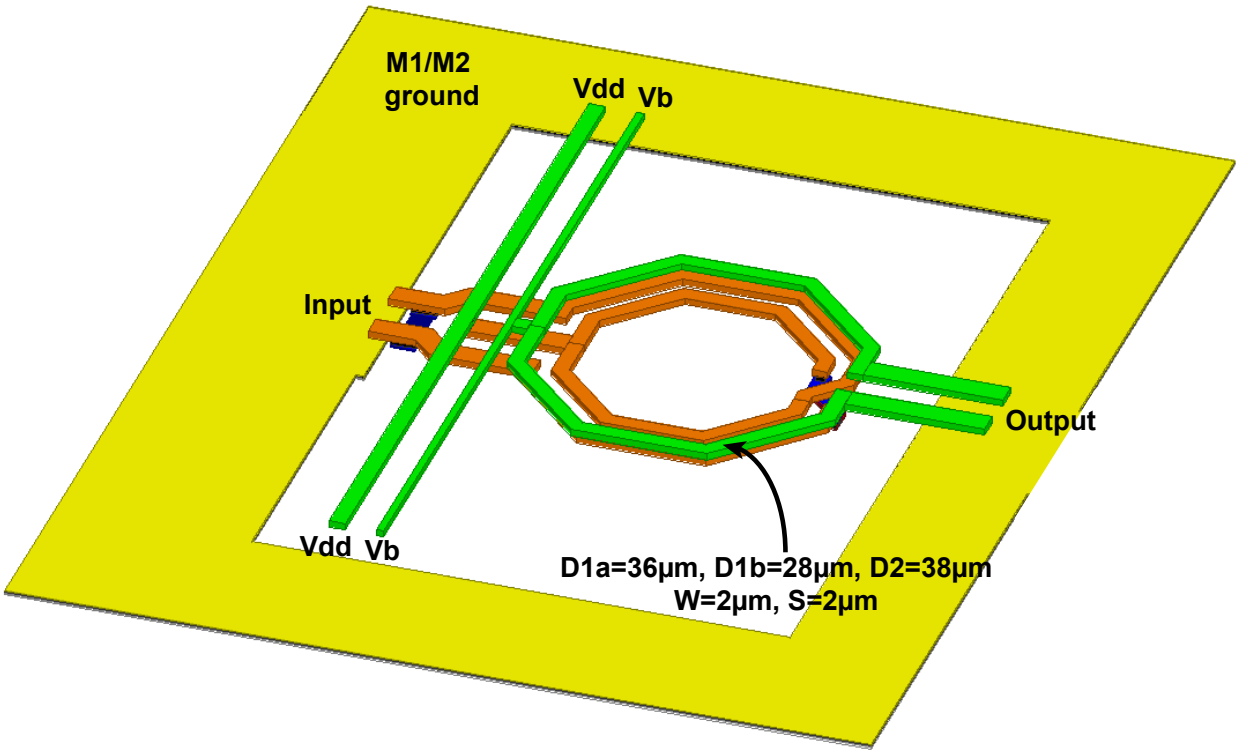


Figure 5.23. 80 GHz LO buffer chain : Buffer 1 - Buffer 2 transformer matching network

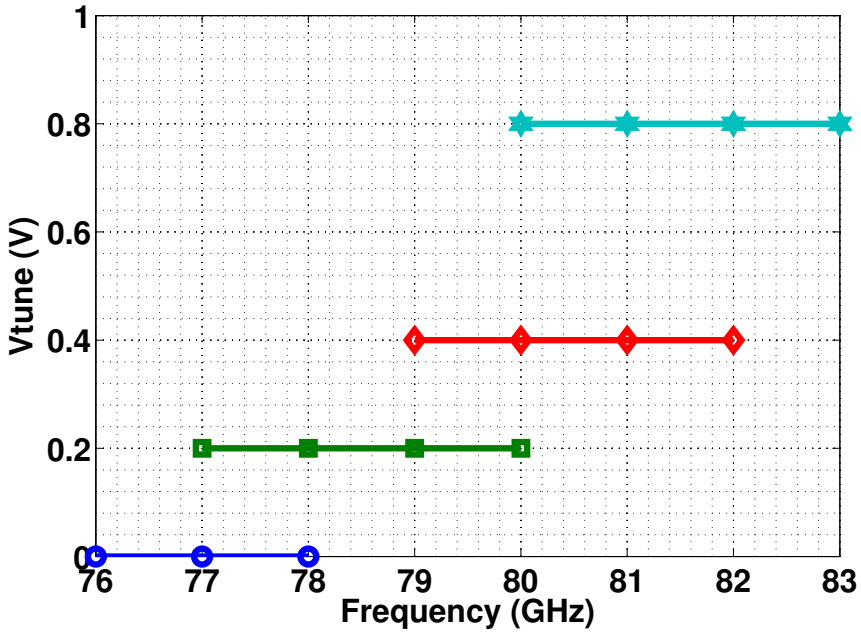


Figure 5.24. 80 GHz IL-VCO - Lock range as a function of the tuning voltage

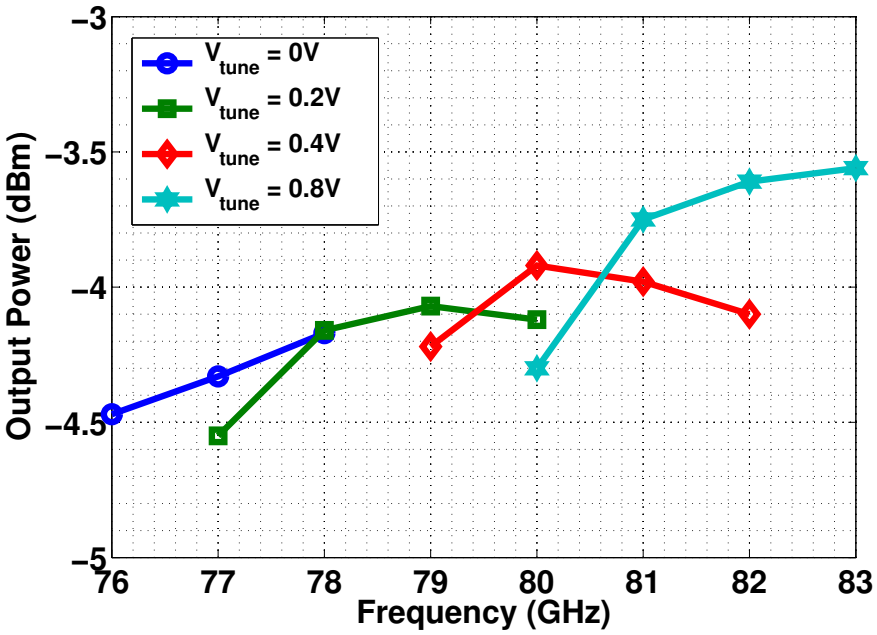


Figure 5.25. 80 GHz IL-VCO - Output power with the first buffer as a function of frequency for different tuning voltages under lock

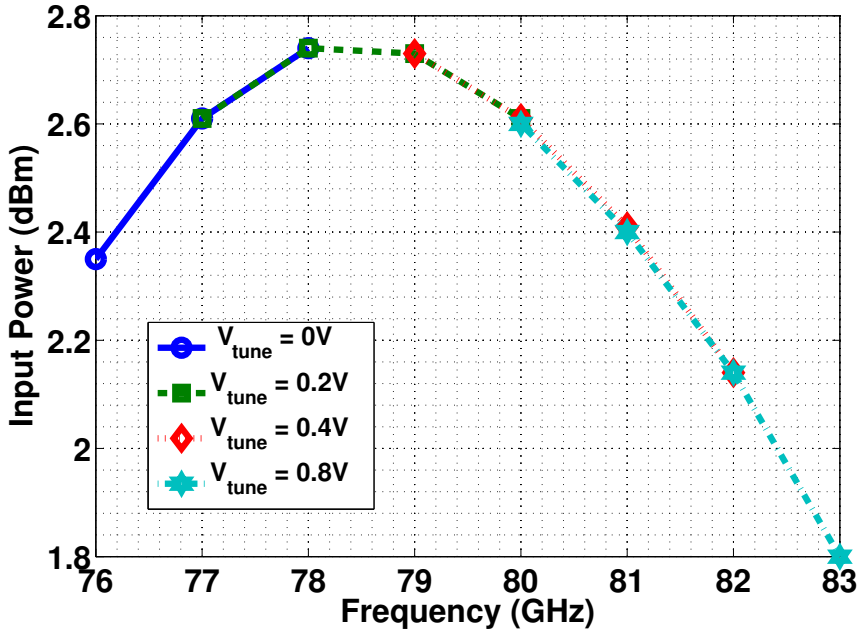


Figure 5.26. 80 GHz IL-VCO - Input power as a function of frequency for different tuning voltages under lock

in Fig. 5.26. The 27 to 80 GHz tripler requires an input power of atleast 2.75 dBm to allow locking to an external source.

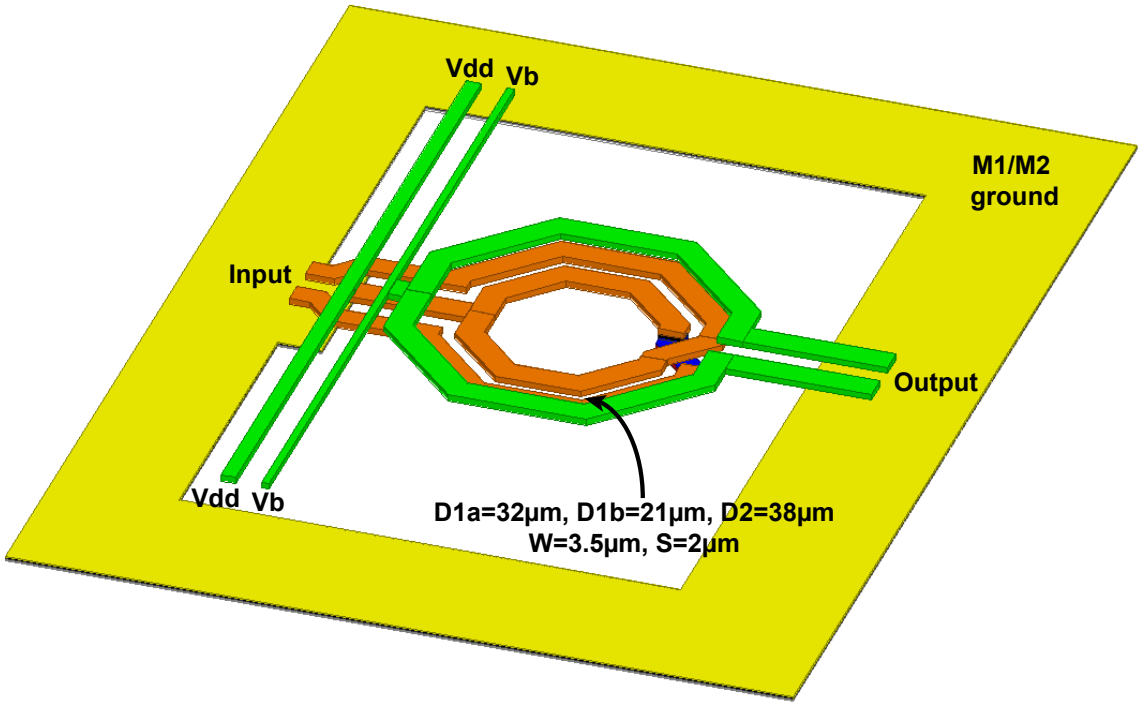


Figure 5.27. 80 GHz LO buffer chain : Buffer 2 - Buffer 3 transformer matching network

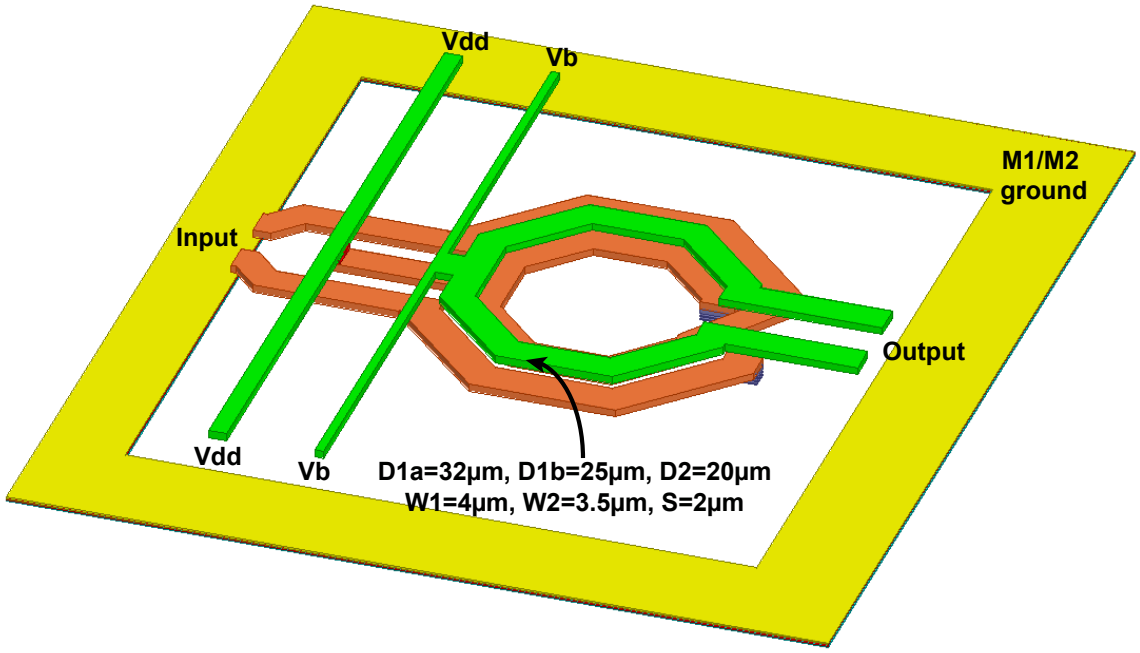


Figure 5.28. 80 GHz LO buffer chain : Buffer 3 - hybrid transformer matching network

The second and third amplification stages consist of fully differential amplifiers coupled

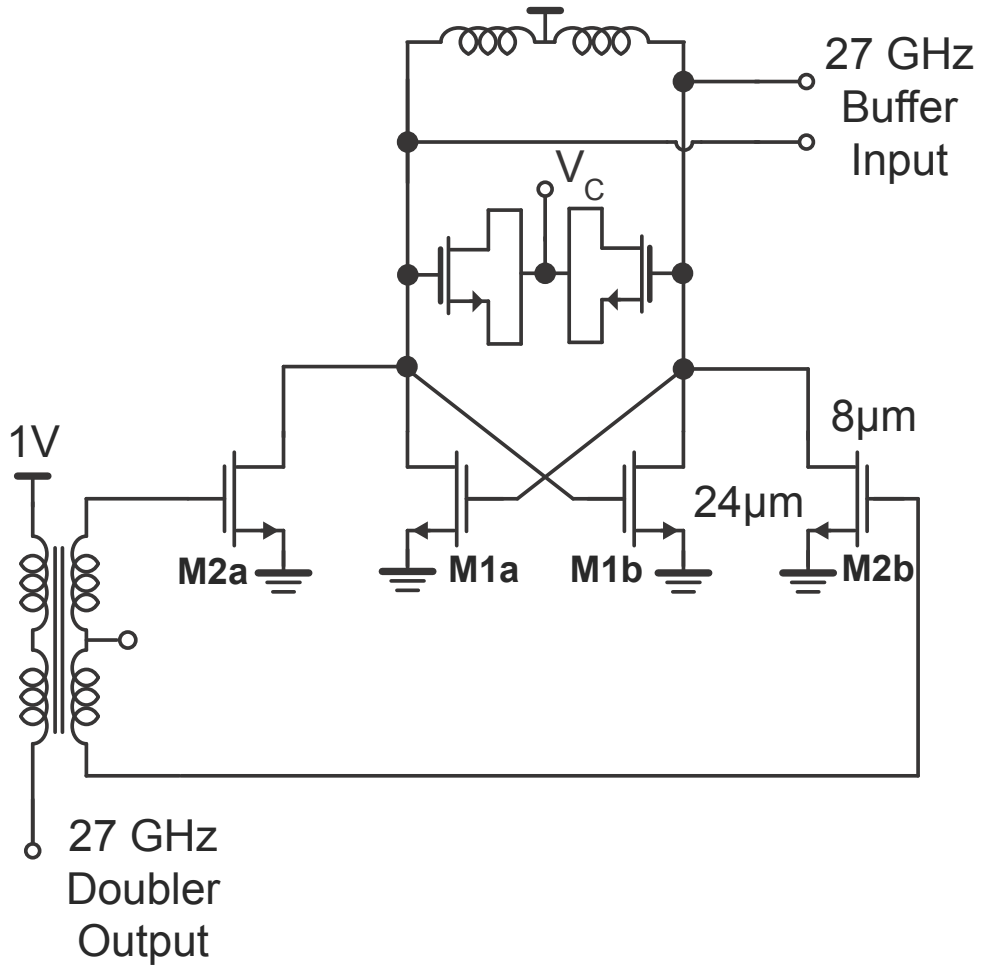


Figure 5.29. Schematic of the 27 GHz Injection-locked oscillator with the injection devices

using transformer matching networks. The second amplification stage comprises of differential pairs M4a and M4b with sizing $10(1\,\mu\text{m}/0.06\,\mu\text{m})$. The tail current source M3 is chosen to have double the size of the differential pairs. By adjusting the current flowing through the tail current source, the output power of the buffer stage is controlled. This is required as there exists an optimum power level at which the modulator operates. The designed power level of the LO chain could change with process and temperature variations and needs to be tunable. Under normal operating conditions, the current flowing in the second buffer is 3 mA. The second buffer is interfaced to the third amplification stage using a $2:1$ transformer network shown in Fig. 5.27. The buffer is matched using load-pull simulations to maximize its efficiency. The third amplification stage is similar to second one except it is impedance scaled down by a factor of two. The final amplification stage is interfaced to the hybrid using another transformer matching network shown in Fig. 5.28. The third buffer stages consumes a total current of 6 mA and is also tunable. The LO chain consisting of the IL-VCO and the three buffers generates an output power of 0 dBm and can be tuned from -5 dBm to 3 dBm.

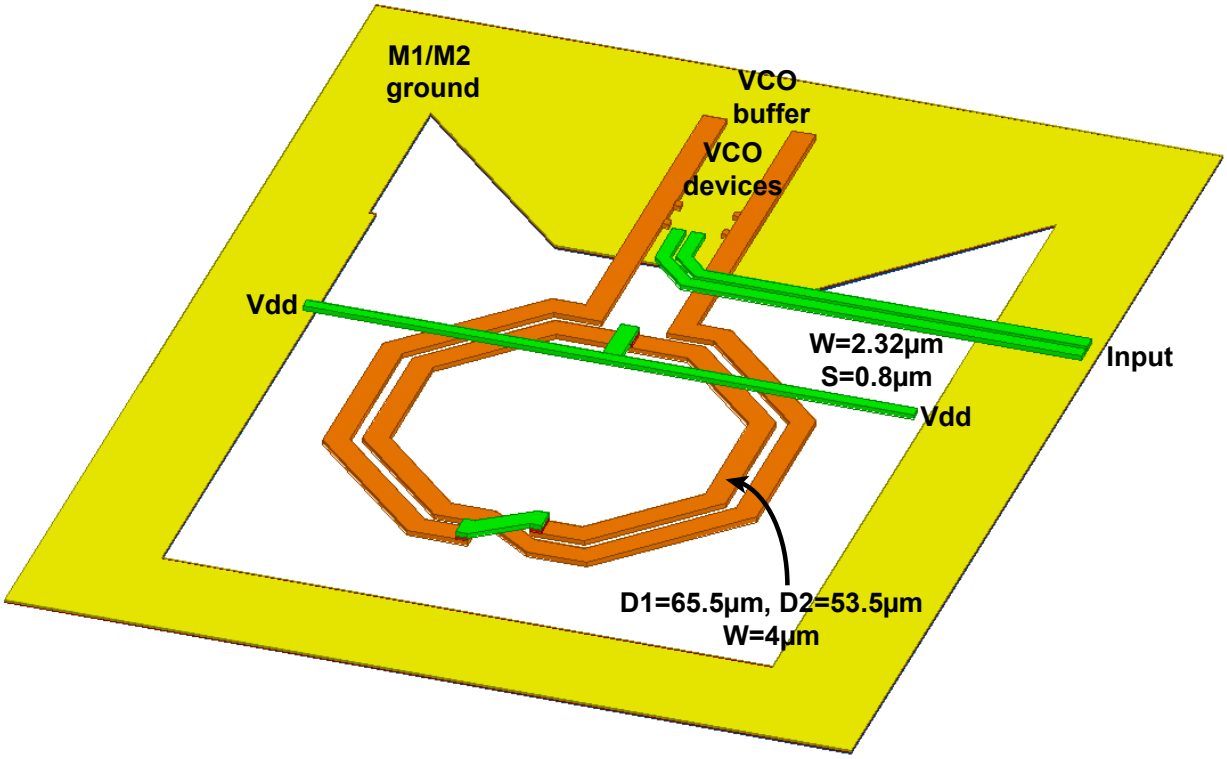


Figure 5.30. 27 GHz IL-VCO loop inductor

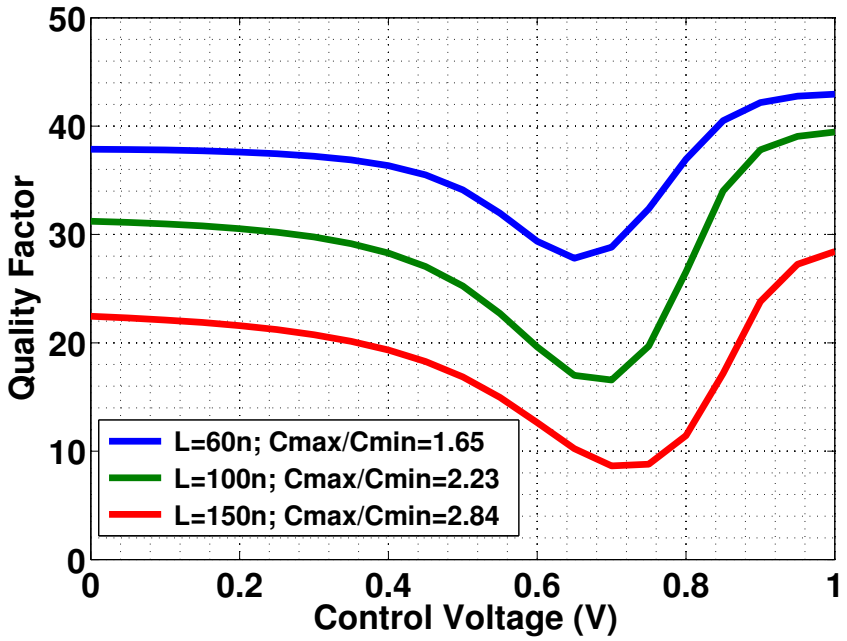


Figure 5.31. Variation of varactor quality factor with the tuning voltage at 27 GHz

5.4.4 27 GHz injection-locked voltage controlled oscillator

Fig. 5.29 shows the schematic of the 27 GHz IL-VCO. It consists of cross-coupled pairs M1a and M1b which generate the required negative impedance. Unlike the 80 GHz IL-VCO, the 27 GHz IL-VCO uses an explicit inductor for the tank. Fig. 5.30 shows the layout of the two-turn inductor. The supply for the VCO is fed using the center tap of the inductor. Varactors are used to allow tuning of the VCO center frequency to compensate for process and temperature variations. Similar to the 80 GHz, this oscillator design also uses MOS varactors operating in the depletion/inversion region for tuning. Fig. 5.31 shows the variations of the quality factors as a function of the control voltage (with the output nodes held at 1 V) for different channel lengths. As the channel length is increased, the quality factor of the varactor degrades with 9 being the minimum for a channel length of 150 nm. The injection into the VCO is performed using transistors M2a and M2b whose inputs are driven by the 27 GHz doubler output. The design procedure for the 27 GHz IL-VCO is similar to 80 GHz IL-VCO. However, the 27 GHz IL-VCO is designed such that its lock range covers the entire operation range of the 80 GHz IL-VCO. In this design, a MOS varactor with a sizing of 28(1 μm/0.15 μm) was used. The cross coupled pairs have a sizing of 24(1 μm/0.06 μm) each and the injection devices have a sizing of 8(1 μm/0.1 μm). All the transistors in the IL-VCO were implemented using triple-well devices for better isolation. The 27 GHz IL-VCO operates from a supply voltage of 0.36 V and consumes 2.15 mA.

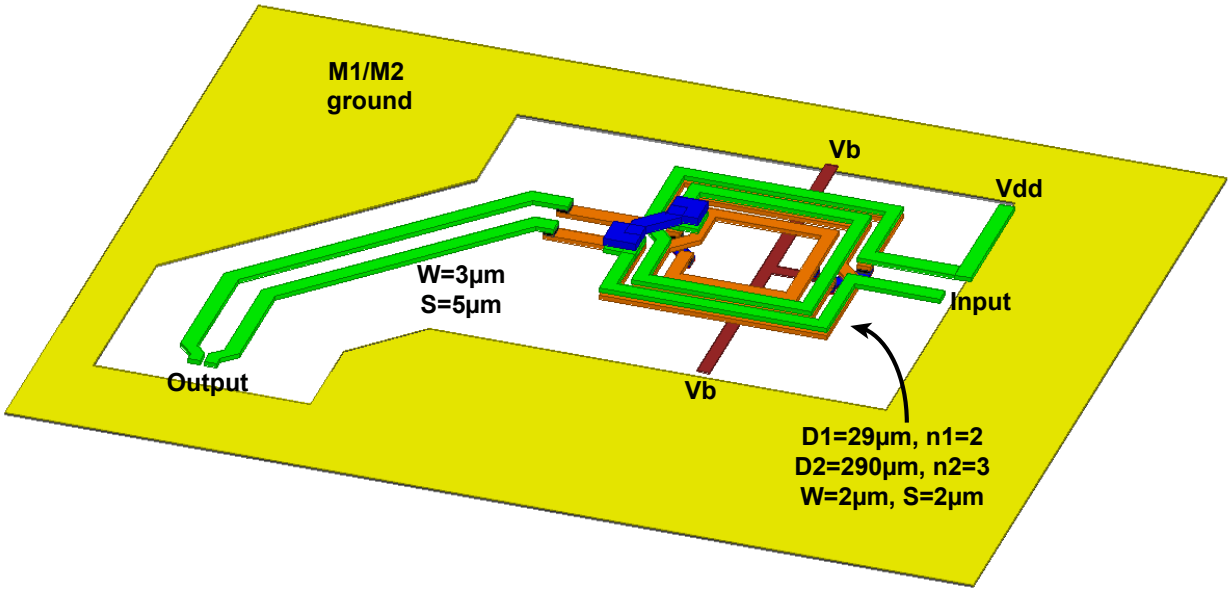


Figure 5.32. Transformer matching network between the doubler and the 27 GHz IL-VCO

The input to the 27 GHz IL-VCO injection devices is fed using CPS lines with a width of 2.32 μm and spacing of 0.8 μm. These dimensions were restricted mainly because of layout constraints. The input lines are then transitioned to another CPS lines of width 3 μm and spacing of 5 μm. Fig. 5.32 shows the balun structure used to interface the doubler to the

27 GHz IL-VCO. It consists of a 2 : 3 turn structure implemented using vertically coupled inductors. The top two metal layers are used for the inductors and the Alucap and lower metal layers are used for the cross-overs. On the primary side, one end of the balun is tied to the supply and the input from the doubler is fed to the other terminal.

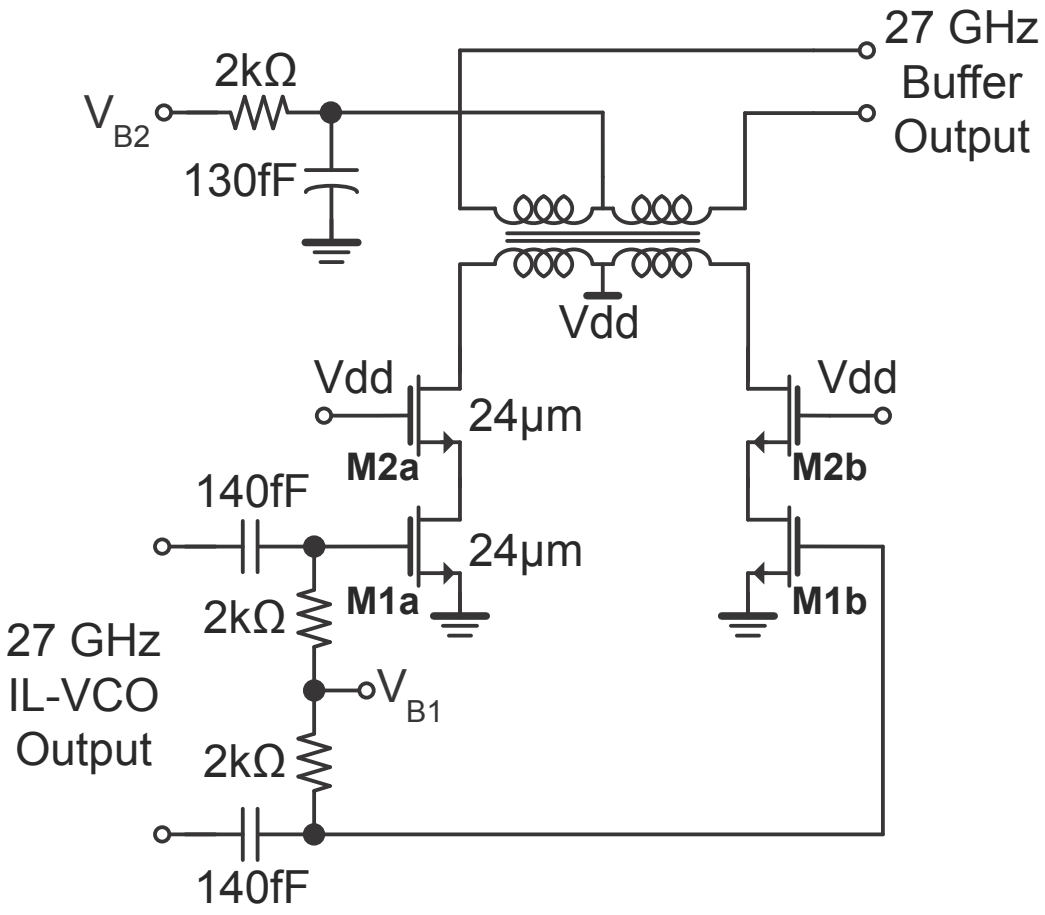


Figure 5.33. Schematic of 27 GHz LO buffer

5.4.5 27 GHz buffer

The output from the 27 GHz IL-VCO is capacitively coupled to a single buffer stage. A capacitive coupling is used to separately bias the buffers as the operating supply voltage of the IL-VCO is only 0.36 V. Fig. 5.33 shows the schematic of the 27 GHz buffer stage. It consists of a pseudo differential cascode stage and the output is load matched to the input impedance of the 27 to 80 GHz tripler. Each transistor is implemented using triple well devices and have a sizing of 24(1 μm/0.06 μm) each. The buffer stage can deliver a maximum of 5 dBm output power to the tripler stage. The output power can also be tuned by varying the input bias voltage V_{B1}. The buffer is interfaced to the tripler using a transformer matching network as shown in Fig. 5.34. Due to the highly non-linear action of the tripler and the finite C_{gd}

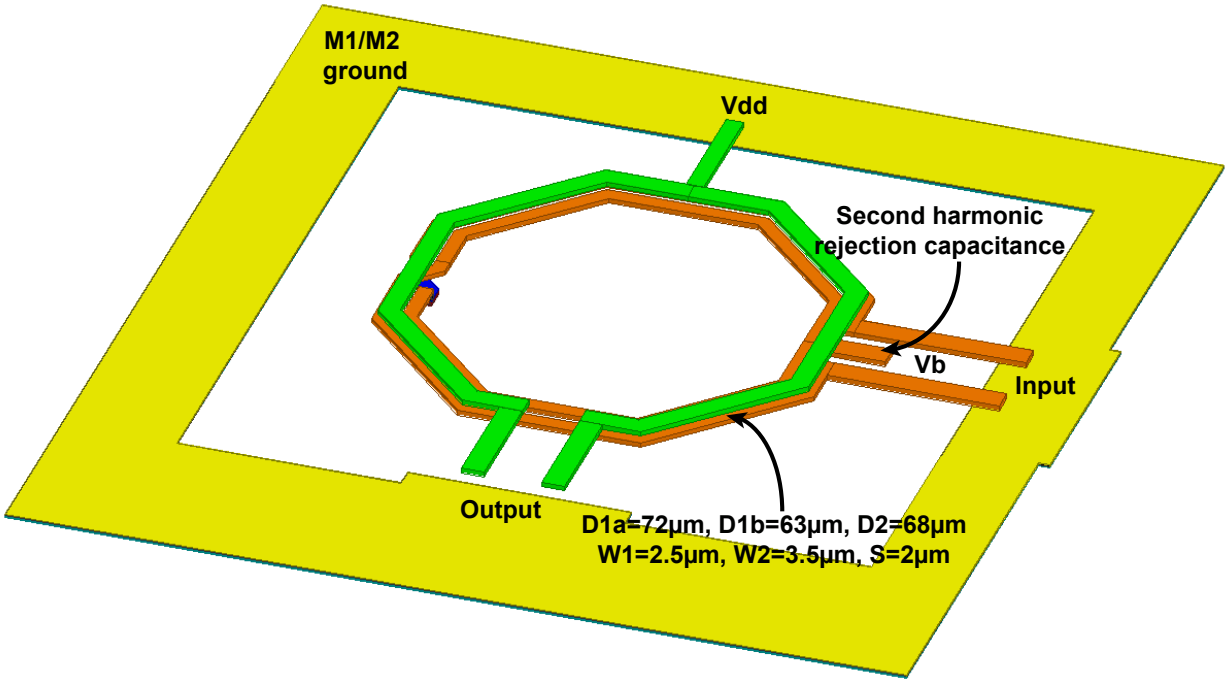


Figure 5.34. Transformer matching network between the 27 GHz LO buffer and the 80 GHz injection device

of the transistors M2a and M2b in Fig. 5.18, there is significant second harmonic kick-back to the gate nodes. This leads to a distorted sinusoidal waveform at the input and degrades the conversion gain of the tripler. This in turn leads to a lower lock range for the 80 GHz IL-VCO. Hence, the transformer matching network specifically uses a $2:1$ turn structure. For a two turn inductor, the common mode inductance is one-fourth of its inductance at the fundamental. By choosing the inductor diameter, trace width and spacing carefully, the second harmonic content at the gate nodes of M2a and M2b are filtered out by adding a capacitor at the center tap. This shorts the second harmonic kick-back to ground and preserves the sinusoidal nature of the drive waveforms. The gate is biased using a high impedance resistor. A similar idea has been used in [61].

5.4.6 Hybrid design

The in-phase and quadrature 80 GHz signals can be generated using various well-known techniques in literature with the branch-line coupler and the transformer-based hybrids being the popular ones. Fig. 5.35(a) shows the schematic of a transformer-based hybrid structure. In order achieve the hybrid operation, the coupling factor k must be set to $1/\sqrt{2}$ and the inductance and capacitance in the circuit must satisfy the relation [62][63],

$$L = \sqrt{2}C_C \tag{5.7}$$

and

$$C_G = (\sqrt{2} - 1)C_C \tag{5.8}$$

However as discussed later, a differential implementation of the hybrid is desired. Implementing a differential hybrid using a transformer-based structure results in complicated layout and the differential nature of the signals cannot be guaranteed using two separate transformers (for each of the differential signals). Hence a branch-line coupler based hybrid is used in this design. Fig. 5.35(b) shows the schematic of a branch-line hybrid. Here, each transmission line has a line length of $\lambda/4$ and the two pairs have a characteristic impedance of Z_0 while the other two have $Z_0/\sqrt{2}$. This configuration ensures perfect isolation between the I and Q channels and matches the hybrid to Z_0 at all the ports. However, the line length of $\lambda/4$ per transmission line (i.e. 1.875 mm) causes the hybrid to occupy significant die area. This motivates one to implement the hybrid using capacitively loaded transmission lines.

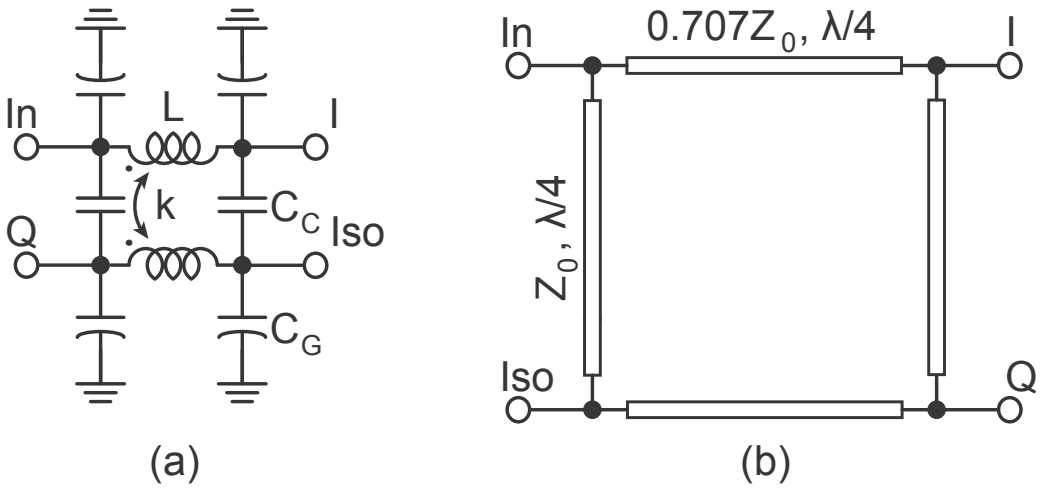


Figure 5.35. (a) Transformer-based hybrid (b) Branch-line coupler hybrid

Fig. 5.36 shows the schematic of a transmission line with characteristic impedance Z_0 and its capacitively loaded equivalent at a particular operating frequency. With a capacitive loading of C, the required electrical length in radians θ_0 at the given operating frequency ω_0 is calculated as [64]

$$\theta_0 = \cos^{-1}(\omega_0 Z_0 C) \tag{5.9}$$

The required characteristic impedance Z of the shorter transmission line is given as

$$Z = \frac{Z_0}{\sin(\theta_0)} \tag{5.10}$$

Ideally, one would like to minimize the hybrid area by choosing a shorter transmission line. However from (5.10), this results in a larger characteristic impedance compared to Z_0. The transmission lines can be implemented using either a microstrip structure or as coplanar striplines (CPS). In a microstrip structure, a high characteristic impedance requires the conductor to be placed at a larger distance from the substrate (which cannot be controlled

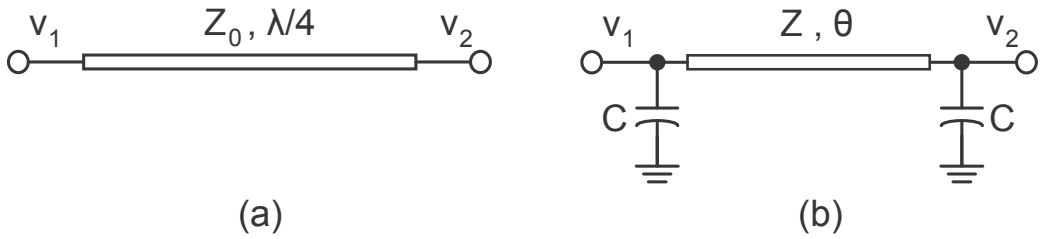


Figure 5.36. (a) $\lambda/4$ transmission line (b) Capacitively loaded equivalent

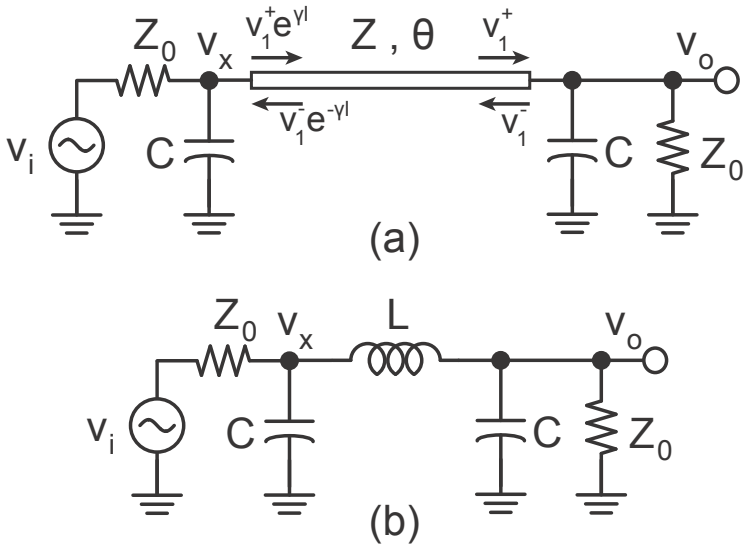


Figure 5.37. (a) Transmission line circuit with matched load (b) Transmission line circuit with lumped components

by the designer in an integrated circuit process) or using a smaller width for the conductor (which results in a higher loss). By using a CPS structure, a high impedance can be achieved by increasing the spacing between the conductors. However, the spacing cannot be increased beyond a certain limit as the odd mode needs to be the dominant mode of propagation. The other factors which govern the choice of the line length are the attenuation and the achievable bandwidth of the hybrid. To understand this, consider the schematic of the capacitively loaded transmission line shown in Fig. 5.37(a). Here, the line is terminated by a load Z_0 and is driven by a voltage source v_i with source impedance Z_0.

Using KCL at node v_o, we have

$$({v_1}^+ + {v_1}^-)(\frac{1}{Z_0} + j\omega C) = \frac{{v_1}^+ - {v_1}^-}{Z} \tag{5.11}$$

and at v_x

$$({v_1}^+ e^{\gamma l} + {v_1}^- e^{-\gamma l})(\frac{1}{Z_0} + j\omega C) + \frac{{v_1}^+ e^{\gamma l} - {v_1}^- e^{\gamma l}}{Z} = \frac{v_i}{Z_0} \tag{5.12}$$

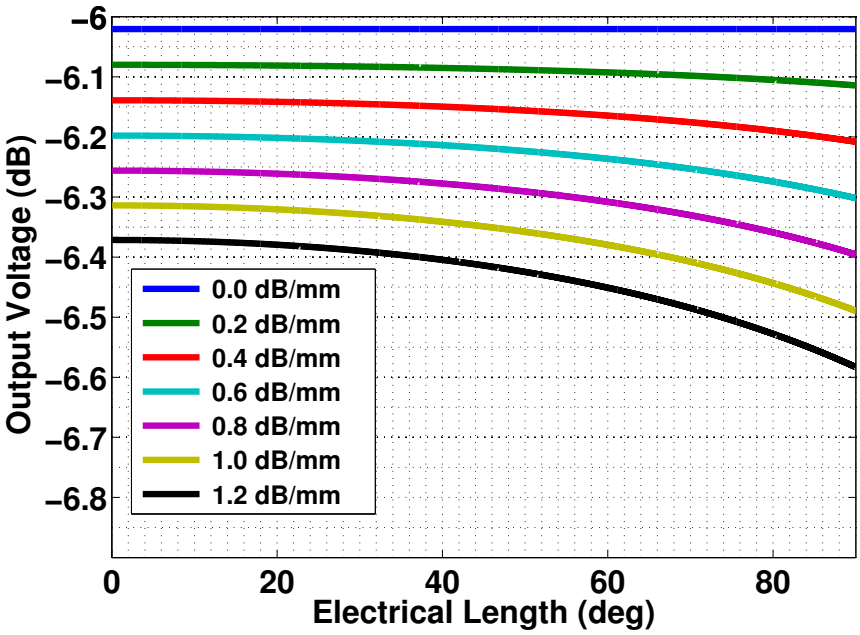


Figure 5.38. Variation of the output voltage with line length for different attenuation at 80 GHz

where γ is the propagation constant and l is the length of the transmission line. Here $\gamma = \alpha + j\beta$, where α is the attenuation constant and β the phase constant. The line length l is related to the θ as $l = c\theta_0/\omega_0$, where c is the speed of propagation in the medium.

Combining (5.9), (5.10), (5.11) and (5.12), the transfer function v_o/v_i is calculated to be

$$\frac{v_o}{v_i} = \frac{2\sin(\theta_0)}{\left[1+\sin(\theta_0)+j\frac{\omega}{\omega_0}\cos(\theta_0)\right]^2 e^{\gamma l} - \left[1-\sin(\theta_0)+j\frac{\omega}{\omega_0}\cos(\theta_0)\right]^2 e^{-\gamma l}} \tag{5.13}$$

where ω is the frequency of operation and ω_0 the frequency of design of the transmission line. Fig. 5.38 shows the plot of the output voltage as a function of the electrical line length for different attenuation constants at 80 GHz (the desired operating frequency). As the transmission line length is reduced, more capacitance is added to get the required equivalent characteristic impedance. We observe that the effect of the line length on the output voltage is negligible ($0.3 - 0.4$ dB) and can be ignored for the design of the hybrid. The bandwidth of the capacitively loaded transmission line is also simulated as a function of the line length and is shown in Fig. 5.39. For large transmission line lengths, the effect of capacitance is negligible and the response is broadband in nature. However, as the line length is reduced, the increased capacitance reduces the bandwidth of the circuit and remains constant beyond a certain point. To understand this effect, consider the schematic shown in Fig. 5.37(b). The transmission line can be represented as an equivalent Π network with inductance L. As the transmission is assumed to be short in length, its capacitance contribution is neglected

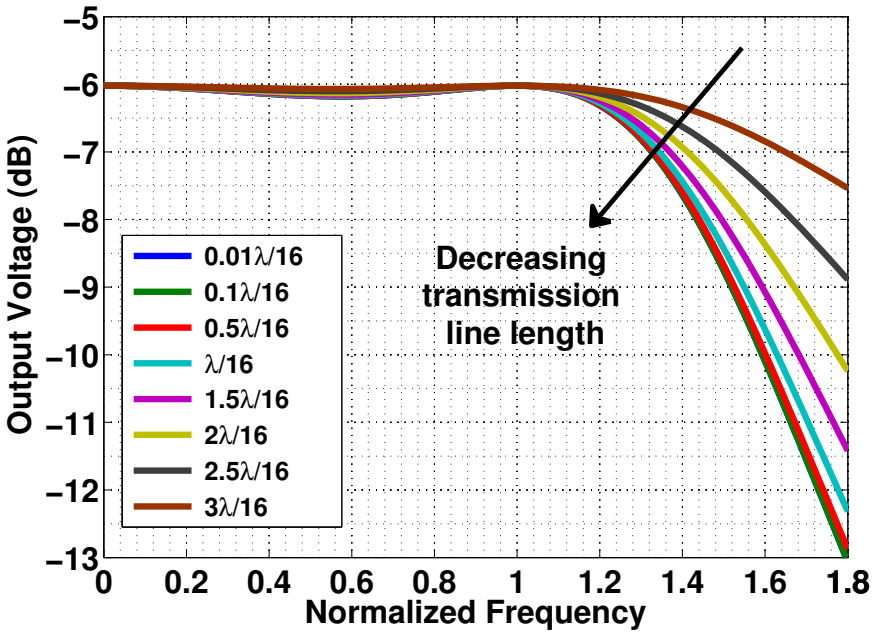


Figure 5.39. Variation of the output voltage with frequency for various line lengths

compared to the external capacitors C. The transfer function v_o/v_i is calculated to be

$$\frac{v_o}{v_i} = \frac{1}{(1 + j\omega Z_0 C)(2 - \omega^2 LC + j\omega L/Z_0)} \tag{5.14}$$

For an equivalent $\lambda/4$ line length, the inductance L must resonate with the capacitance C and hence the resonant frequency (which is same as the transmission line design frequency) $\omega_0 = 1/\sqrt{LC}$. Also, near the 3 dB bandwidth of the circuit, the characteristic impedance $Z_0 = \sqrt{L/C}$. Using these values, (5.14) can be simplified as

$$\frac{v_o}{v_i} = \frac{1}{(1 + j\frac{\omega}{\omega_0})\left[2 - (\frac{\omega}{\omega_0})^2 + j\frac{\omega}{\omega_0}\right]} \tag{5.15}$$

The 3 dB bandwidth of (5.15) is calculated to be $1.52\omega_0$ and matches well with the plots shown in Fig. 5.39. We thus observe that reducing the line length after a particular point has no significant effect on the bandwidth of the circuit.

One of the key questions that arises from the above analysis is how the above results translate to the design of a hybrid. In the case of a hybrid, each transmission line is replaced by its capacitively loaded equivalent and sees a particular load and source impedance which is proportional to Z_0. Hence, in the above analysis, the calculated bandwidth would result in a different value depending on the proportionality factors, but would still be a constant as shown above. A complete analysis of a capacitively loaded hybrid is complicated and results in less intuition of the overall circuit. Therefore, the design of the hybrid is dictated by three factors namely

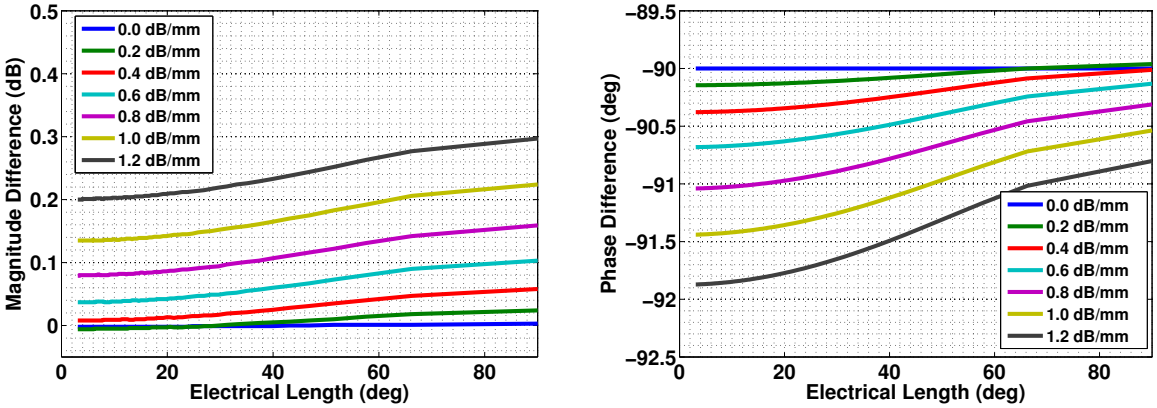


Figure 5.40. Simulated I/Q magnitude and phase difference of the hybrid as a function of the transmission line length (with characteristic impedance $Z_0/\sqrt{2}$). The transmission line with characteristic impedance Z_0 is kept constant at its nominal value.

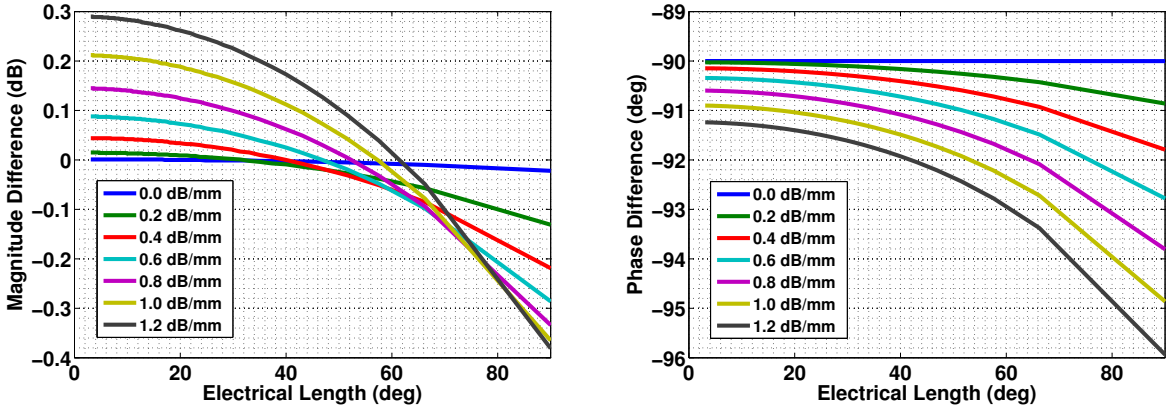


Figure 5.41. Simulated I/Q magnitude and phase difference of the hybrid as a function of the transmission line length (with characteristic impedance Z_0). The transmission line with characteristic impedance $Z_0/\sqrt{2}$ is kept constant at its nominal value.

1. The transmission line length must be minimized to reduce the area of the hybrid. However, the shortest length is limited by the maximum characteristic impedance achievable on chip.

2. If a short transmission line is used, the bandwidth penalty is negligible.

3. If the attenuation constant of the transmission line is not significant, using a shorter line length has no benefit.

In order to validate these results, the capacitively loaded hybrid was simulated for different attenuation and transmission line lengths. The termination impedance Z_0 was $54\,\Omega$ in tune with the final design value. The transmission line lengths were varied by changing their characteristic impedance and adjusting the capacitance values accordingly. Fig. 5.40

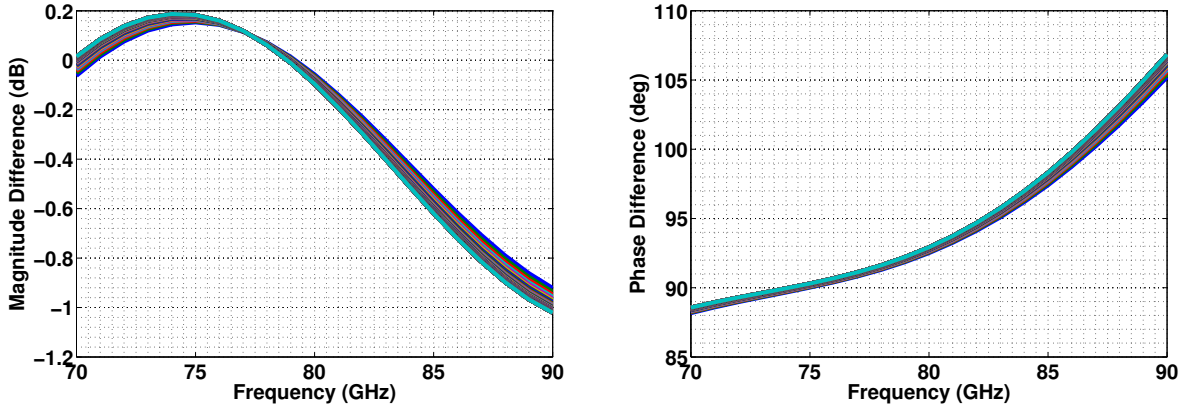


Figure 5.42. Simulated I/Q magnitude and phase difference of the hybrid as a function of frequency for different transmission line length (with characteristic impedance $Z_0/\sqrt{2}$). The transmission line with characteristic impedance Z_0 is kept constant at its nominal value.

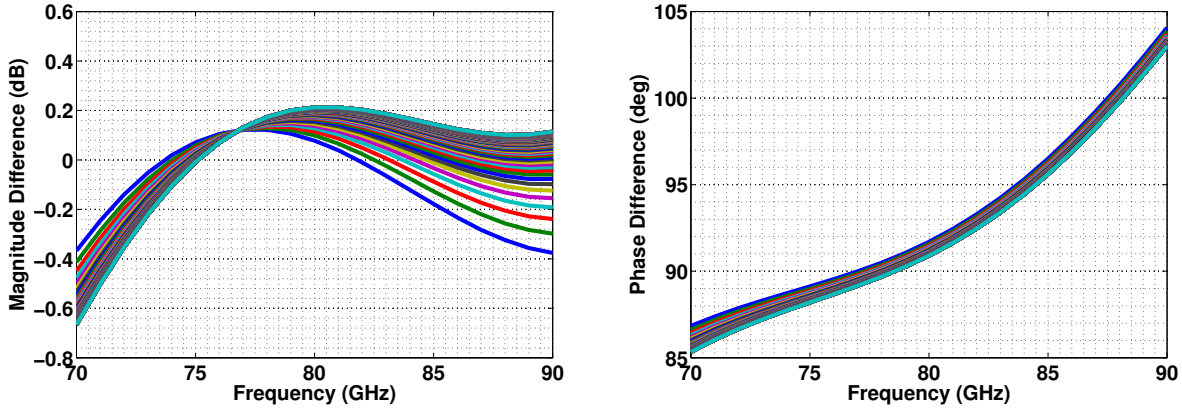


Figure 5.43. Simulated I/Q magnitude and phase difference of the hybrid as a function of frequency for different transmission line length (with characteristic impedance Z_0). The transmission line with characteristic impedance $Z_0/\sqrt{2}$ is kept constant at its nominal value.

and Fig. 5.41 show the simulated I/Q magnitude and phase difference of the hybrid as a function of the transmission line length at 80 GHz. In Fig. 5.40, the length of the $Z_0/\sqrt{2}$ line is varied while keeping the Z_0 line at its nominal value (characteristic impedance of 105 Ω) and vice-versa for Fig. 5.41. In both cases (as predicted by our simplified model of a single transmission line), the effect of attenuation on the magnitude and phase difference is minimal for short line lengths. Fig. 5.42 and Fig. 5.43 show the effect of the line length on the I/Q magnitude and phase difference as a function of frequency. Here, no transmission line attenuation is assumed. As predicted by our analysis of the transmission line, for short transmission line structures, the effect is negligible and not a strong function of the line length.

The conventional method of obtaining a differential in-phase and quadrature signal is to

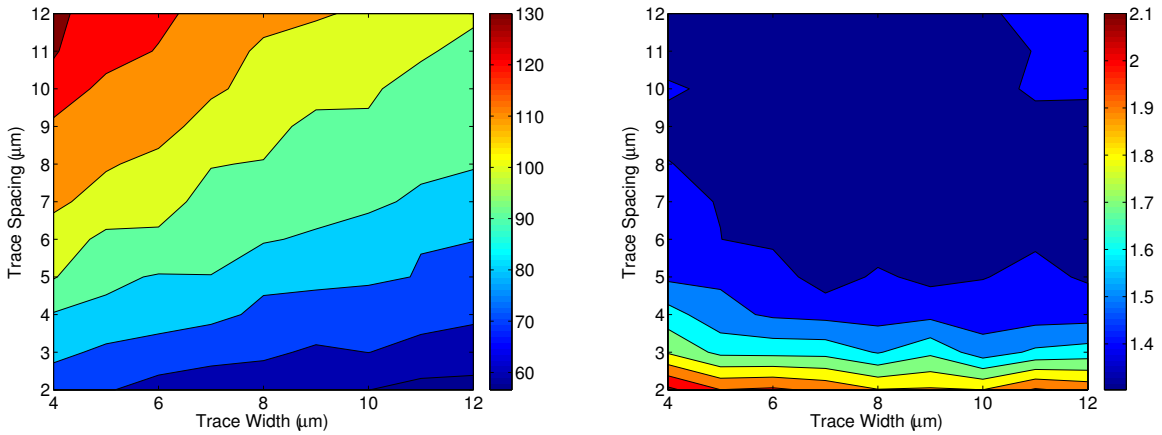


Figure 5.44. Simulated characteristic impedance and loss in dB/mm of CPS lines as a function of conductor width and spacing at 80 GHz

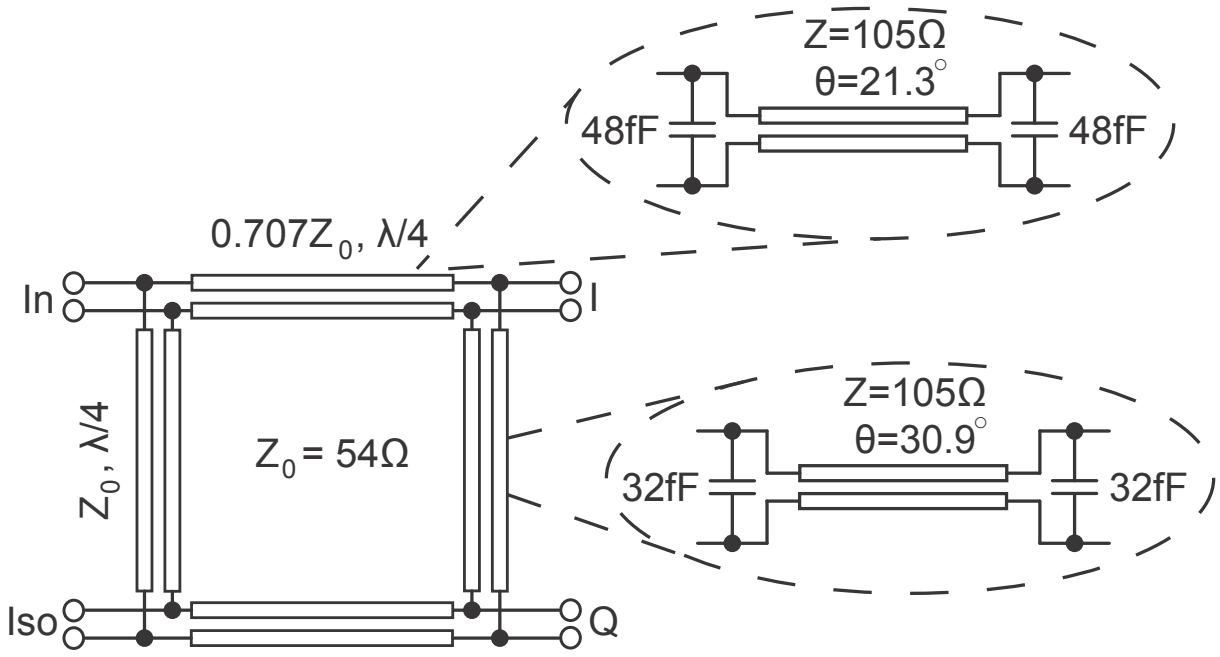


Figure 5.45. Schematic of differential hybrid structure

design a single-ended hybrid followed by a balun. However, the implementation of a balun at mm-wave frequencies is challenging. In order to obtain perfect differential outputs, the common-mode path of the balun must be tuned using capacitors and also requires careful design of the return ground paths. Additionally, the use of a balun makes the design sensitive to common-mode noise and coupling from adjacent circuitry. In order to circumvent this, the hybrid is designed to be completely differential in nature. It uses a capacitively

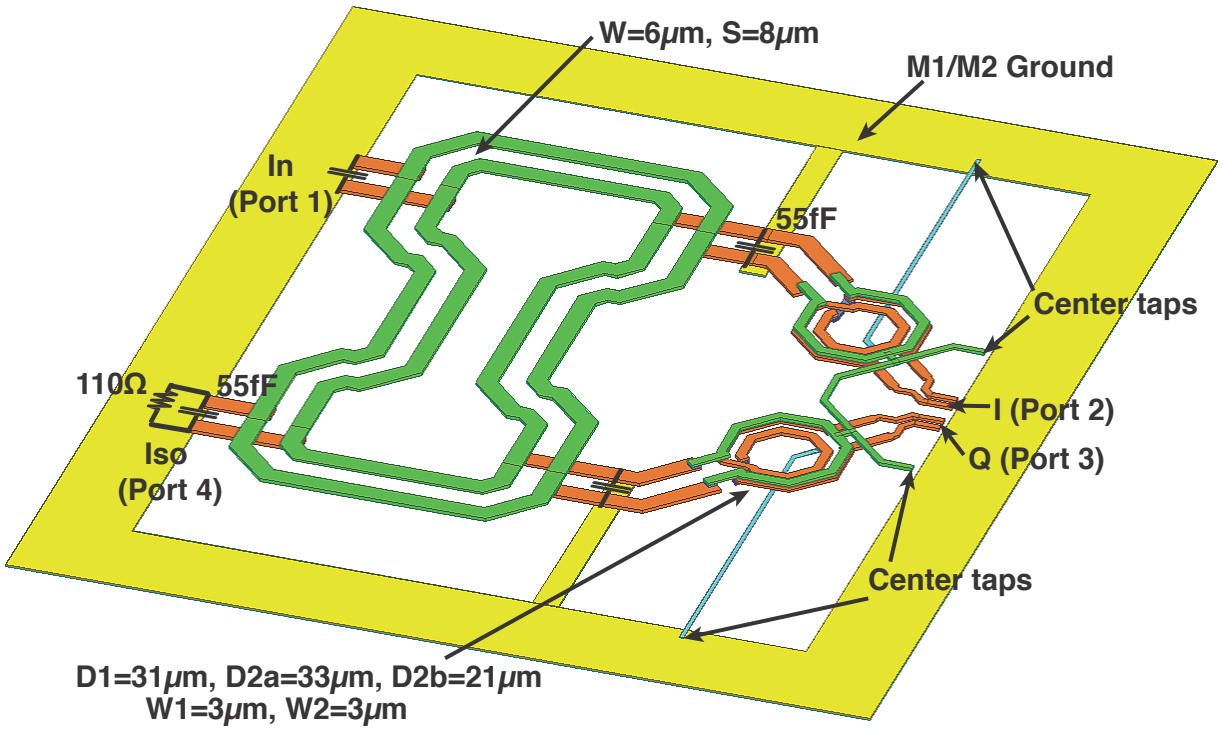


Figure 5.46. Layout of differential hybrid structure

loaded branchline coupler structure where the transmission lines are implemented as coplanar striplines (CPS).

Fig. 5.44 shows the simulated characteristic impedance and loss (in dB/mm) of the CPS lines as a function of the conductor width and spacing. As expected, increasing the spacing and decreasing the conductor width results in a large characteristic impedance for the line with a maximum of 130 Ω. It also leads to a lower loss with the minimum being equal to 1.3 dB/mm. However, using a large spacing results in a significant even mode propagation through the line and hence the maximum spacing is restricted to 8 μm to allow the odd mode to be dominant. Fig. 5.45 shows the schematic of the differential hybrid implemented using coplanar striplines. Each transmission is in-turn implemented as a shorter capacitively loaded transmission line with characteristic impedance of 105 Ω. This was chosen based on the maximum allowed spacing between the lines (8 μm). Additionally, the horizontal and vertical branches have the same characteristic impedance to allow easy layout of the structure.

The layout of the hybrid structure is shown in Fig. 5.46. The transmission line section are implemented in the top thick metal layer with a surrounding ground plane in Metal1/Metal2. The outputs from the hybrid are tapped in the next lower thick metal layer and the impedance transformation from these sections are compensated for by changing the capacitance values. After compensating with a capacitance of 55 fF, the differential impedance seen into each port of the hybrid (with the others terminated with appropriate impedances) is 110 Ω. Due to layout constraints, the length of the CPS lines are not exactly equal. Additionally,

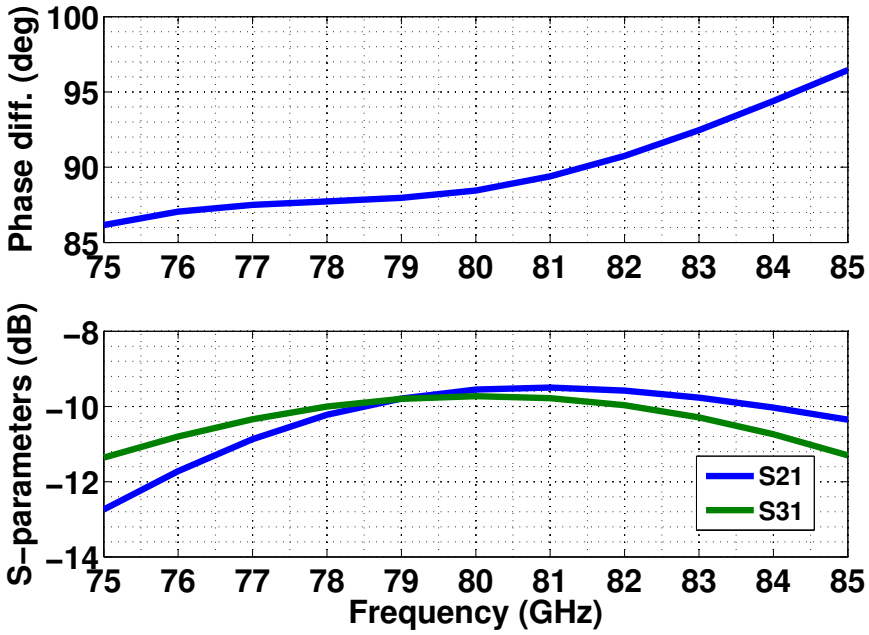


Figure 5.47. Simulated phase difference and gain of differential hybrid structure including the input transformer (not shown)

there is even-mode propagation through the lines due to the close proximity of the ground planes. These factors affect the performance of the hybrid and results in the output voltage waveforms that are not exactly differential in nature. To provide sufficient common-mode rejection ratio, a 2-to-1 transformer is added between the modulator and the hybrid. The center taps of the transformer are carefully laid out to provide a low impedance path for the common mode signals on the primary side. On the secondary side, the center tap is used to bias the modulator. The transformer also serves as a matching network and transforms the high impedance on the modulator side ($872\,\Omega||15.5\,\text{fF}$) to $110\,\Omega$. The complete structure is simulated in HFSS and the simulation results with extracted capacitors is shown in Fig. 5.47. The phase difference is within $\pm 2.5°$ across the 5 GHz band centered around 80 GHz. The magnitude difference is also within ± 1 dB.

5.4.7 Simulation Results of the complete LO Chain

The complete LO chain comprising of the 27 GHz IL-VCO, 80 GHz, the injection devices, the buffer stages, the hybrid and the discussed matching networks were simulated across tt, ss and ff corners. Fig. 5.48 to Fig. 5.50 show the simulated results across the different corners. Here, the output frequency range around 80 GHz has been used for all the blocks. The LO chain has a lock range of 7 GHz starting from 76 GHz to 83 GHz in the typical and fast corner case and a lock range of 6 GHz in the slow corner. In all the simulations, the output power in the I and Q channels are matched at the design frequency of 80 GHz. The required

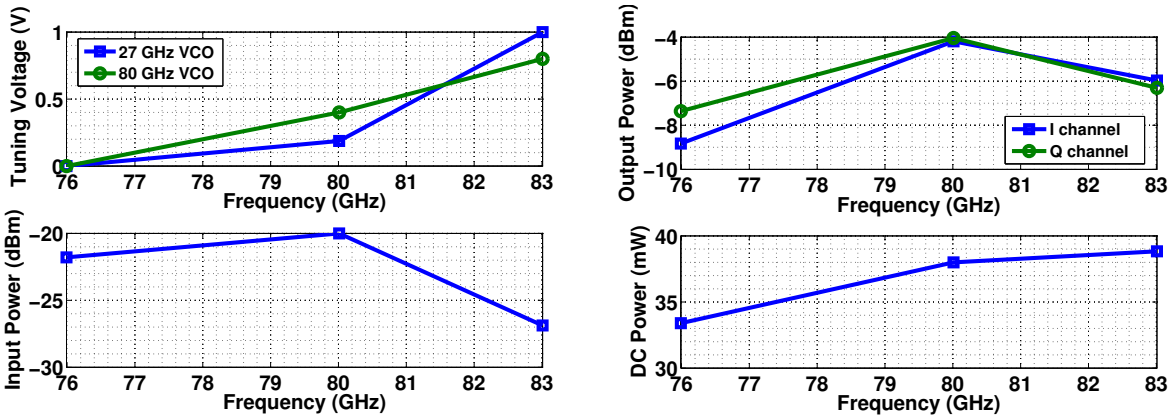


Figure 5.48. Tuning voltages, Input Power, Output Power and DC Power consumption as a function of frequency (tt corner)

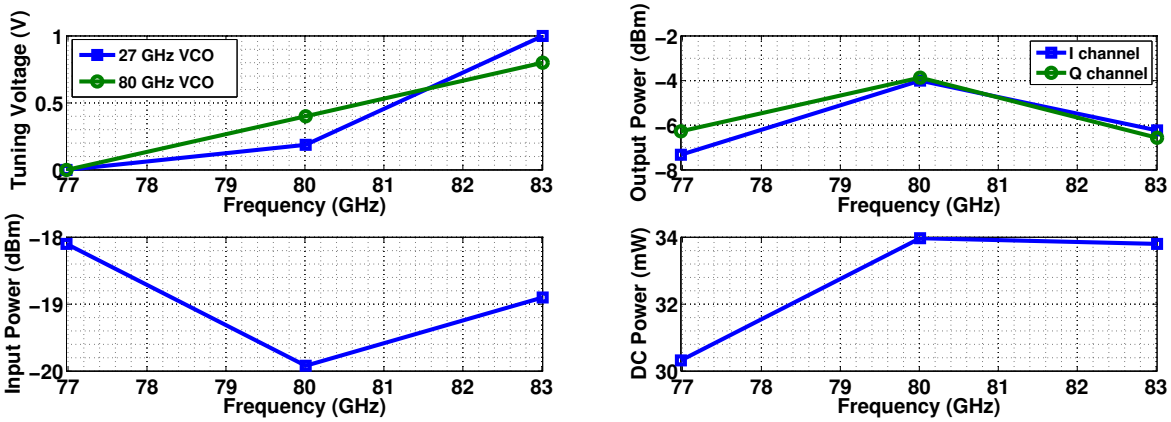


Figure 5.49. Tuning voltages, Input Power, Output Power and DC Power consumption as a function of frequency (ss corner)

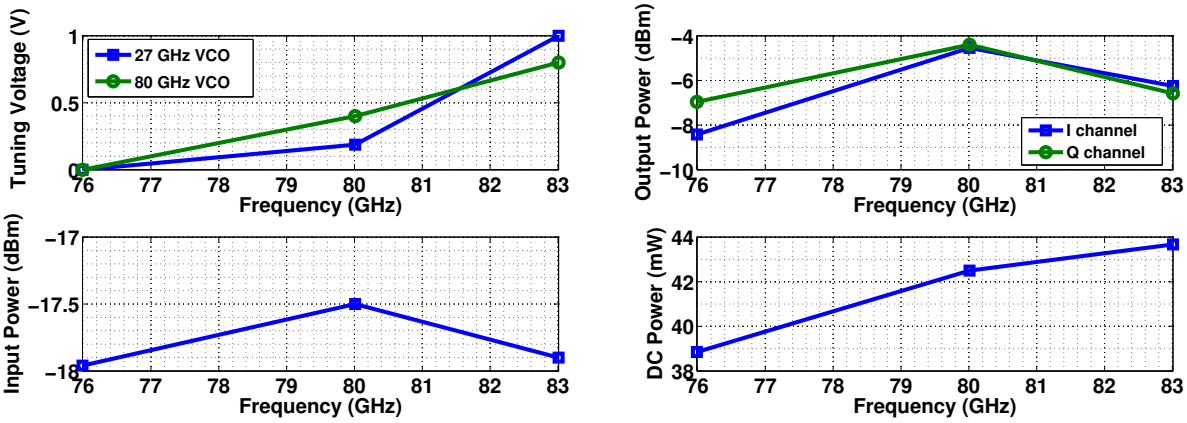


Figure 5.50. Tuning voltages, Input Power, Output Power and DC Power consumption as a function of frequency (ff corner)

input power for the doubler is −20 dBm at 27 GHz. The complete LO chain consumes a total power of 38 mW.

5.5 Conclusion

In this chapter, we discussed the design of a 240 GHz 16 Gbps QPSK wireless transceiver for chip-to-chip communication. Various blocks in the transmitter and receiver chips were discussed. A pair of slotted loop antennas is used for both the transmitter and receiver chips. By using a copper ground plane, the antenna achieves a peak array gain of 1.5 dBi for the transmitter and 0.7 dBi for the receiver. The local oscillator architecture (LO) is common to both the chips. It uses an 80 GHz injection locked VCO (IL-VCO) that is locked using a 27 GHz IL-VCO which in-turn is locked to an external 13.3 GHz reference. On the transmit side, the in-phase and quadrature LO signals are generated using a differential hybrid implemented using coplanar striplines.

Chapter 6

A 240 GHz QPSK Wireless Transceiver in 65 nm CMOS - Part II

In this chapter, we discuss the design of the sub-terahertz mixer operating at 240 GHz. Active and passive mixer topologies are discussed and their performance metrics at these frequencies namely conversion gain and noise figure are compared. The transmitter and transmitter-receiver link measurements are also discussed and compared with state-of-the-art designs at these frequencies.

6.1 Sub-Terahertz Mixer Design

As discussed earlier, an LNA is not feasible in this receiver design as the operating frequency is greater than the f_{max} of the technology. If one employs a super heterodyne architecture, the intermediate frequency (IF) must be chosen to be sufficiently high (typically in the GHz range) to allow high data rate communication. This leads to severe penalties in terms of the conversion gain and noise figure of the receiver chain. Additionally, a single sideband (SSB) noise figure metric needs to be used for this architecture and this leads to a 3 dB penalty compared to a direct conversion case (double sideband (DSB) noise figure is used). Hence, in this design we employ a mixer first direct conversion architecture to down-convert the 240 GHz signal to baseband. The mixer is implemented as a fully balanced architecture to avoid any RF and LO leakages to the output. However, the mixer implementation could either be active or passive. A simple analytical framework is presented to understand the performance differences between the two cases.

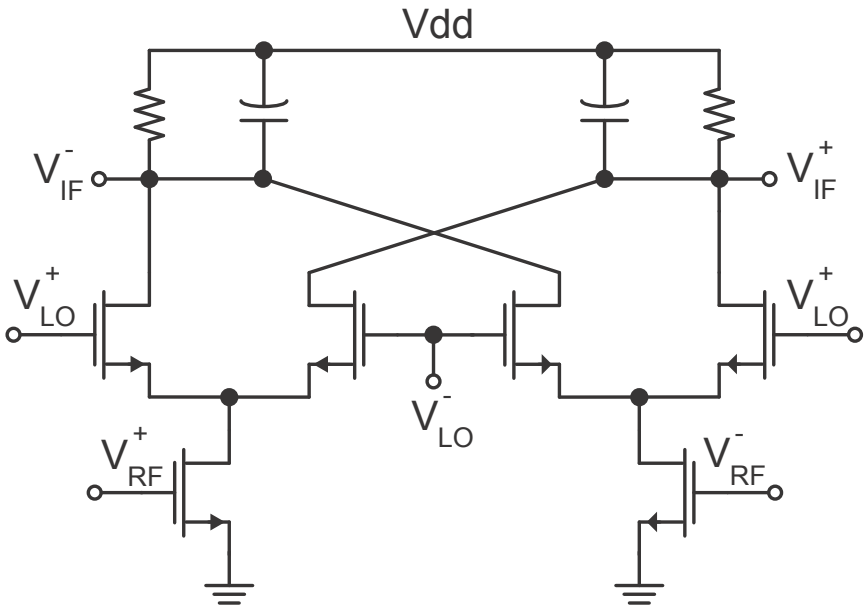


Figure 6.1. Schematic of fully balanced active mixer

6.1.1 Sub-Terahertz Active Mixer

Fig. 6.1 shows the schematic of a fully balanced Gilbert mixer. The RF signals are fed to the bottom devices that are biased with a constant DC current. The high swing LO signals are fed to the differential pair and due to the current switching action of the circuit, the RF signal is down-converted to a lower frequency (IF). A low pass filter at the output rejects the high frequency signals while preserving the required IF signals. Since our design cannot employ an LNA up-front, the noise figure of the mixer must be minimized to achieve an overall low receiver noise figure. Using an analytical approach, we now try to estimate the best noise figure that can be achieved using the active mixer topology.

Fig. 6.2 shows the active mixer schematic with the small signal model for the RF device. Here, R_a represents the antenna impedance, R_g the device gate resistance which includes the sum of the poly resistance and the non-quasi static resistance [40], r_o the device output resistance, C_{gs} the gate-source capacitance, L_s the inductance required for the input match and g_m the transconductance of the device. The noise sources from the antenna, the device gate resistance and the device transconductance are represented by v_{n,R_a}, v_{n,R_g} and i_{n,g_m} respectively. The corresponding noise spectral densities are also given. The single sideband (SSB) noise factor F of the mixer without considering the noise from the LO devices is given as

$$F = 2\left[1 + (R_a + R_g)^2\left(\frac{f_0}{f_T}\right)^2\frac{\gamma g_m}{R_a} + \frac{R_g}{R_a}\right] \tag{6.1}$$

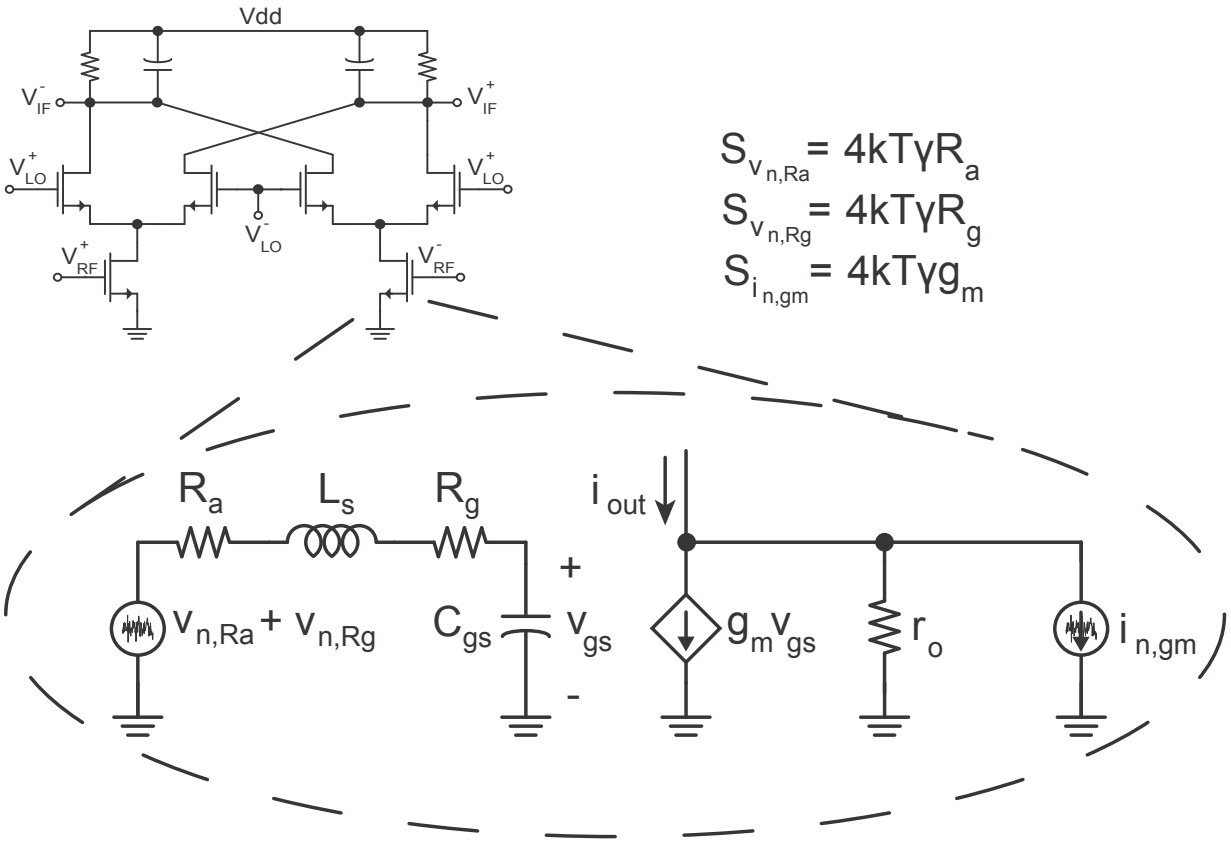


Figure 6.2. Noise analysis of fully balanced active mixer

where f_0 is the operating frequency and f_T is the transition frequency of the device. The maximum oscillation frequency of the device f_{max} can be computed as [21]

$$\omega_{max} = \frac{\omega_T}{2}\sqrt{\frac{r_o}{R_g}} \tag{6.2}$$

Using (6.2) in (6.1), we obtain the SSB noise factor F as

$$F = 2\left[1 + (R_a + R_g)^2\left(\frac{f_0}{f_{max}}\right)^2 \frac{\gamma g_m r_o}{4R_a R_g} + \frac{R_g}{R_a}\right] \tag{6.3}$$

Under a conjugate match case i.e $R_a = R_g$, the noise factor becomes

$$F = 2\left[2 + \left(\frac{f_0}{f_{max}}\right)^2 \gamma g_m r_o\right] \tag{6.4}$$

With $\gamma = 2$, $g_m r_o = 5$ in this technology node, an operating frequency $f_0 = 240\,\text{GHz}$ and a device $f_{max} = 200\,\text{GHz}$, the noise figure $NF = 10\log_{10}(F) = 15.16\,\text{dB}$.

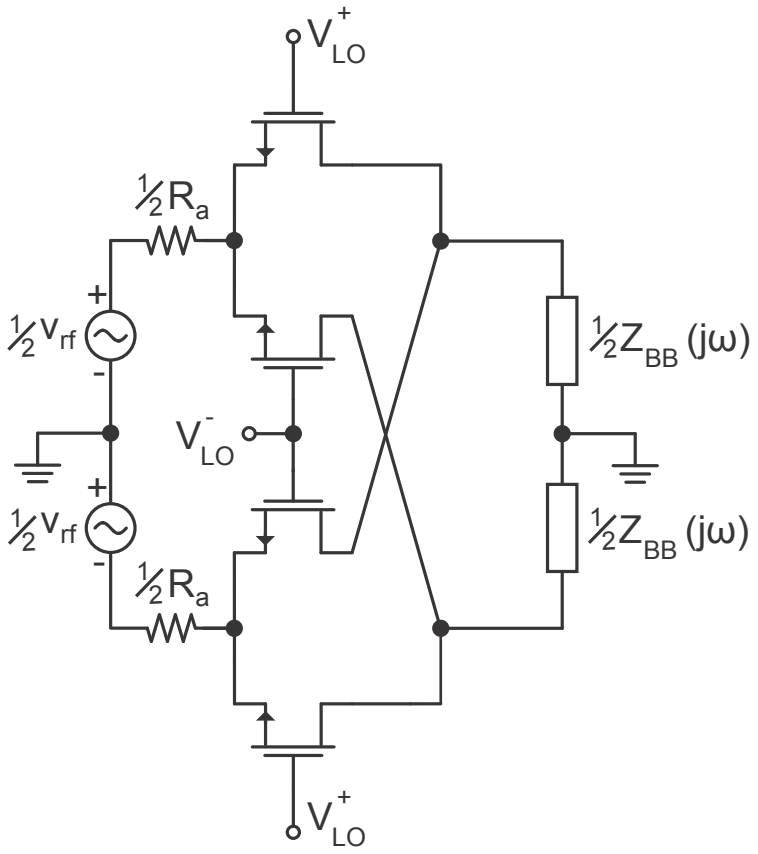


Figure 6.3. Schematic of fully balanced passive mixer

One way to obtain a lower noise figure is to employ inductive degeneration as in the case of a low noise amplifier. Under this scenario, the optimum noise figure is obtained and can be calculated by finding the minimum value of (6.3). The optimum antenna impedance $R_{a,opt}$ is calculated to be

$$R_{a,opt} = R_g\sqrt{1+\left(\frac{f_{max}}{f_0}\right)^2\left(\frac{4}{\gamma g_m r_o}\right)} \tag{6.5}$$

We must note from (6.5) that the operating frequency f_0 is higher than the f_{max} of the device and hence the first term cannot be ignored as is usually done in conventional analysis where $f_0 \ll f_{max}$. Using the technology parameters as above, the optimum antenna impedance $R_{a,opt} = 1.13R_g$. Using this expression in (6.3), the noise factor in this case is calculated to be $NF = 15.14\,\text{dB}$ which is only slightly better than the previous case.

From the above analysis, we conclude that the noise figure of an active mixer is high and would potentially degrade the performance of the receiver. The intuition behind this result is the following. Since the device is operating beyond the maximum oscillation frequency and close to the device cut-off frequency, there is no gain from the RF device. Hence, the

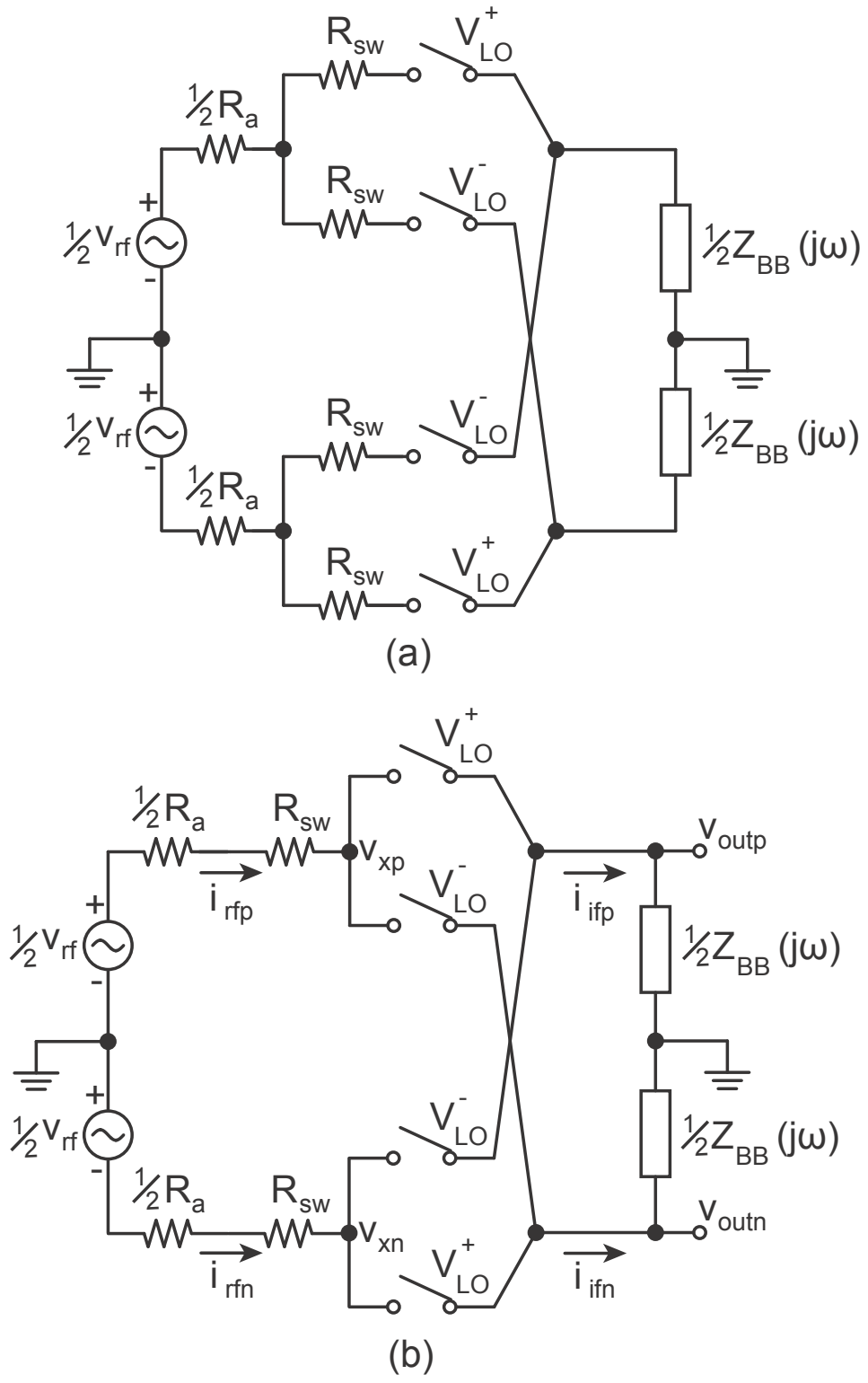


Figure 6.4. Switch model of fully balanced passive mixer

input noise and the gate resistance noise are attenuated through the RF device. However, the inherent current noise of the RF device adds directly at its drain node. Hence, its noise referred back to the input is amplified due to no available gain at this frequency. Therefore, the noise figure is degraded. Another potential disadvantage of using an active mixer is with regard to its conversion gain. The drain node of the RF device (source node of the LO devices) has a bandwidth of $f_T/2$ and hence has a filtering effect on the input current signal injected by the RF device. Thus, only a part of the signal current is switched by the LO devices and thus degrading the conversion gain of the mixer. This gain can be improved by resonating the capacitance at this node using an inductor. However, this results in complicated layout and modeling issues at this frequency.

6.1.2 Sub-Terahertz Passive Mixer

We now explore the feasibility of a passive mixer for this receiver architecture. Fig. 6.3 shows the schematic of a fully balanced passive mixer. It consists of four transistors operating as switches. The transistors are driven by high swing LO signals that down-convert the RF signal v_{rf} fed from the antenna (with impedance R_a). The resulting IF signal is then filtered using the baseband impedance Z_{bb}. To get an analytical expression for the conversion gain, consider the circuit shown in Fig. 6.4(a). Here the transistor is modeled with a switch resistance R_{sw} and is driven by complimentary square wave signals ${V_{LO}}^+ = A_{LO}s(t)$ and ${V_{LO}}^- = A_{LO}\overline{s(t)}$. Here A_{LO} is the amplitude of the switching waveform and

$$s(t) = 0.5 + \frac{2}{\pi}\left[\sin(\omega_{LO}t) + \frac{1}{3}\sin(3\omega_{LO}t) + \frac{1}{5}\sin(5\omega_{LO}t) + \dots\right] \tag{6.6}$$

and

$$\overline{s(t)} = 0.5 - \frac{2}{\pi}\left[\sin(\omega_{LO}t) + \frac{1}{3}\sin(3\omega_{LO}t) + \frac{1}{5}\sin(5\omega_{LO}t) + \dots\right] \tag{6.7}$$

where ω_{LO} is the LO fundamental frequency. The circuit in Fig. 6.4(a) can be simplified to that in Fig. 6.4(b) by placing the switch resistance R_{sw} before the ideal switches. The baseband impedance Z_{BB} could either be purely capacitive or an RC filter. Typical analysis of this circuit involves a steady state charge based approach as in [65]. This analysis assumes that the baseband bandwidth is small so that the charge lost by the capacitor in every cycle is compensated by the charge flowing through the switches. However, in this design the baseband bandwidth is large ($\sim 10\,\text{GHz}$) and we need to accurately calculate the conversion gain. The analysis of a single balanced structure is complicated and requires frequency domain analysis. However, if we consider the fully balanced structure and consider the differential signals as shown below, a closed form expression for the conversion gain can be obtained. The voltages v_{xp} and v_{xn} are given as

$$v_{xp} = v_{outp}s(t) + v_{outn}\overline{s(t)} \tag{6.8}$$

$$v_{xn} = v_{outp}\overline{s(t)} + v_{outn}s(t) \tag{6.9}$$

The RF currents i_{rfp} and i_{rfn} are given as

$$i_{rfp} = \frac{0.5v_{rf} - v_{xp}}{0.5R_a + R_{sw}} \tag{6.10}$$

$$i_{rfn} = \frac{-0.5v_{rf} - v_{xn}}{0.5R_a + R_{sw}} \tag{6.11}$$

The IF currents i_{ifp} and i_{ifn} are given as

$$i_{ifp} = i_{rfp}s(t) + i_{rfn}\overline{s(t)} \tag{6.12}$$

$$i_{ifn} = i_{rfp}\overline{s(t)} + i_{rfn}s(t) \tag{6.13}$$

Combining (6.8)-(6.13), the differential IF current $i_{if} = \frac{i_{ifp} - i_{ifn}}{2}$ is given as

$$i_{if} = \frac{1}{2}\left[\frac{v_{rf}}{0.5R_a + R_{sw}}(s(t) - \overline{s(t)}) - \frac{v_{out}}{0.5R_a + R_{sw}}\right] \tag{6.14}$$

Using (6.14), the output voltage is given by the convolution of the IF differential current and the load impedance. In frequency domain, if $v_{rf} = A_{RF}\sin[(\omega_{RF} + \omega_m)t]$, then the baseband output voltage is given as

$$v_{out}(\omega_m) = \frac{1}{\pi}\left[\frac{Z_{BB}(\omega_m)}{0.5R_a + R_{sw} + 0.5Z_{BB}(\omega_m)}\right]A_{RF} \tag{6.15}$$

This is true as long as the baseband impedance filters the high frequency signals that include the up-converted mixer products. Hence, the baseband impedance can be purely capacitive in nature as long as the cut-off frequency is chosen to be lower than the operating LO frequency. The cut-off frequency of this filter is determined by the antenna and switch resistance and the value of chosen capacitance.

The input differential RF current $i_{rf} = \frac{i_{rfp} - i_{rfn}}{2}$ has two frequency components due to up-conversion from baseband. The component at frequency $\omega_{LO} + \omega_m$ is given as

$$i_{rf}(\omega_{LO} + \omega_m) = \frac{1}{2}\left[1 - \frac{4}{\pi^2}\left(\frac{Z_{BB}(\omega_m)}{0.5R_a + R_{sw} + 0.5Z_{BB}(\omega_m)}\right)\right]\left[\frac{A_{RF}}{0.5R_a + R_{sw}}\right] \tag{6.16}$$

and the current at the frequency $\omega_{LO} - \omega_m$ is given as

$$i_{rf}(\omega_{LO} - \omega_m) = -\frac{2}{\pi^2}\left[\frac{Z_{BB}(\omega_m)}{0.5R_a + R_{sw} + 0.5Z_{BB}(\omega_m)}\right]^*\left[\frac{A_{RF}}{0.5R_a + R_{sw}}\right] \tag{6.17}$$

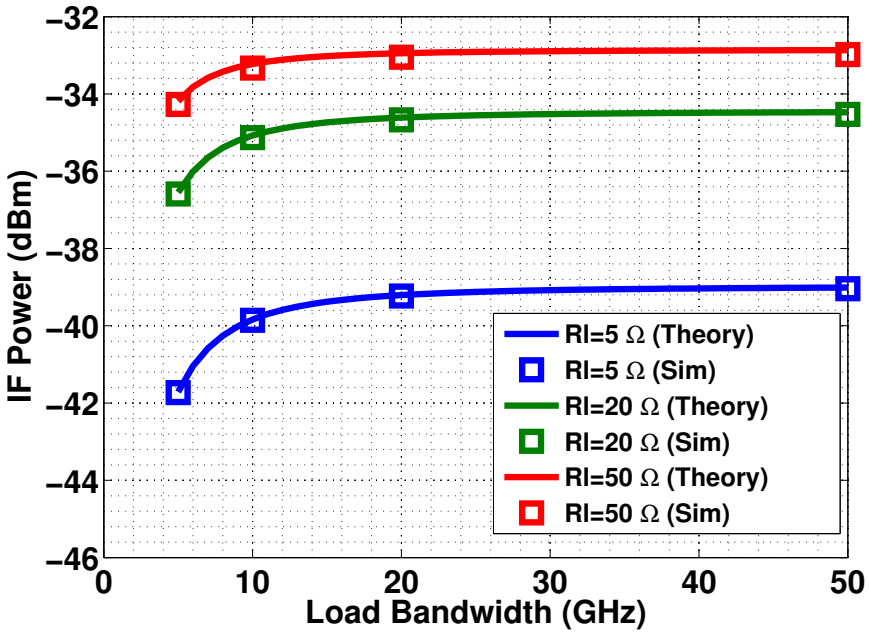


Figure 6.5. Variation of IF power as a function of IF bandwidth for the passive mixer using the switch model

Thus, the RF input impedance $R_{in,rf}$ is given as

$$R_{in,rf}(\omega_{LO}+\omega_m) = \frac{R_a + 2R_{sw}}{1 - \frac{4}{\pi^2}\left[\frac{Z_{BB}(\omega_m)}{0.5R_a+R_{sw}+0.5Z_{BB}(\omega_m)}\right]} \tag{6.18}$$

To verify the above theory, the circuit in Fig. 6.4(b) was simulated for different load resistances R_l. The antenna resistance R_a in this case is 100 Ω and the switch resistance R_{sw} is 25 Ω. An RC load was used for Z_{BB} and the load bandwidth was varied by changing C_l for different R_l values. A low-side injection is used and the RF signal is at an offset of 5 GHz from the LO. Fig. 6.5 shows the plot of the IF power as a function of the load bandwidth. There is good match between the theory and simulation and as expected the IF power drops for bandwidths close to the IF frequency. Fig. 6.6 shows the plot of the RF power as a function of the load bandwidth. We again observe a good correlation between theory and simulation. The RF power is relatively flat with the load bandwidth as evident from (6.18). Here the second term in the denominator is negligible compared to unity and hence the input resistance remains relatively constant.

In the above analysis, we assumed $v_{rf} = A_{RF}\sin[(\omega_{RF}+\omega_m)t]$. However, when the transmitted RF signal is generated by modulating a real baseband waveform, the tones in the RF signal are symmetric about the carrier frequency i.e. every RF signal can be decomposed into a sum of two sinusoidal signal pairs around ω_{RF}. Hence, for analysis we now assume $v_{rf} = A_{RF}\sin[(\omega_{RF}+\omega_m)t] + A_{RF}\sin[(\omega_{RF}-\omega_m)t]$. As the mixer is a linear time varying (LTV) system, we can find the resulting output waveforms by using superposition across different frequencies. Thus, from (6.15), the baseband output voltage is given as

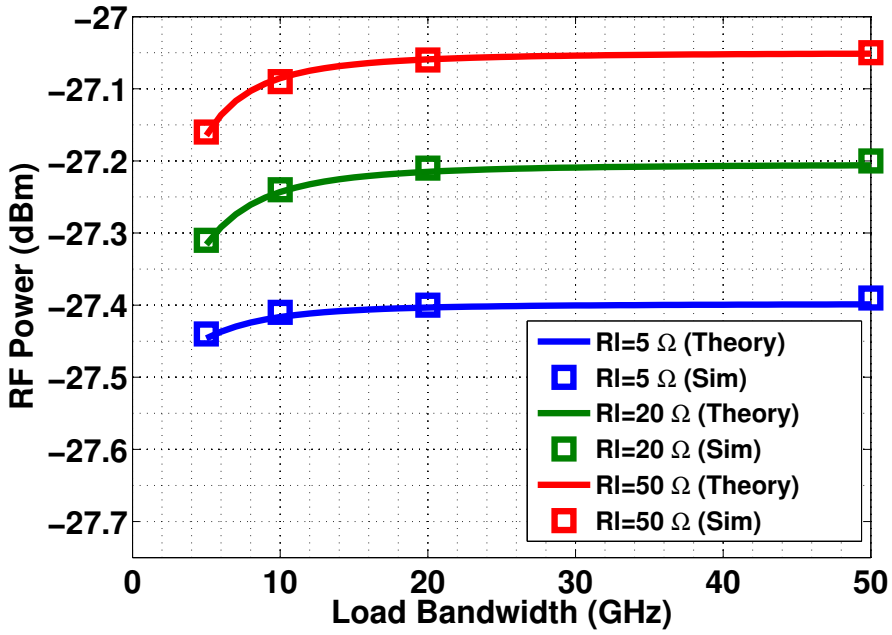


Figure 6.6. Variation of IF power as a function of RF bandwidth for the passive mixer using the switch model

$$v_{out}(\omega_m) = \frac{2}{\pi}\left[\frac{Z_{BB}(\omega_m)}{0.5R_a + R_{sw} + 0.5Z_{BB}(\omega_m)}\right] A_{RF} \tag{6.19}$$

The input differential RF current $i_{rf} = \frac{i_{rfp} - i_{rfn}}{2}$ has two frequency components due to up-conversion from baseband. The component at frequency $\omega_{LO} + \omega_m$ is given as

$$i_{rf}(\omega_{LO} + \omega_m) = \frac{1}{2}\left[1 - \frac{8}{\pi^2}\Re\left(\frac{Z_{BB}(\omega_m)}{0.5R_a + R_{sw} + 0.5Z_{BB}(\omega_m)}\right)\right]\left[\frac{A_{RF}}{0.5R_a + R_{sw}}\right] \tag{6.20}$$

and the current at the frequency $\omega_{LO} - \omega_m$ is given as

$$i_{rf}(\omega_{LO} - \omega_m) = \frac{1}{2}\left[1 - \frac{8}{\pi^2}\Re\left(\frac{Z_{BB}(\omega_m)}{0.5R_a + R_{sw} + 0.5Z_{BB}(\omega_m)}\right)\right]\left[\frac{A_{RF}}{0.5R_a + R_{sw}}\right] \tag{6.21}$$

Thus, the RF input impedance $R_{in,rf}$ seen by each source at $\omega_{LO} + \omega_m$ and $\omega_{LO} - \omega_m$ is given as

$$R_{in,rf}(\omega_{LO} + \omega_m) = R_{in,rf}(\omega_{LO} - \omega_m) = \frac{R_a + 2R_{sw}}{1 - \frac{8}{\pi^2}\Re\left[\frac{Z_{BB}(\omega_m)}{0.5R_a + R_{sw} + 0.5Z_{BB}(\omega_m)}\right]} \tag{6.22}$$

The analysis shown above assumes a square wave LO drive and ideal switching of the transistors. However, due to the high frequency of operation and sinusoidal LO drives, the

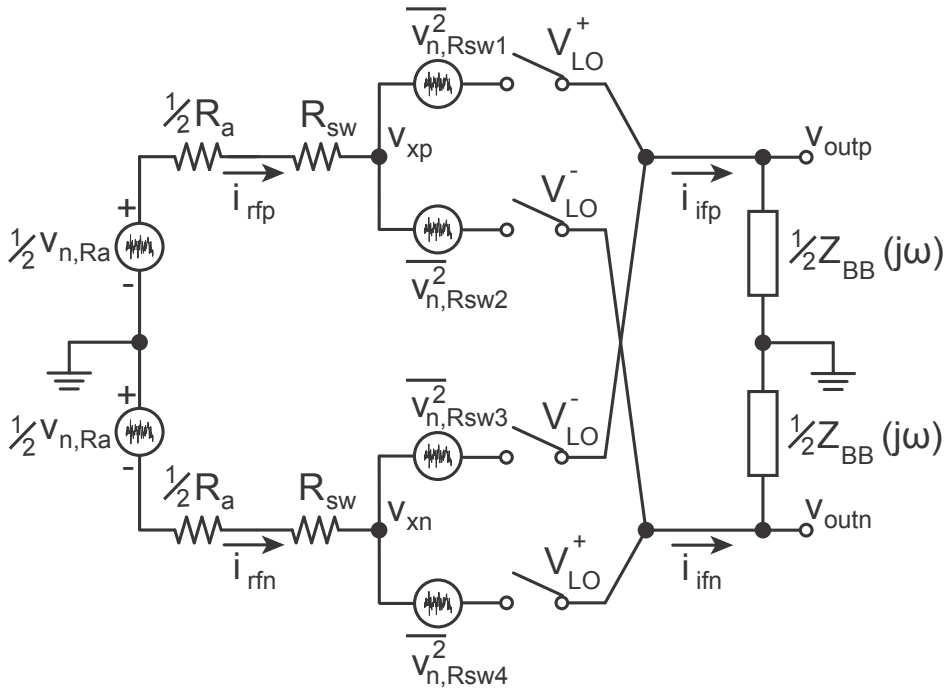


Figure 6.7. Noise analysis of fully balanced passive mixer using the switch model

conversion gain of the mixer is low. The term $8/\pi^2$ in (6.22) is related to the conversion gain of the mixer. Operating at these high frequencies leads to a lower conversion gain and this leads to an input resistance $R_{in,rf} \approx R_a + 2R_{sw}$.

We now need to estimate the noise figure of the passive mixer topology and compare it with the active mixer. Consider the schematic of the passive mixer with the noise sources shown in Fig. 6.7. We will assume that the load impedance Z_{BB} is mostly capacitive in nature and thus its noise contribution can be ignored. Hence, there are mainly two noise sources, one from the antenna impedance (or the input noise source) modeled as v_{n,R_a} and the other from the transistor resistance R_{sw} modeled as $v_{n,R_{sw}}$. In order to simplify the calculation of the conversion gain in Fig. 6.4(b), the switch resistors were combined as a single unit. However, such a simplification is possible only for the switch resistors and not for the individual noise sources as their noise contributions are uncorrelated. In order to calculate the noise figure of the mixer, we follow a procedure similar to the calculation of the conversion gain. We first consider the noise contribution from the switch resistances which means $v_{n,R_a} = 0$.

The voltages v_{xp} and v_{xn} are given as

$$v_{xp} = (v_{n,R_{sw1}} + v_{outp})s(t) + (v_{n,R_{sw2}} + v_{outn})\overline{s(t)} \tag{6.23}$$

$$v_{xn} = (v_{n,R_{sw3}} + v_{outp})\overline{s(t)} + (v_{n,R_{sw4}} + v_{outn})s(t) \tag{6.24}$$

The RF currents i_{rfp} and i_{rfn} are given as

$$i_{rfp} = \frac{-v_{xp}}{0.5R_a + R_{sw}} \tag{6.25}$$

$$i_{rfn} = \frac{-v_{xn}}{0.5R_a + R_{sw}} \tag{6.26}$$

The IF currents i_{ifp} and i_{ifn} are again given as

$$i_{ifp} = i_{rfp}s(t) + i_{rfn}\overline{s(t)} \tag{6.27}$$

$$i_{ifn} = i_{rfp}\overline{s(t)} + i_{rfn}s(t) \tag{6.28}$$

Combining (6.23)-(6.28), the differential IF current $i_{if} = \frac{i_{ifp} - i_{ifn}}{2}$ is given as

$$i_{if} = \frac{1}{2}\left[\frac{-v_{n,R_{sw1}}s(t) + v_{n,R_{sw2}}\overline{s(t)} - v_{n,R_{sw3}}\overline{s(t)} + v_{n,R_{sw4}}s(t)}{0.5R_a + R_{sw}} - \frac{v_{out}}{0.5R_a + R_{sw}}\right] \tag{6.29}$$

As a simplification, we now consider the noise contribution only from the first sideband and compute the noise figure of the mixer. The output noise spectral density due to the switch resistances $S_{vout,R_{sw}}$ is calculated from (6.29) as

$$\begin{aligned} S_{vout,R_{sw}} &\approx 4\left[(0.5)^2 + 2\left(\frac{1}{2}.\frac{2}{\pi}\right)^2\right]\left|\frac{0.5Z_{BB}(\omega)}{0.5R_a + R_{sw} + 0.5Z_{BB}(\omega)}\right|^2(4kTR_{sw}) \\ &= (1 + 8/\pi^2)\left|\frac{0.5Z_{BB}(\omega)}{0.5R_a + R_{sw} + 0.5Z_{BB}(\omega)}\right|^2(4kTR_{sw}) \end{aligned} \tag{6.30}$$

The factor of 1/2 is due to the sinusoidal multiplication and the factor of 2 is due to two sidebands (signal and image bands). The output noise spectral density due to the input $S_{vout,R_{sw}}$ is calculated using the baseband voltage expression in (6.15) and is given as

$$S_{vout,R_a} \approx \left(\frac{1}{2}.\frac{4}{\pi}\right)^2\left|\frac{0.5Z_{BB}(\omega)}{0.5R_a + R_{sw} + 0.5Z_{BB}(\omega)}\right|^2(4kTR_a) \tag{6.31}$$

Hence, the noise factor F is calculated to be

$$F \approx 2 + (2 + 0.25\pi^2)\frac{R_{sw}}{R_a} \tag{6.32}$$

From (6.18), if $|Z_{BB}(\omega_m)| \gg |0.5R_a + R_{sw} + Z_{BB}(\omega_m)|$ which is usually true given a purely capacitive load at the IF stage, the RF input impedance is given as

$$R_{in,rf}(\omega_{LO}+\omega_m) \approx \frac{R_a + 2R_{sw}}{1-\frac{4}{\pi^2}} \tag{6.33}$$

For conjugate matching $R_{in,rf} = 2R_a$, which gives $R_a = 10.56R_{sw}$. Using this value in (6.32), the noise figure NF is calculated to be $NF = 10\log_{10}(F) = 3.84\,\text{dB}$. In actual practice, the LO waveforms are not exactly square wave in nature and this results in a higher switch resistance, lower conversion gain, a higher noise figure and an optimum relation of $R_a/R_{sw} < 10.56$ which is easier to realize on chip. From the above analysis, we conclude the following

1. With regard to noise figure, the performance of a passive mixer is much better compared to an active one when the operating frequency is greater than the f_{max} of the device.
2. Since the employed topology is a direct conversion architecture, a large voltage conversion gain is desired. In this case, a peak conversion gain of $2/\pi$ can be achieved.
3. The analysis is based on a lot of simplifying assumptions which allow us to make a choice of the topology. In actual practice however, the LO drive signals are sinusoidal in nature and complete electromagnetic simulations and extracted parasitic models must be utilized to design the passive mixer.

6.1.3 240 GHz Passive Mixer Design

Fig. 6.8 shows the schematic of the mixer including the antenna interface and the baseband amplifier. It consists of a fully balanced structure with the baseband outputs capacitively coupled to a common source amplifier stage. Each transistor based switch is implemented as a triple well device for better isolation. A device size of $10\,\mu$m is used for all transistors. This size is chosen based on the available LO power and the minimum inductance realizable on the chip at these frequencies. The switches are biased at a DC voltage of 400 mV and are driven by LO signals with a power level of -3 dBm (LO swing of 400 mV). The bias voltage depends on two factors namely the switch resistance and the turn-off capability of the switch. Using a higher DC bias allows one to obtain a lower on-resistance. However, as the LO swing is limited, the switch does not turn off easily. Hence, given a fixed LO swing (which is determined by the tripler output power), there exists an optimum bias point that maximizes the conversion gain of the mixer. As the antenna is implemented on chip, the mixer is designed in tune with the antenna to obtain the best trade-off between conversion gain and noise figure. The variation of the mixer noise figure and voltage conversion gain as a function of the LO power is shown in Fig. 6.9. The mixer achieves a simulated peak gain of -3 dB and a SSB noise figure of 12 dB with -3 dBm LO power at 240 GHz.

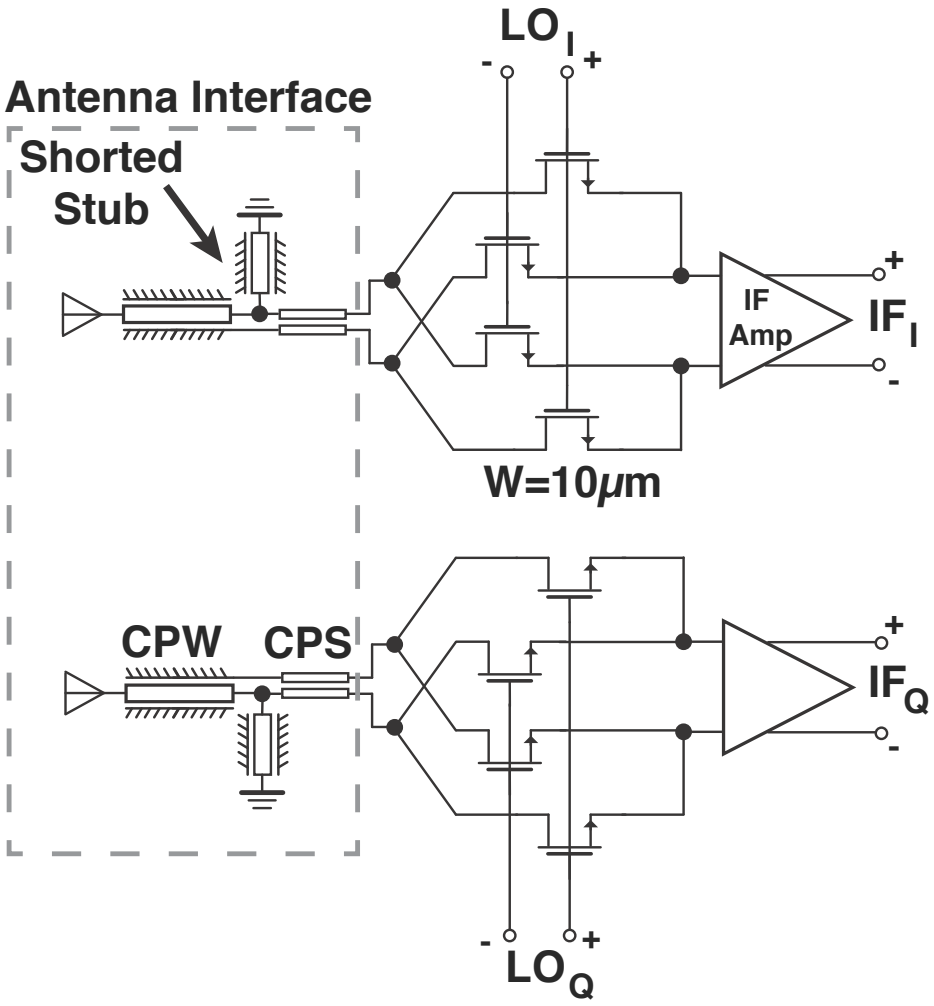


Figure 6.8. Schematic of the passive mixer with the antenna interface

6.1.4 240 GHz In-phase/Quadrature Phase Generation

The required LO signal for the mixer is generated by the 240 GHz tripler in the LO chain. The tripler is interfaced to the 80 GHz LO generation blocks using the power amplifier and driver stages. For accurate demodulation of the received data, the phase mismatch between the I and Q LO signals must be minimized. Hence, this design uses in-phase/quadrature generation using passive networks. This network is implemented just before the mixer to minimize any I/Q mismatch. Fig. 6.10 shows the passive network layout used for I/Q generation. The capacitive impedance seen at the gate of the mixer is transformed into a real impedance of 118 Ω using transformer networks. On the secondary side (mixer side), the top two thick metal layers are utilized to split the LO signals symmetrically. These are then used to drive the four LO ports of each mixer. Using a transformer network also allows one to conveniently bias the mixer gate node at the required potential. The transformer primary and secondary diameters are 16 μm and 13 μm respectively with a trace width of

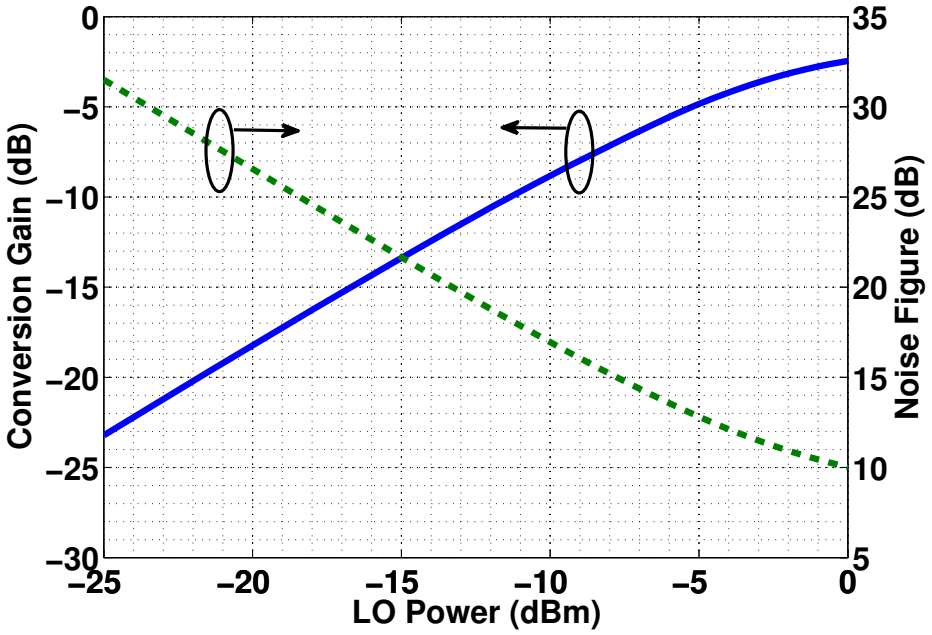


Figure 6.9. Simulated voltage conversion gain and noise figure as a function of the LO power

3 μm each. The transformer is then interfaced to coplanar striplines (CPS) with a characteristic impedance of 118 Ω and loss of 3.1 dB/mm. The trace width is 2 μm and the spacing between the lines is 4 μm. The lines are then connected in parallel and driven by the tripler. In order to achieve the quadrature signal, one leg has an additional length of $\lambda/4$, where λ is the wavelength. The CPS lines are implemented using the top two thick metal layers. The passive structure is surrounded by Metal1/Metal2 ground plane and characterized using full wave electromagnetic simulations. The structure has a simulated loss of 2.5 dB at 240 GHz in the LO path. The in-phase and quadrature LO outputs have a magnitude difference of 1 dB and a phase difference of 89.91° at 240 GHz. The IF outputs from the mixer are tapped in the lower strapped metal layers to minimize its coupling with the LO signals. Using strapped layers minimizes the resistance of the IF path and avoids noise and bandwidth penalty. The asymmetric crossing of the top metal layers however introduces mismatch in the LO drive signals and causes imbalance in the IF outputs. As the baseband amplifiers are implemented as fully differential amplifiers, they have a high common mode rejection ratio. Thus, the final output signals are fully differential.

6.2 Choice of the baseband amplifier

The noise figure of the receiver chain is determined by the noise figure of the mixer, its conversion gain and the noise figure of the baseband amplifier. Fig. 6.11 shows two possible circuits which could be used for the amplification of the baseband signal. In Fig. 6.11(a) the

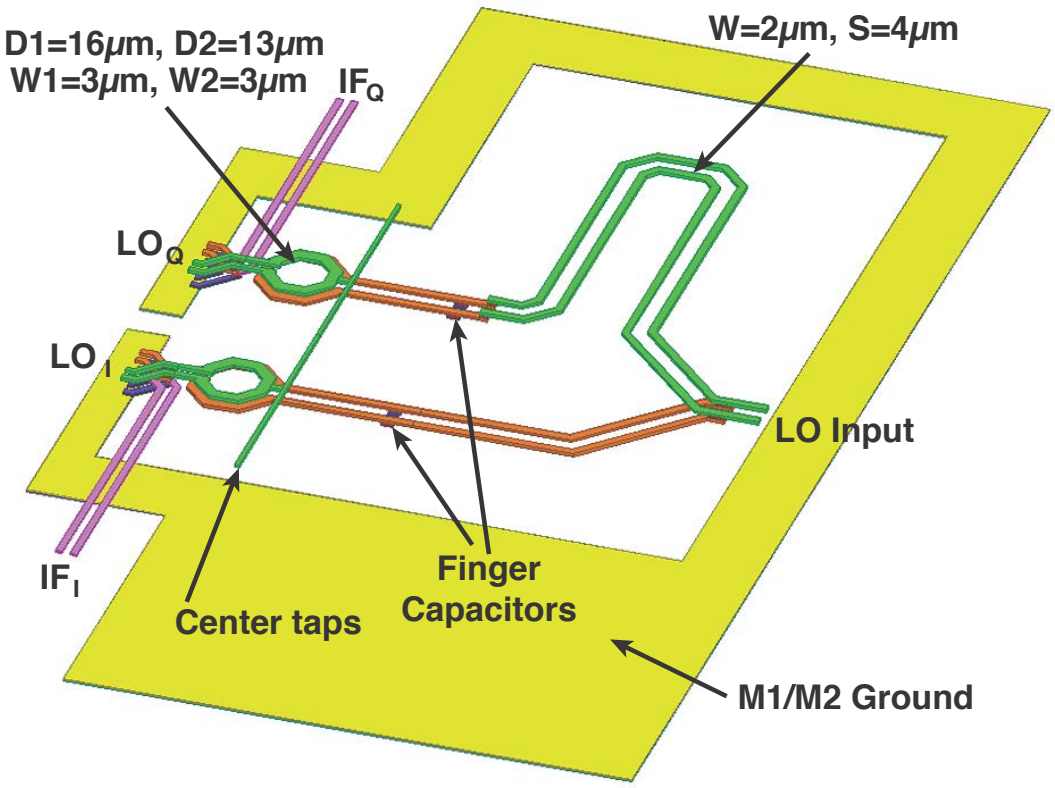


Figure 6.10. 240 GHz I/Q generation and mixer LO matching interface

mixer operates in current mode on the IF side and the IF voltage is generated by passing the signal into a trans-impedance amplifier (TIA). If the mixer is represented as a voltage source with a source resistance R_s, for the trans-impedance amplifier case, the noise spectral density at the output due the input alone ($S_{vo,Rs}$) is given as

$$S_{vo,Rs} = \left[\frac{(1 - g_m R_b)^2}{(1 + g_m R_s)^2}\right] 4k_B T R_s \tag{6.34}$$

where g_m the transconductance of the operational transconductance amplifier (OTA), R_b the feedback resistance, k_B the Boltzmann constant and T the temperature.

Similarly, the noise spectral density at the output due to R_b ($S_{vo,Rb}$) and the OTA ($S_{vo,gm}$) can be calculated as

$$S_{vo,Rb} = \left[\frac{(1 - g_m R_s)^2}{(1 + g_m R_s)^2}\right] 4k_B T R_b \tag{6.35}$$

$$S_{vo,gm} = \left[\frac{(R_s + R_b)^2}{(1 + g_m R_s)^2}\right] 4k_B T \gamma g_m \tag{6.36}$$

where γ is a constant. The noise factor F is thus given as

$$F \approx 1 + \left(\frac{\gamma}{g_m R_s} + \frac{R_s}{R_b} \right) \tag{6.37}$$

where g_m the transconductance of the operational transconductance amplifier (OTA), R_b the feedback resistance and R_s the source resistance looking into the mixer. In order to minimize the noise figure of the baseband amplifier and also increase the TIA gain, the value of R_b must be increased. However, this has a serious penalty on the input bandwidth of the baseband amplifier. To overcome this, the mixer operates in voltage mode in the IF stage and is interfaced to a common source amplifier stage in the baseband as shown in Fig. 6.11(b). In this case, the noise spectral density at the output due the input alone ($S_{vo,Rs}$) is given as

$$S_{vo,Rs} = 4k_B T R_s (g_m R_b)^2 \tag{6.38}$$

Similarly, the noise spectral density at the output due to R_b ($S_{vo,Rb}$) and the OTA ($S_{vo,gm}$) can be calculated as

$$S_{vo,Rb} = 4k_B T R_b \tag{6.39}$$

$$S_{vo,gm} = 4k_B T \gamma g_m {R_b}^2 \tag{6.40}$$

The noise factor F is thus given as

$$F \approx 1 + \frac{\gamma}{g_m R_s} \tag{6.41}$$

Comparing (6.37) and (6.41), the noise figure is lower in the case of a common source amplifier. Additionally, the input bandwidth and the gain of the amplifier stage are not directly related as in the TIA case. For example, the input bandwidth restricts the maximum value of R_b and to further increase the gain of the amplifier one needs to reduce R_s. In the case of a common source amplifier, the gain can be increased either by varying R_b or the g_m of the transistor. This freedom allows the designer to optimize the gain without sacrificing the bandwidth. The input bandwidth in this case would then be determined only by the input capacitance and the sum of the antenna resistance and the mixer switch resistances.

In order to obtain an estimate for the number of stages in the baseband amplifier, we start with a received power of $-50\,\text{dBm}$ at the received antenna (for a range of $2 - 2.5\,\text{cm}$). With a conversion gain of $-10\,\text{dB}$ from the mixer, the received voltage at the baseband amplifier input is $316\,\mu\text{V}$. Therefore, in order to obtain a reasonable voltage swing of $100\,\text{mV}$ at the output, the required gain from the baseband amplifiers is 316 or $50\,\text{dB}$. We also require the overall baseband bandwidth per channel to be around $10\,\text{GHz}$ for $20\,\text{Gbps}$ communication. The number of stages required to obtain the above gain and bandwidth is calculated from (4.4). Given a cascade of common source amplifiers with a required total voltage gain of A_{total} and a given gain-bandwidth product per stage GBW_{stage}, the optimum number of stages N is given as

$$N = \ln(A_{total}) \tag{6.42}$$

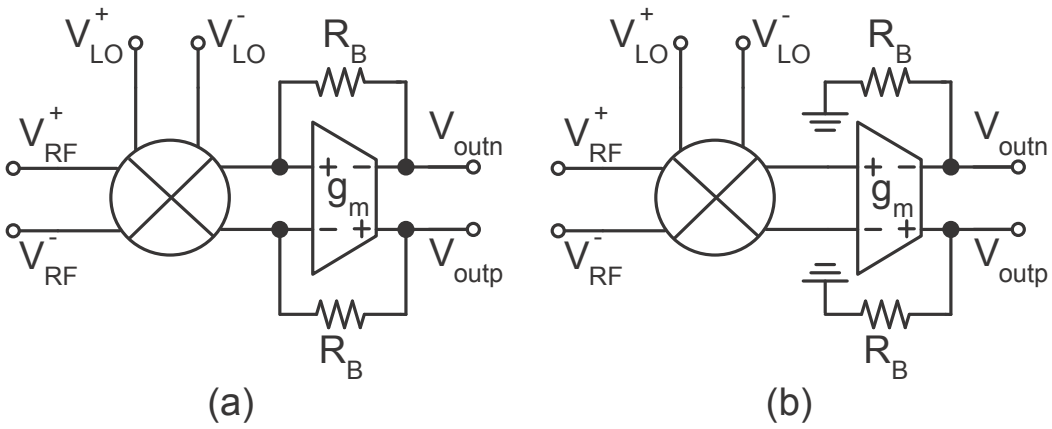


Figure 6.11. 240 GHz I/Q generation and mixer LO matching interface

The gain per stage A_{stage} is equal to $\mathbf{e}$ and the total bandwidth of the amplifier chain BW_{total} is given as

$$BW_{total} = \frac{GBW_{stage}}{\mathbf{e}\ln(A_{total})} \tag{6.43}$$

In this technology, the $GBW_{stage} = 200\,\text{GHz}$ and the required total gain $A_{total} = 316$. Hence, the optimum number of stages $N = 6$ with a gain of 2.61 per stage. The overall bandwidth $BW_{total} = 12.78\,\text{GHz}$. The devices are biased at their peak f_T and majority of the power is allocated for the first stage to reduced the noise figure of the baseband amplifier chain. The successive stages are impedance scaled to minimize the total power.

6.3 Other blocks

The circuit blocks described earlier were part of this thesis work. We now briefly discuss some of the other blocks. The 240 GHz tripler consists of a differential pair with inductive degeneration. This combines the non-linearity of the device along with a power mixer approach to boost the overall conversion gain. The 80 GHz power amplifier (PA) consists of a Class-E output stage with three driver stages. The output stage of the PA is optimized for high efficiency while considering its non-linear effects on the modulated waveform. The 80 GHz QPSK modulator consists of a Gilbert mixer structure where the data is fed on the RF port and the modulated in-phase and quadrature signals are combined in the current domain. The data to the modulator is fed using an on-chip PRBS generator. The PRBS implements a 7-bit sequence and is implemented using a loop unrolled (by a factor of 2) architecture with a cascade of flip-flops. The PRBS has three modes of operation namely continuous wave (CW), BPSK and QPSK. The doubler in the LO path is implemented using a pseudo differential pair bias in Class-B regime. The output current from the differential

pair are combined to generate the required second harmonic. On the receiver side, the baseband amplifiers are implemented using fully differential amplifiers. A total of six stages provides the required gain for detection of the modulated data.

6.4 Measurement Results

The 240 GHz transmitter and receiver chips are fabricated in 65 nm bulk CMOS process without any special options. The microphotograph of the chips is shown in Fig. 6.12. Each chip occupies a die area of 2 mm × 1 mm and the antenna size is 800 μm × 500 μm including the ground plane. The supply voltages and the bias signals are provided through DC pads. The required LO chain and PRBS clock signals are fed using GSG pads. The chips are attached to FR-4 boards using conductive epoxy and all the pads are wire bonded. The required copper plate for the antennas is designed as part of the PCB board. The transmitter and receiver boards are mounted using PCI buses onto a regulator board and are placed in line of sight for testing purposes.

6.4.1 Transmitter Measurements

The transmitter chip is measured first using an external down-converter. Fig. 6.13 shows the measurement setup. An external signal generator feeds the required LO clock at 13.3 GHz. The required data clock is fed through another signal generator and varies from 1.5 to 6 GHz corresponding to a minimum data rate of 3 Gbps and a maximum of 12 Gbps per channel. The radiated 240 GHz modulated signal from the chip is captured by an external WR-3.4 horn antenna and demodulated to baseband using the down-converter. The down-converter operates off the second harmonic of its LO which is fed externally using an ×8 multiplier. The down-converted signal spectrum is then measured using a spectrum analyzer and the eye diagram is captured using a real-time scope. In order to receive the eye diagram, the real-time oscilloscope is triggered using the PRBS data clock. The eye diagram measurement also requires the LO frequencies to be locked to each other. For this purpose, the signal generators feeding the chip LO signal and the multiplier are reference locked to 10 MHz. Since the multiplication factors on the chip and the multiplier are different (18 and 16 respectively), a same reference clock cannot be used for both. This results in frequency drift within the 10 MHz and prevents capture of the eye.

First, a single tone measurement is performed. The LO frequency into the chip is held at 13.3 GHz and the LO frequency for the multiplier is at 14.8 GHz. Fig. 6.14 shows the down-converted spectrum. The received frequency tone is observed at 2.6 GHz matching well with the calculations i.e. 13.3 GHz × 18 − 14.8 GHz × 16 = 2.6 GHz. No other spurious tones were observed and hence this confirms the transmission of the 240 GHz tone. By fixing the position of the chip, its distance from the horn antenna is adjusted and the resulting measured power level is plotted as a function of the distance. Fig. 6.15 shows the measured

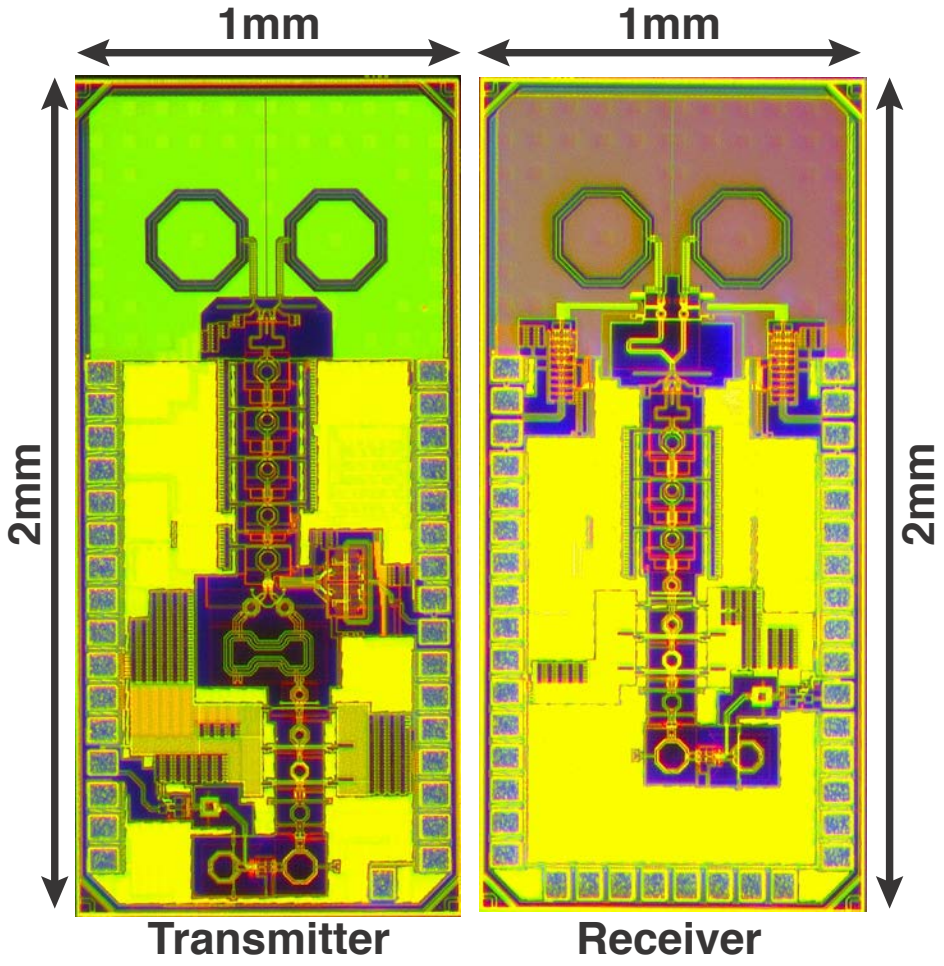


Figure 6.12. Chip microphotograph of the transmitter and receiver

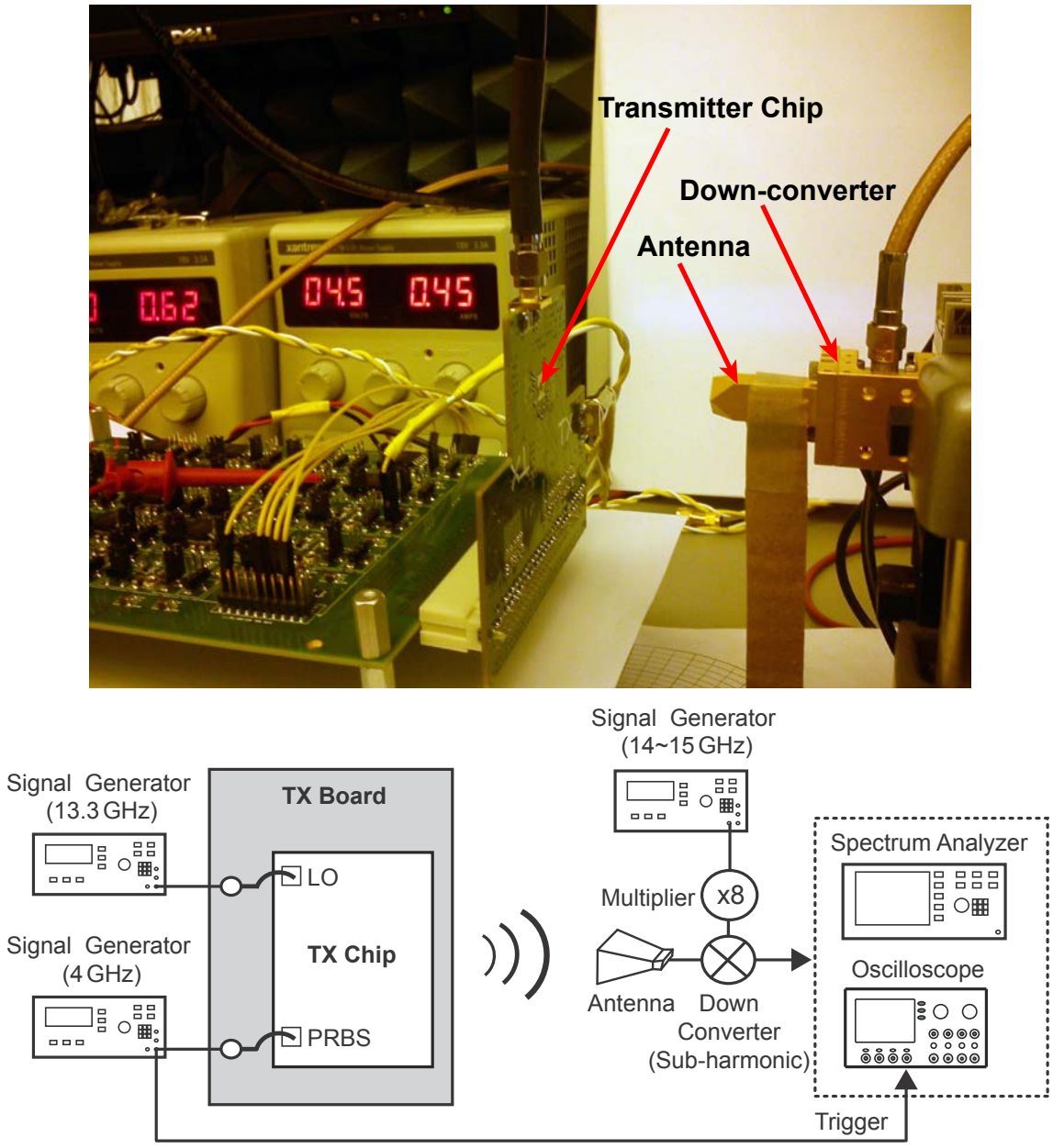


Figure 6.13. Transmitter measurement setup

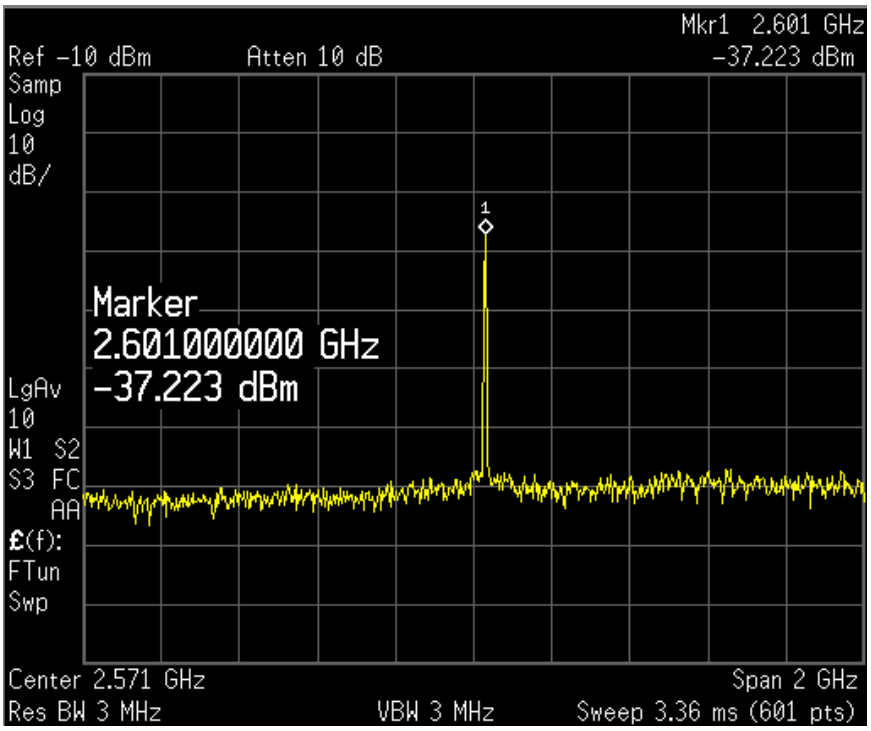


Figure 6.14. Transmitter continuous wave (CW) mode measurement

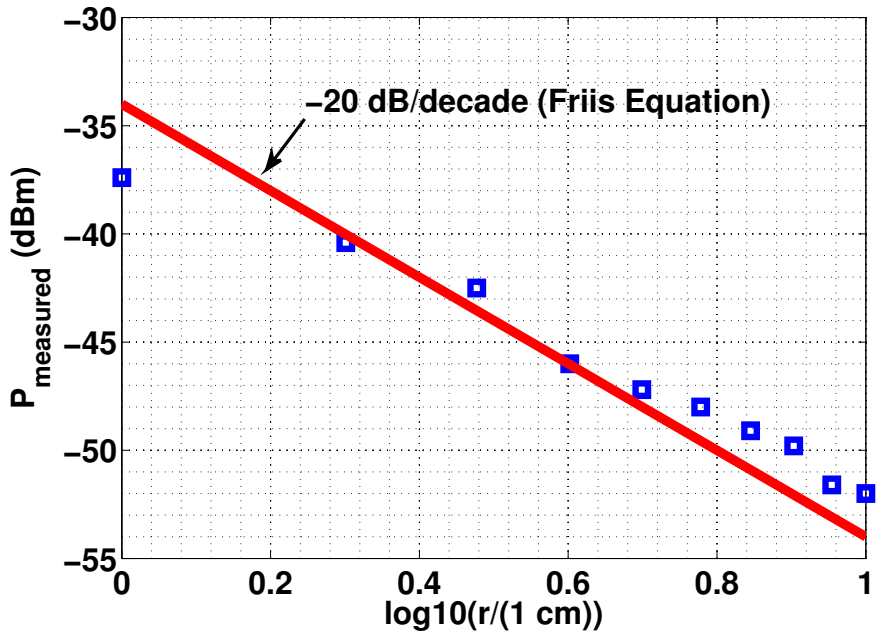


Figure 6.15. Variation of transmitter output power with distance

result. The data points follow the 20 dB per decade slope as predicted by Frii's equation. In terahertz measurements, it is difficult to measure the exact value of the Equivalent Isotropic Radiated Power (EIRP) as it depends on several factors such as alignment of the antenna and the accuracy of measured down-converter parameters. In this case, the horn antenna has a gain 23 dB with a coupling efficiency of about 50% at 240 GHz. The down-converter has a conversion gain of −11 dB. The cables and waveguide interconnects add further losses. Hence, with a measured value of −40 dBm and a path loss of −46 dB at 240 GHz, the approximate EIRP is −2 to 0 dBm.

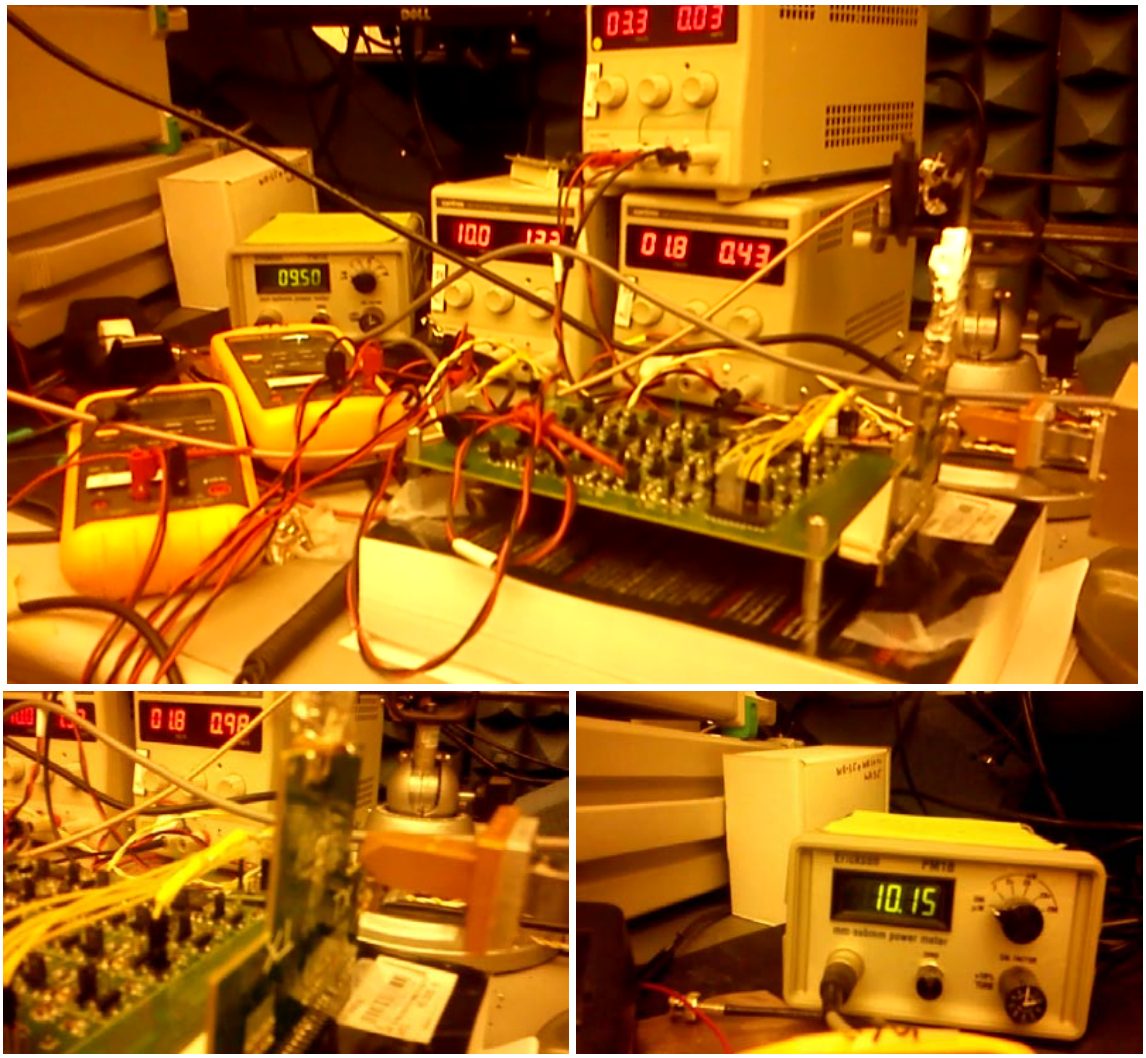


Figure 6.16. Calorimetric measurement of EIRP

A more accurate measurement is performed using the Erickson calorimeter. The WR-3.4 horn antenna is transitioned into a WR-10 waveguide which then interfaces to the calorimeter. The external antenna is placed at a distance of 1 cm from the chip. With the chip turned off, the calorimeter reading is adjusted to read zero. The chip is then turned on and the final reading is measured in the μW scale. Fig. 6.16 shows the results. The measured

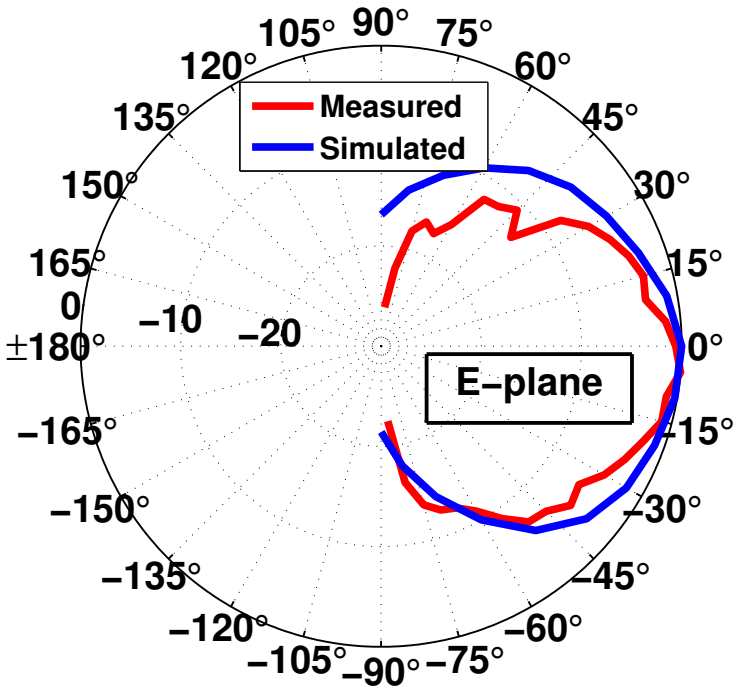


Figure 6.17. Measured and simulated antenna pattern in E-plane

reading is 10.15 μW or -19.93 dBm. With a path loss of -40 dB at 240 GHz, an effective antenna gain of 20 dB and including the cable losses, the EIRP is 0 to 1 dBm.

Next, using the down-converter, the transmitter antenna pattern is measured. The measurement is performed on the E-plane along the Φ axis (azimuthal plane). Fig. 6.17 shows the normalized measured and simulated antenna patterns. The results match very well with simulation. The measured beam width (half-width full maximum (HWFM)) of the antenna is 54°.

The down-converted spectrum of the transmitted signal is measured using a spectrum analyzer. Fig. 6.18 to Fig. 6.27 shows the measured spectrum for data rates 3 Gbps to 12 Gbps. The sinc function is clearly visible for the 3 Gbps measurement shown in Fig. 6.18 and degrades as the data rate is increased. As described earlier, the Pseudo Random Bit Sequence (PRBS) generator generates a 7 bit random sequence. Hence, the waveform has a repetition rate with a beat frequency Δf given by

$$\Delta f = \frac{f_b}{2^7 - 1} \tag{6.44}$$

where f_b is the data rate. For a 3 Gbps data rate, $\Delta f = 23.62$ MHz which is very close to 23.47 MHz shown in Fig. 6.18. Additionally, the location of the first null occurs at 3 GHz. This verifies the operation of the PRBS generator and the entire transmitter chain including

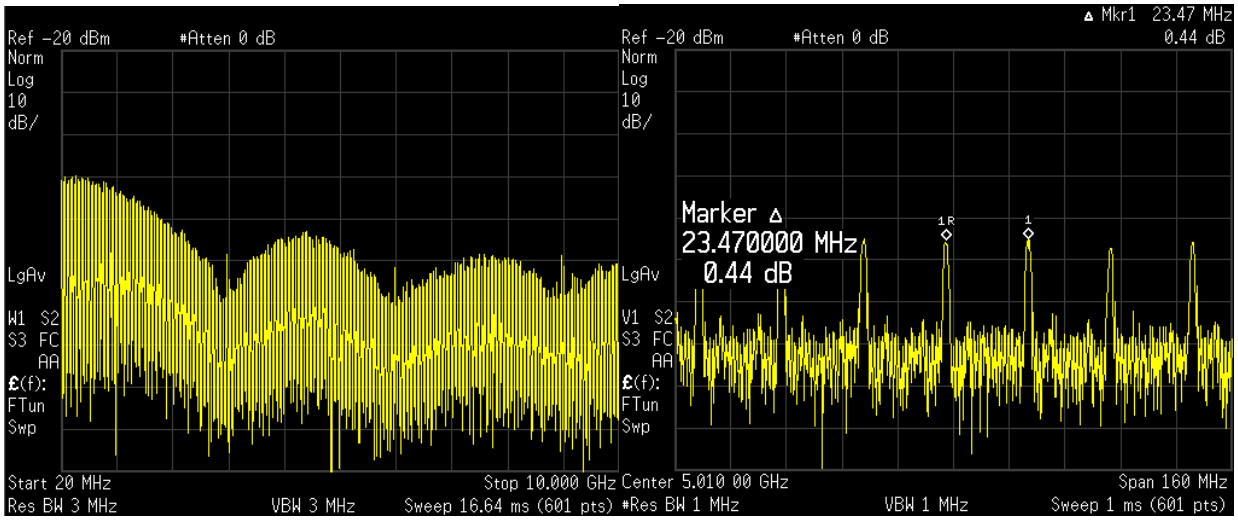


Figure 6.18. Measured down-converted transmitter spectrum and beat frequency for 3 Gbps data

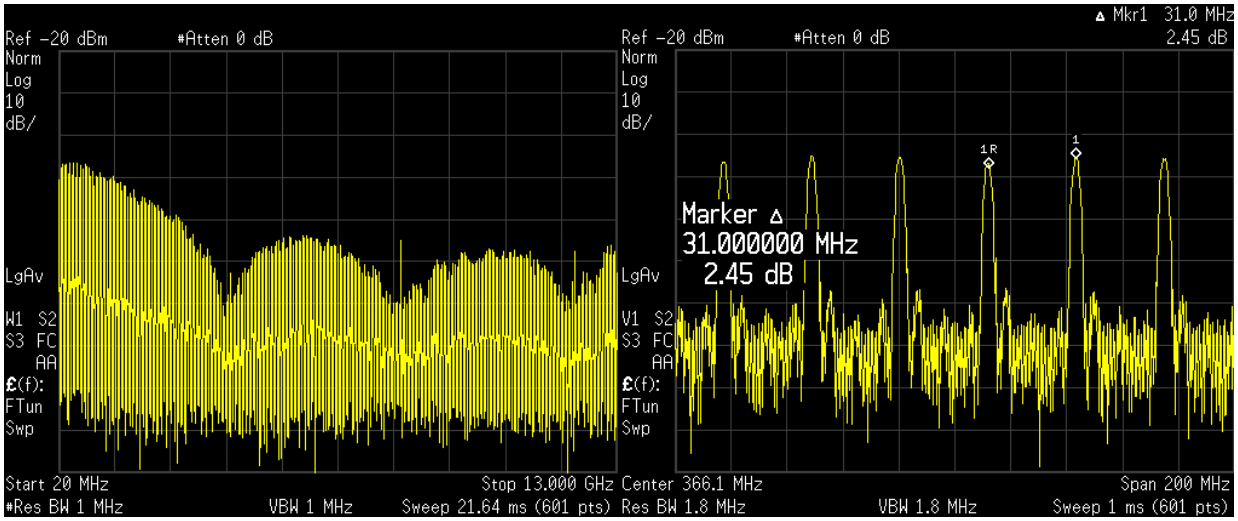


Figure 6.19. Measured down-converted transmitter spectrum and beat frequency for 4 Gbps data

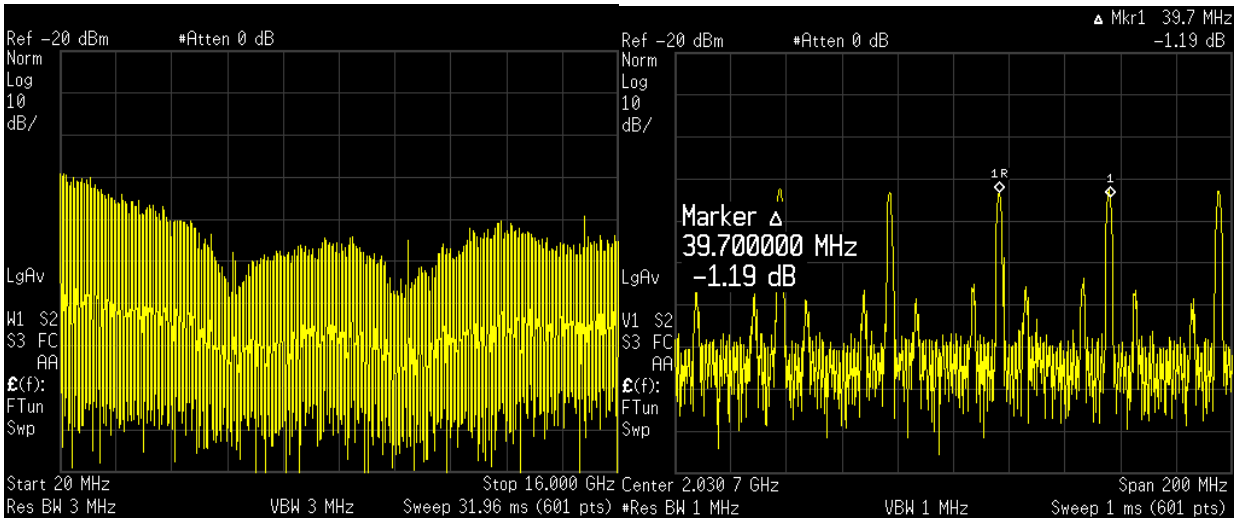


Figure 6.20. Measured down-converted transmitter spectrum and beat frequency for 5 Gbps data

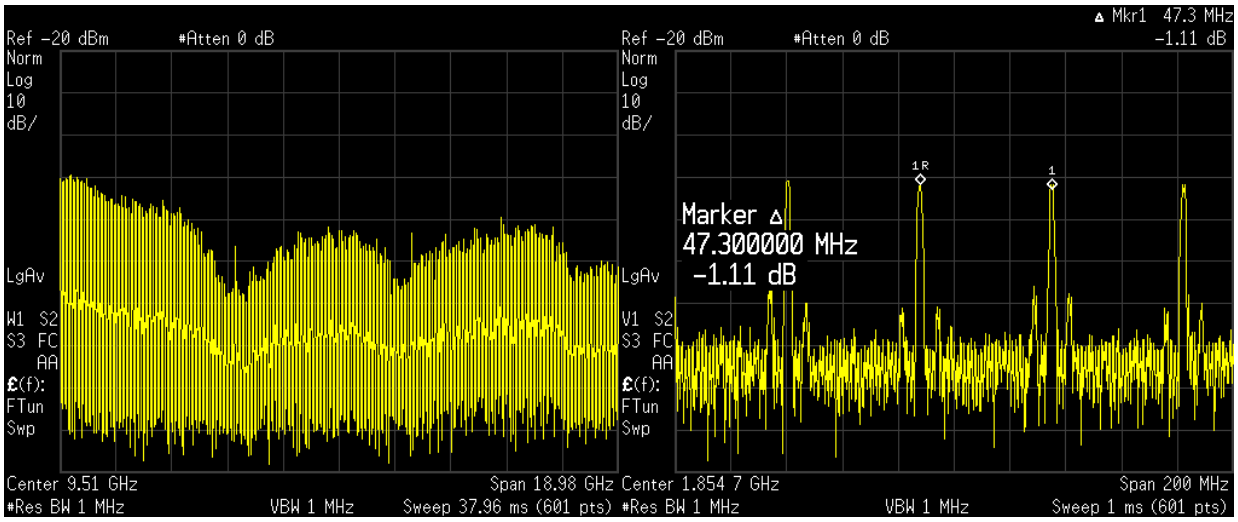


Figure 6.21. Measured down-converted transmitter spectrum and beat frequency for 6 Gbps data

the 240 GHz blocks and the antennas. Measurements at higher data rates also verify the functionality of the transmitter operation. Due to the the finite bandwidth of the transmitter chain, the spectrum starts degrading as one moves to higher data rates. Another issue that prevents clean measurement of the spectrum is the 7^{th} and 9^{th} harmonic leakage of the multiplier. Due to this, multiple copies of the sinc function are down-converted near baseband and start overlapping onto each other. This effect is more pronounced for higher data rates as the null frequency point in this case is at a higher frequency. Nonetheless, the repetition rate is still very close to the calculated value.

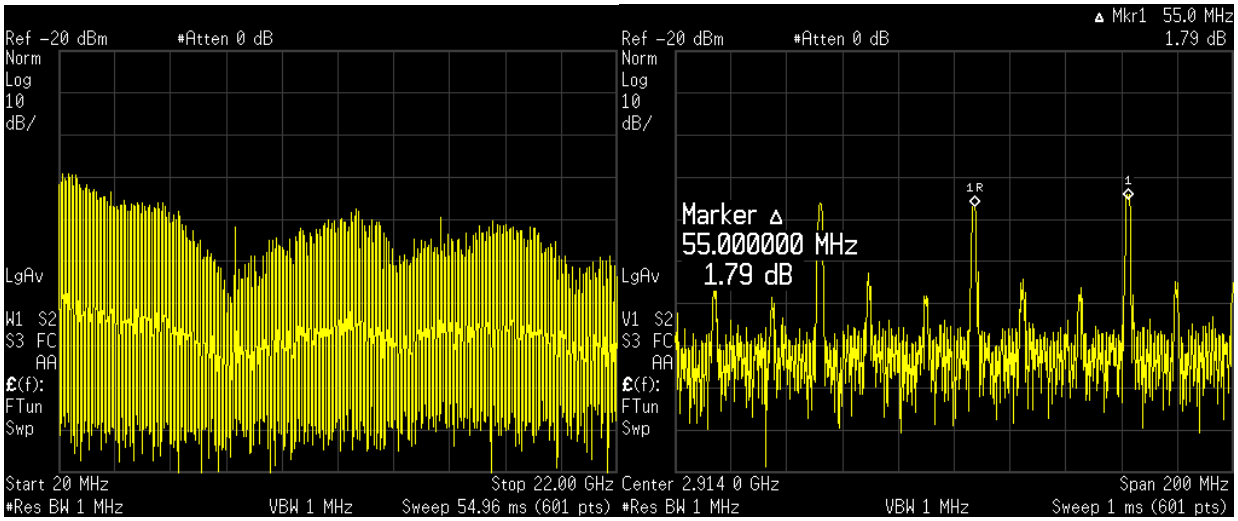


Figure 6.22. Measured down-converted transmitter spectrum and beat frequency for 7 Gbps data

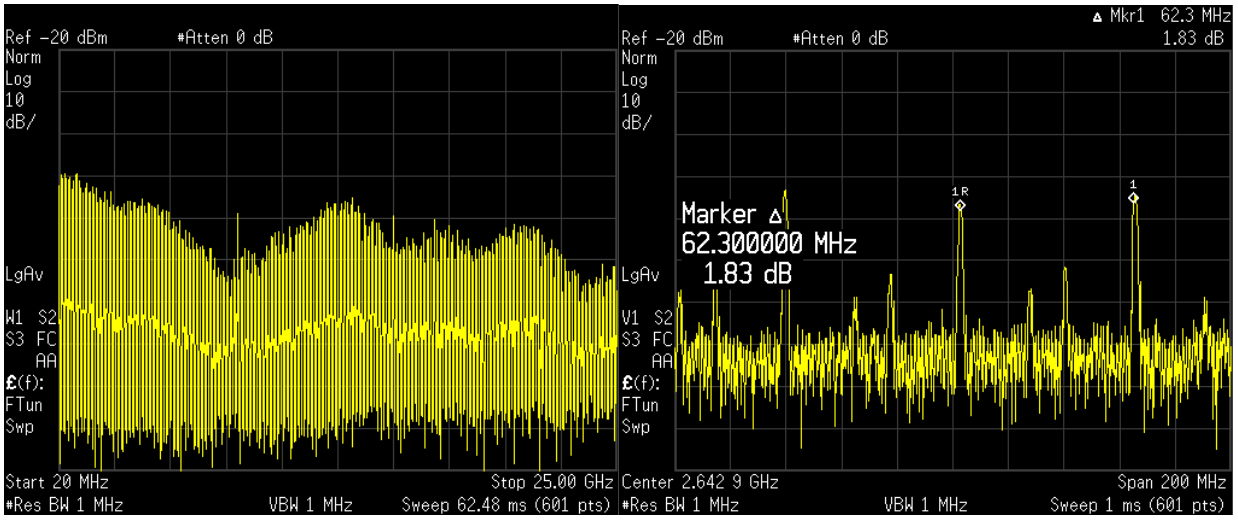


Figure 6.23. Measured down-converted transmitter spectrum and beat frequency for 8 Gbps data

From the above measurement results, it is confirmed that the transmitter can attain a maximum data rate of 12 Gbps per channel. The eye diagram of the down-converted signal

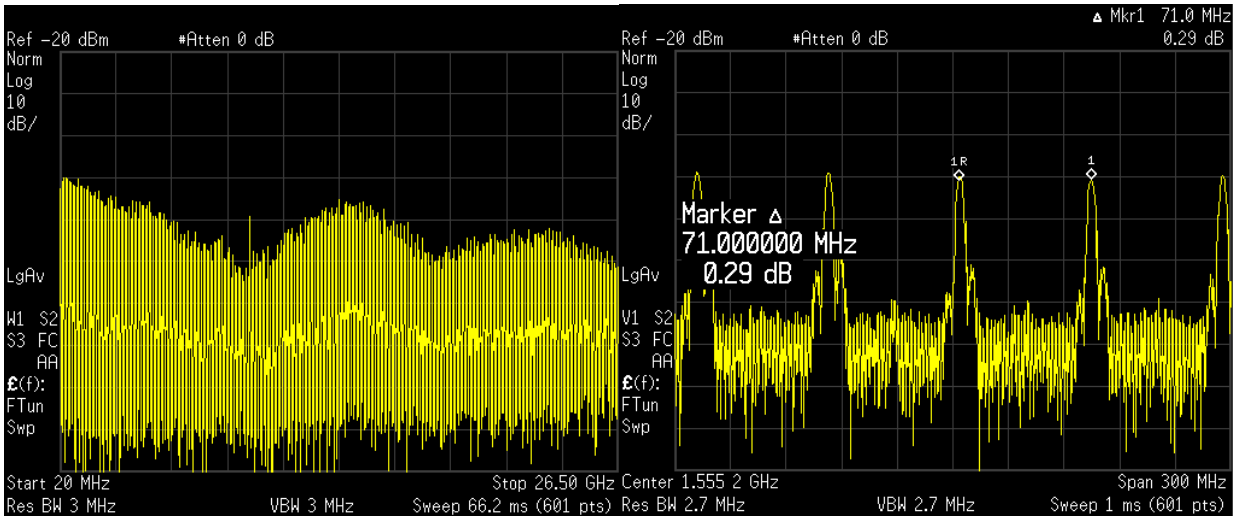


Figure 6.24. Measured down-converted transmitter spectrum and beat frequency for 9 Gbps data

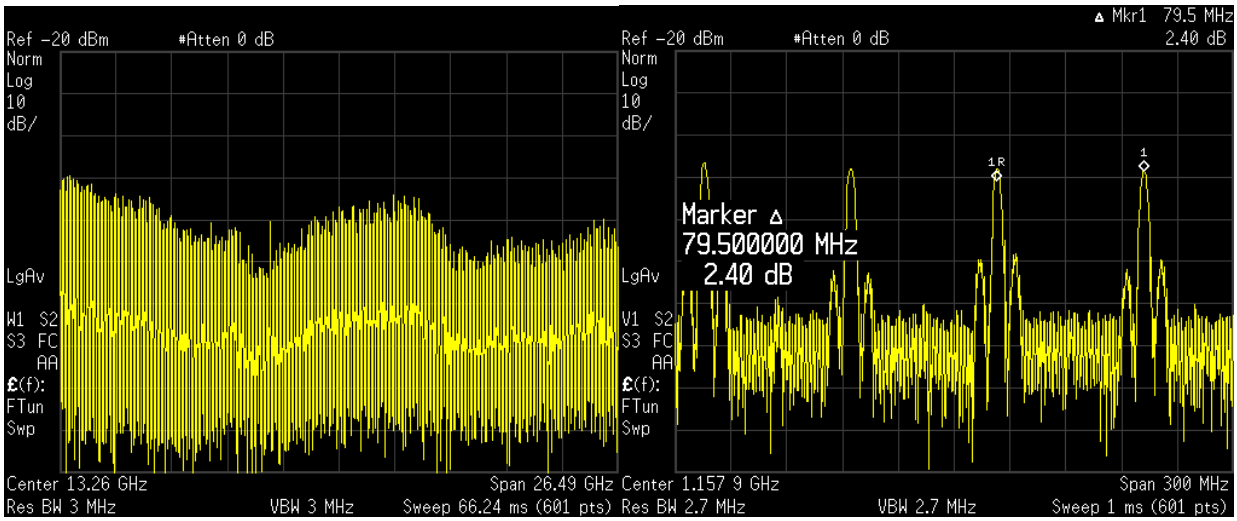


Figure 6.25. Measured down-converted transmitter spectrum and beat frequency for 10 Gbps data

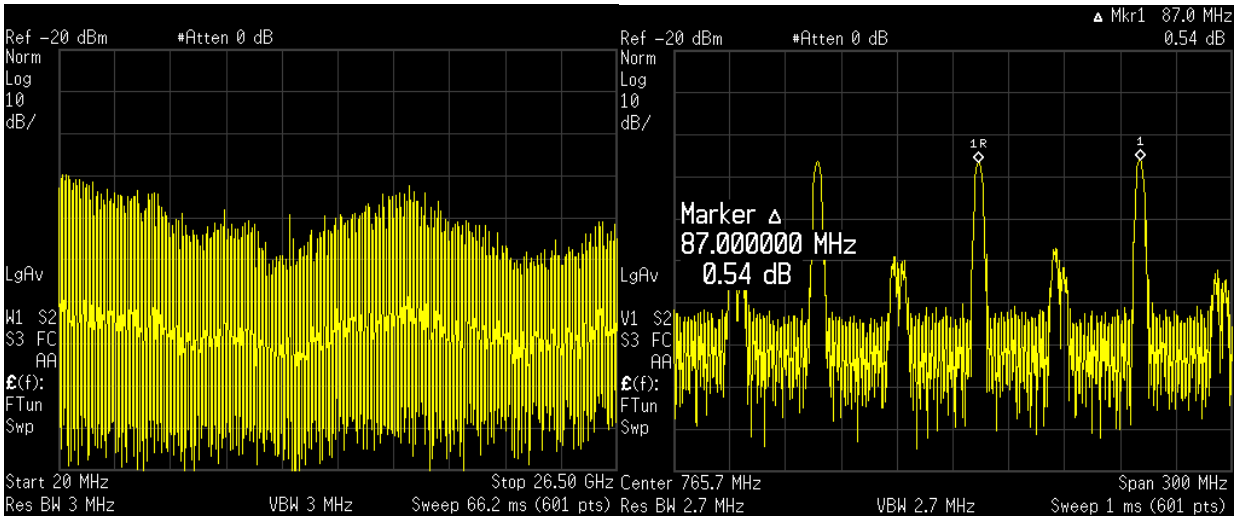


Figure 6.26. Measured down-converted transmitter spectrum and beat frequency for 11 Gbps data

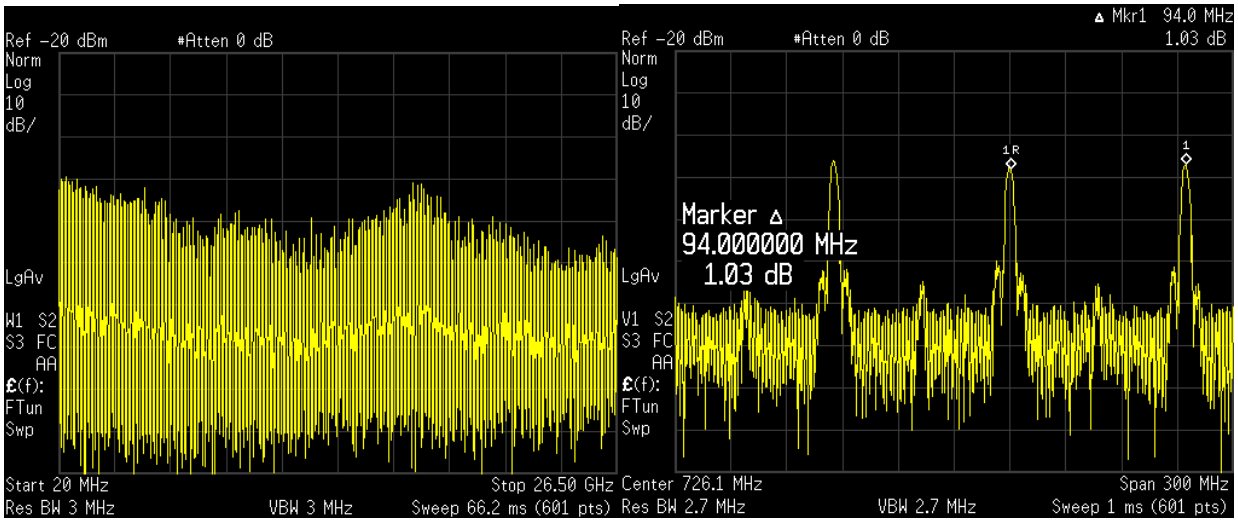


Figure 6.27. Measured down-converted transmitter spectrum and beat frequency for 12 Gbps data

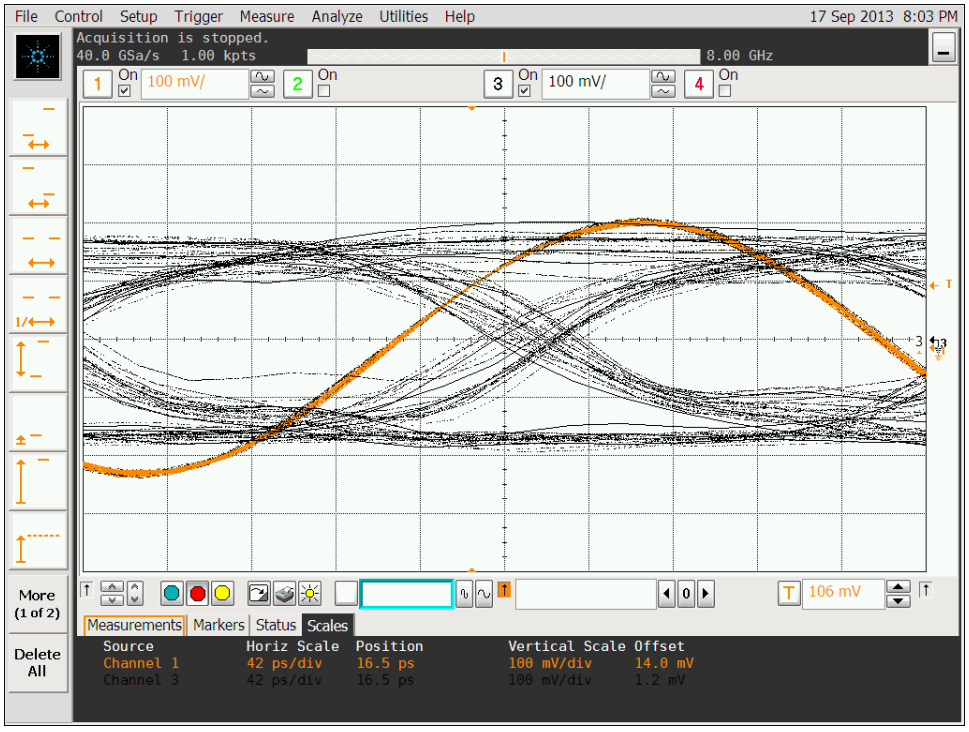


Figure 6.28. Measured transmitter eye diagram for 4 Gbps data

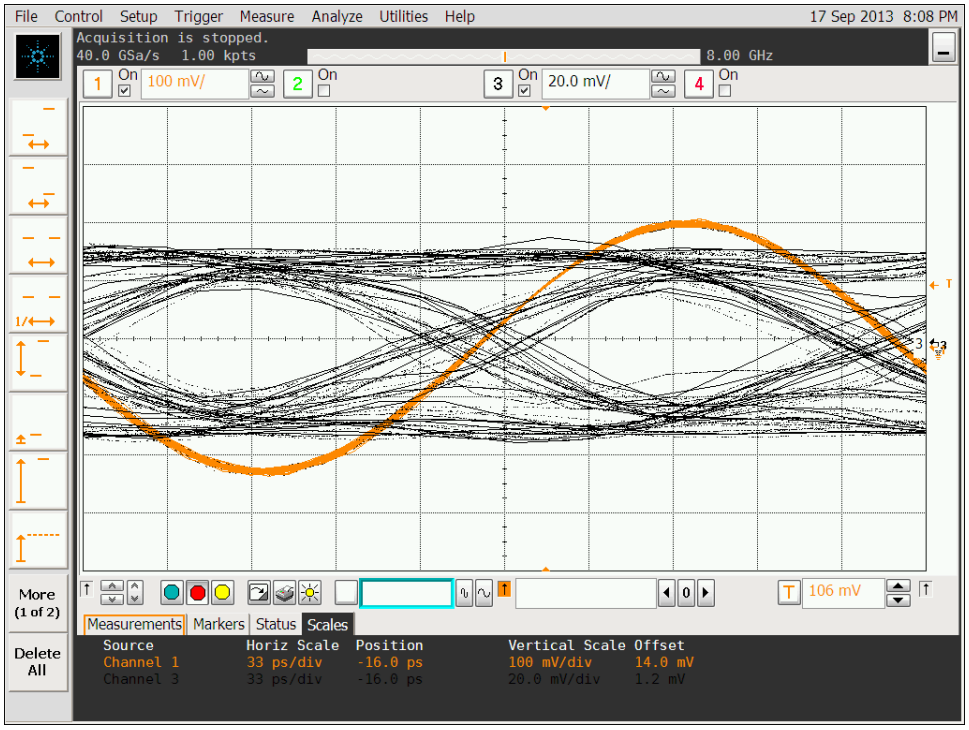


Figure 6.29. Measured transmitter eye diagram for 6 Gbps data

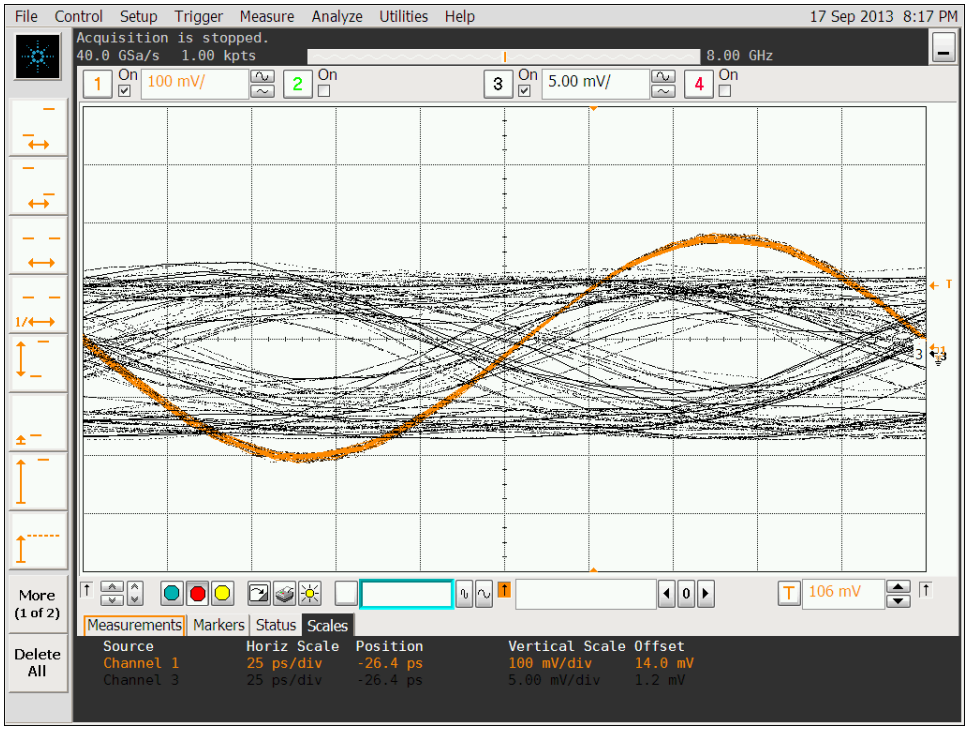


Figure 6.30. Measured transmitter eye diagram for 8 Gbps data

was captured using the real time oscilloscope. As mentioned earlier, in order to obtain a stable eye diagram, the oscilloscope needs to be triggered using the data clock and the LO clocks also need to be frequency locked. In this case, the LO clocks are locked within 10 MHz of each other and this does not allow one to capture the eye for a long time. Additionally, due to the harmonics of the multiplier, the time domain waveform of the down-converted signal is affected. Fig. 6.28, Fig. 6.29, Fig. 6.30 show the measured eye diagrams for 4 Gbps, 5 Gbps and 6 Gbps respectively along with the clock waveforms. The eye remain open for all the measured data rates.

6.4.2 Transmitter-Receiver Wireless Link Measurements

The transmitter and receiver wireless link is tested next to characterize and verify the functionality of the receiver and also the feasibility of data communication at these frequencies. Fig. 6.31 shows the measurement setup. An external signal generator feeds the required LO clock at 13.3 GHz to both the transmitter and receiver chips using a splitter. The required data clock is fed through another signal generator as before. The chips are interfaced using PCI slots and placed vertically facing each other in a line of sight (LOS) communication. The radiated 240 GHz modulated signal from the transmitter is captured by the receiver chip and demodulated to baseband I and Q signals. This signal is then measured using a spectrum analyzer and the eye diagram is captured using a real time oscilloscope.

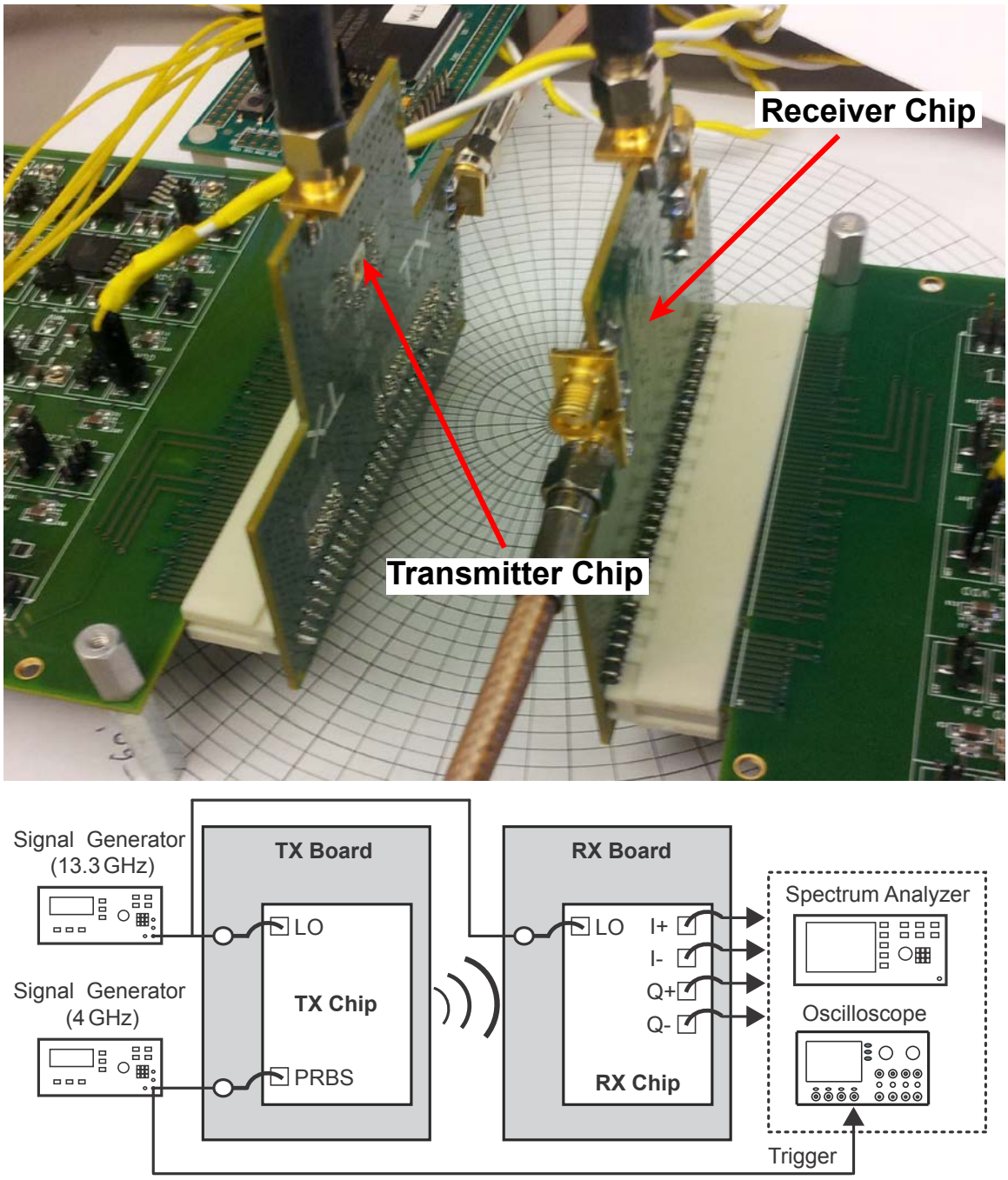


Figure 6.31. Receiver measurement setup

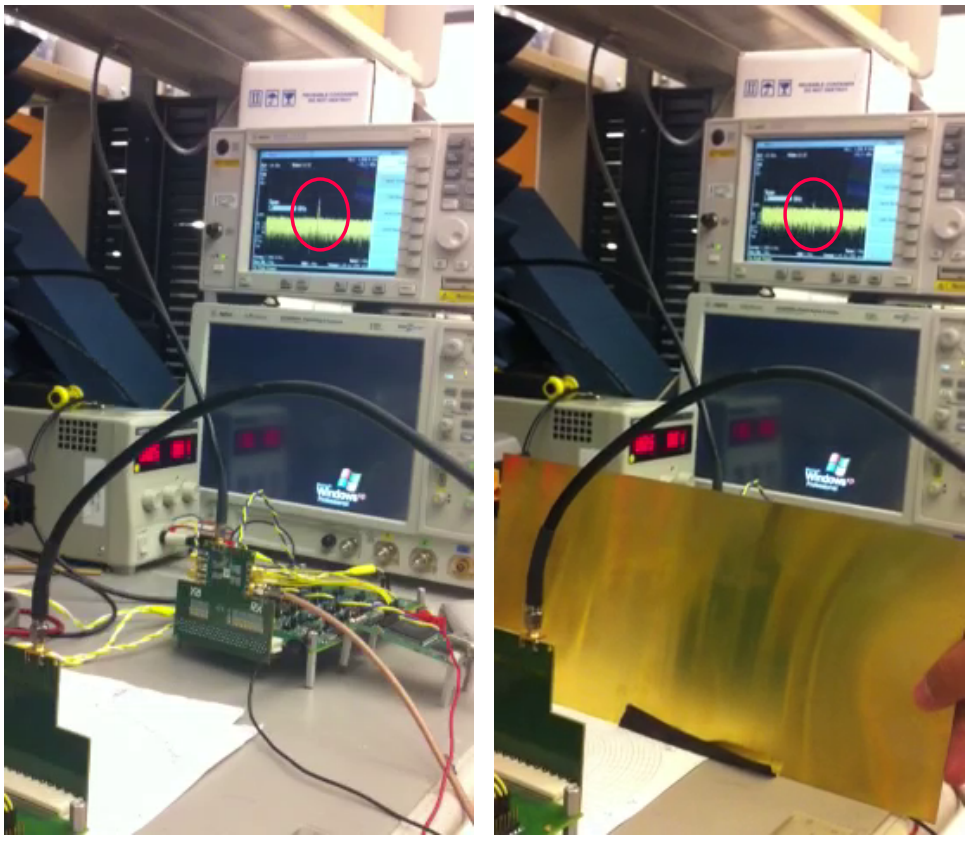


Figure 6.32. Link CW mode measurement with and without reflector

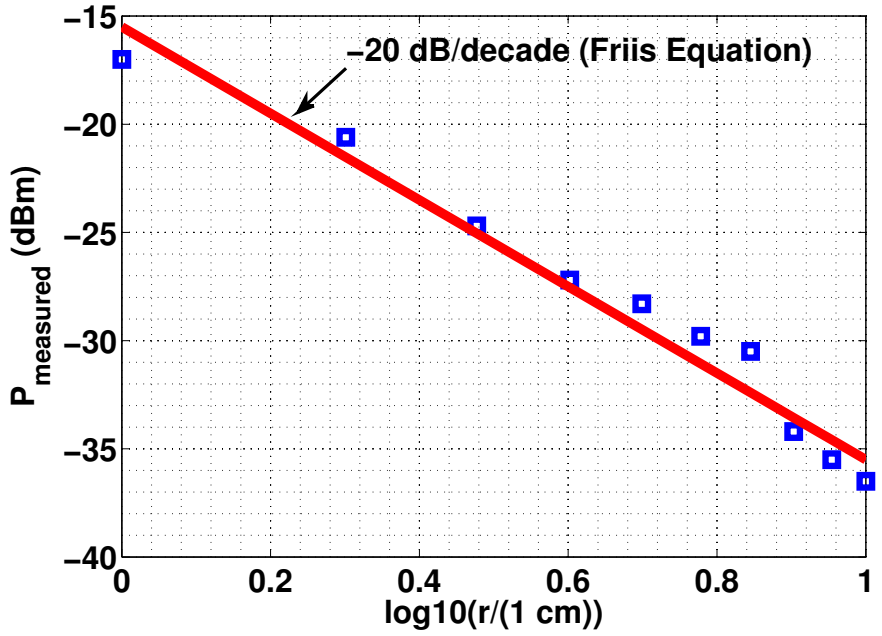


Figure 6.33. Variation of measured received output power with distance in CW mode

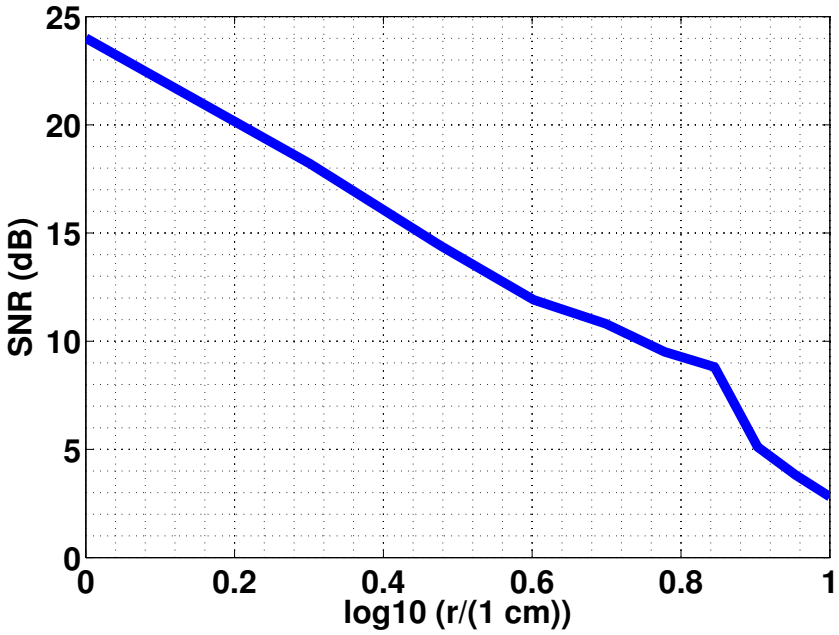


Figure 6.34. Variation of measured SNR with distance in CW mode

Compared to the transmitter measurements, the same LO clock can be used now for both the transmitter and the receiver and this allows one to plot the eye diagram of the received bits. For the lock range and continuous wave measurements, different LO frequencies are used for the transmitter and receiver chips.

A continuous wave (CW) measurement is first performed with the chips placed placed 60 cm apart. The frequency of the received tone is 18 times the difference in the LO frequencies. As shown in Fig. 6.32, the link is tested with and without a metal blocker. In the presence of a metal blocker, the sub-terahertz tone is not received by the receiver chip. By keeping the transmitter chip fixed, its distance from the receiver is adjusted and the resulting measured power level is plotted as a function of the distance. Fig. 6.33 shows the measured result. The data points follow the 20 dB per decade slope as predicted by Frii's equation. The signal to noise ratio (SNR) of the received waveform is calculated by summing up the total noise power in the bandwidth of interest. Fig. 6.34 shows the measured SNR. At a distance of 2 cm, the link has a measured SNR of 17 dB, which is good for high data rate communication at these frequencies. Since the transmitted power is known from the previous measurements and the path loss at a given distance can be calculated by Frii's equation, the signal power received by the receiver antenna can be calculated. Assuming room temperature and given the bandwidth of communication, the SNR at the receiver front-end can be estimated. The SNR at the baseband output is known from the above measurements. From these two measurements, the gain and the SSB noise figure of the receiver chain is calculated to be 25 dB and 15 dB respectively.

Next, the lock range of the transmitter and receiver LO chains is measured. In the same measurement, the functionality of both the I and Q channels is also verified. Fig. 6.35 shows

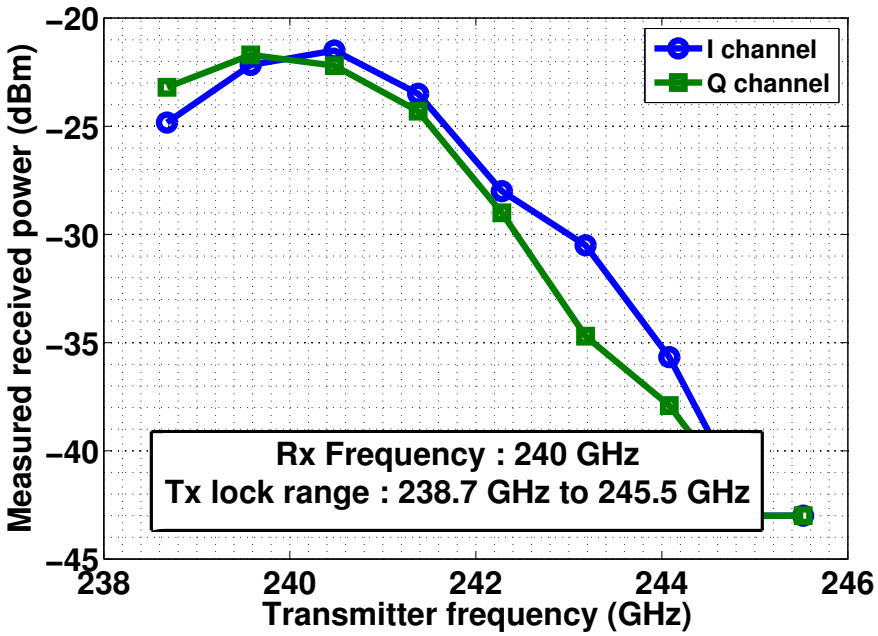


Figure 6.35. Measured CW receiver power for I and Q channels with varying transmitter LO frequency. Receiver LO frequency is held at 240 GHz

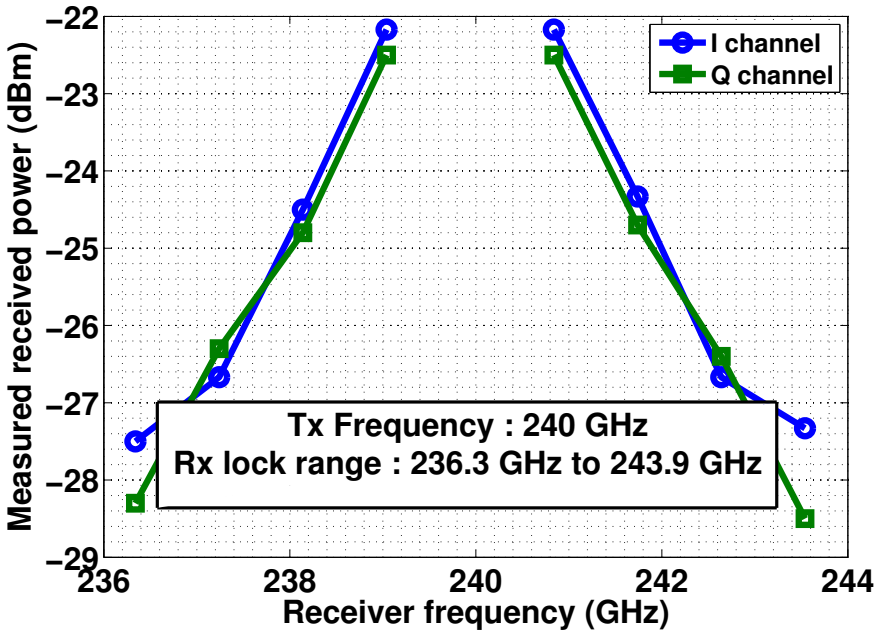


Figure 6.36. Measured CW receiver power for I and Q channels with varying receiver LO frequency. Transmitter LO frequency is held at 240 GHz

the measured received power in the I and Q channels as a function of the transmitter LO frequency. The receiver LO frequency is held constant at 240 GHz. It is observed that the power levels in the I and Q channels is well matched. The measured transmitter lock range is 6.8 GHz. A similar measurement is performed by fixing the transmitter LO frequency at 240 GHz and varying the receiver LO. The measured power levels in the I and Q channels are well matched and the receiver lock range is 7.6 GHz centered about 240 GHz.

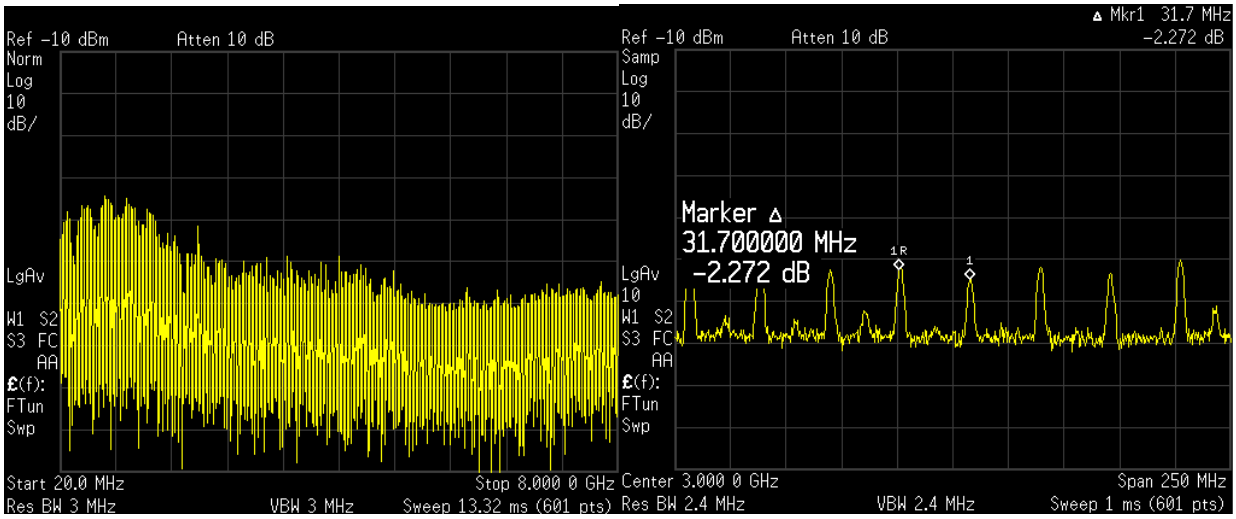


Figure 6.37. Measured receiver spectrum and beat frequency for 4 Gbps data

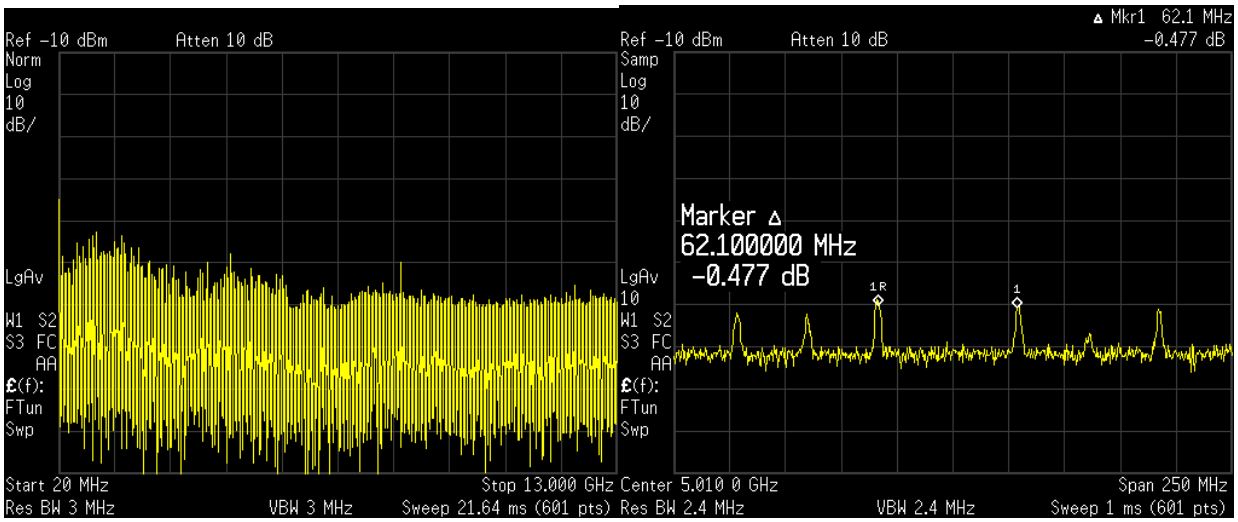


Figure 6.38. Measured receiver spectrum and beat frequency for 8 Gbps data

The transmitter is then configured to transmit modulated data by changing the PRBS settings. Fig. 6.37 and Fig. 6.38 show the received demodulated data for 4 Gbps and 8 Gbps BPSK. The received spectrum has a sinc pattern as expected. Additionally, the waveform has a repetition rate with a beat frequency given by (6.44). This confirms the functionality of the overall link.

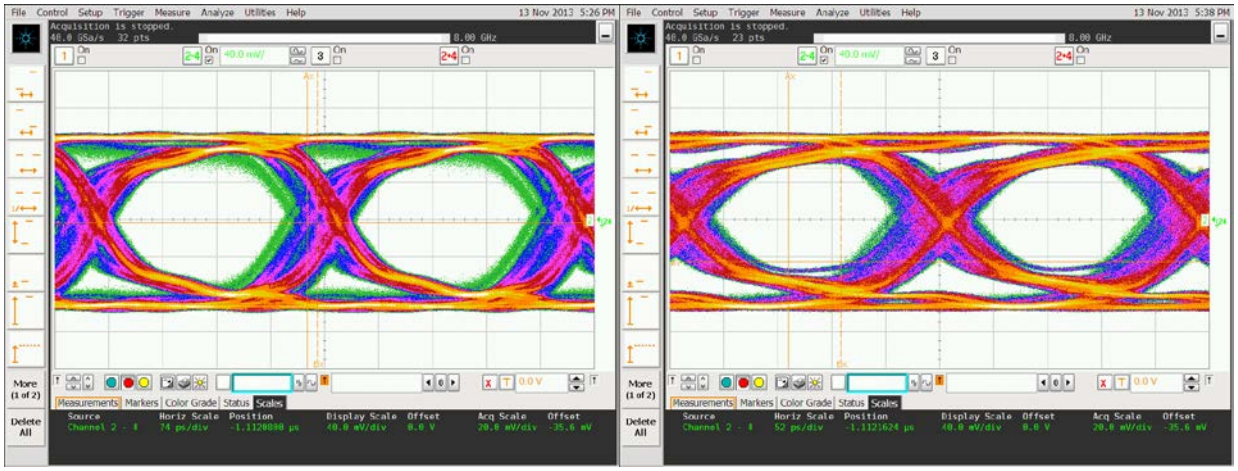


Figure 6.39. Measured receiver eye diagram for 3 Gbps [left] and 4 Gbps [right] data in BPSK mode

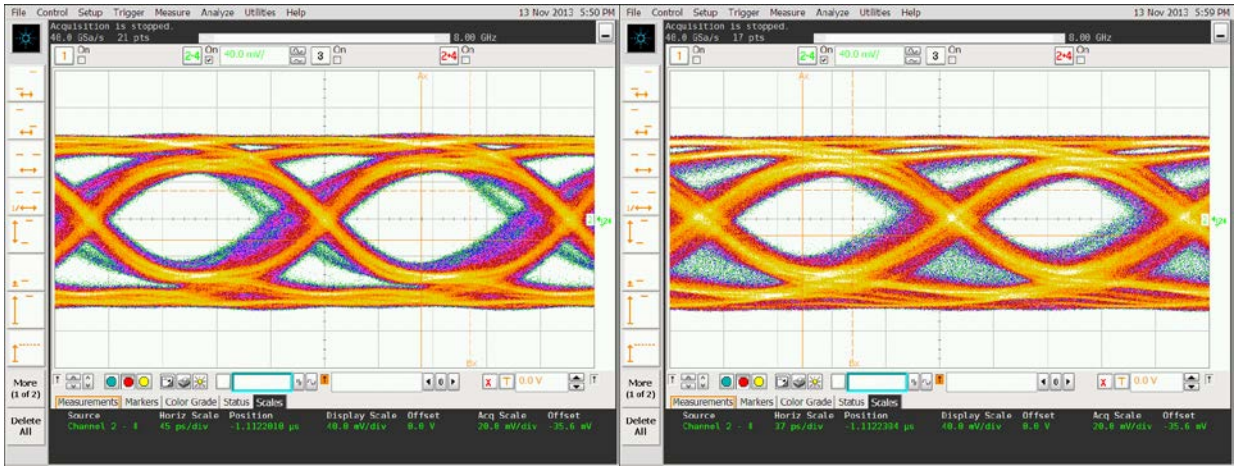


Figure 6.40. Measured receiver eye diagram for 5 Gbps [left] and 6 Gbps [right] data in BPSK mode

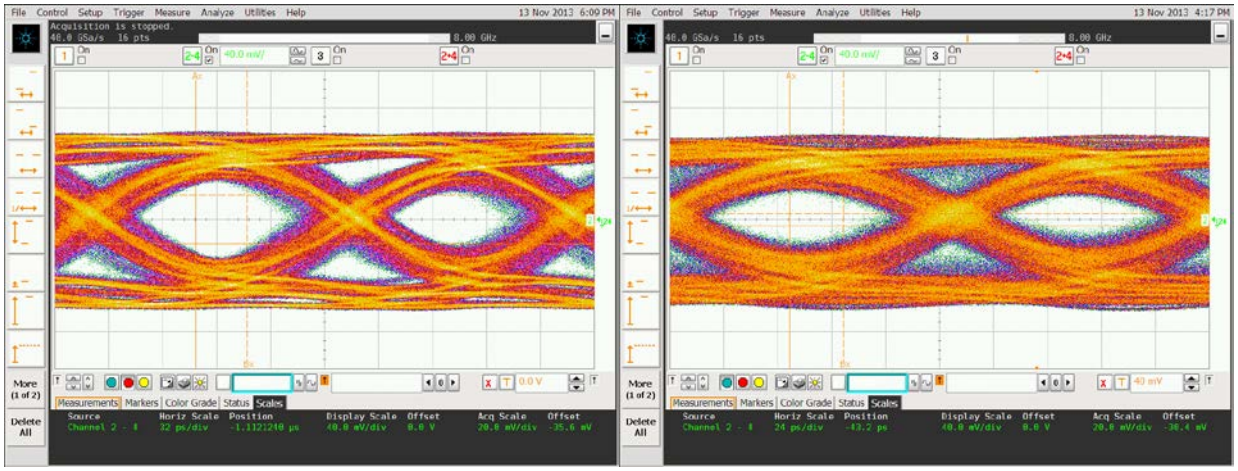


Figure 6.41. Measured receiver eye diagram for 7 Gbps [left] and 8 Gbps [right] data in BPSK mode

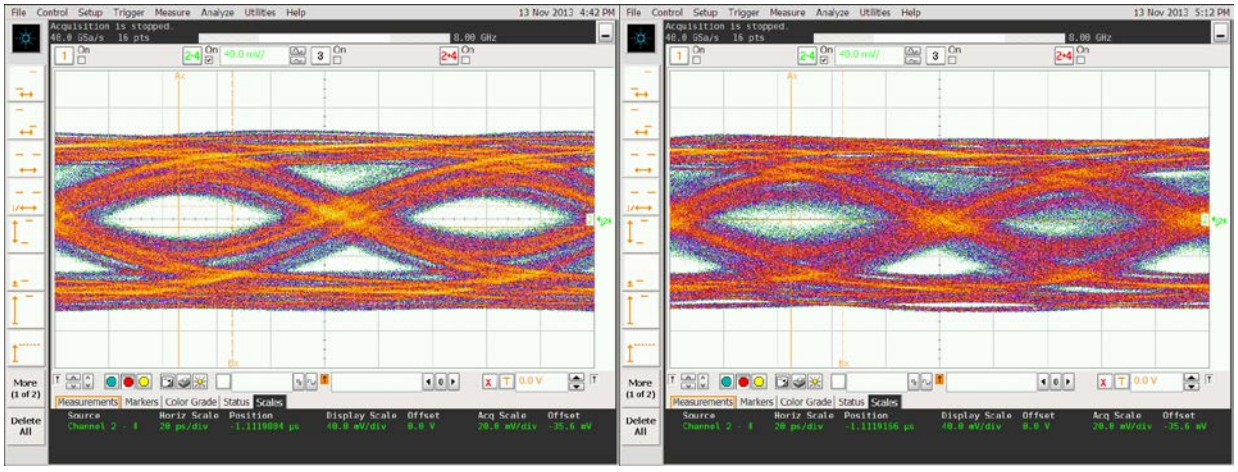


Figure 6.42. Measured receiver eye diagram for 9 Gbps [left] and 10 Gbps [right] data in BPSK mode

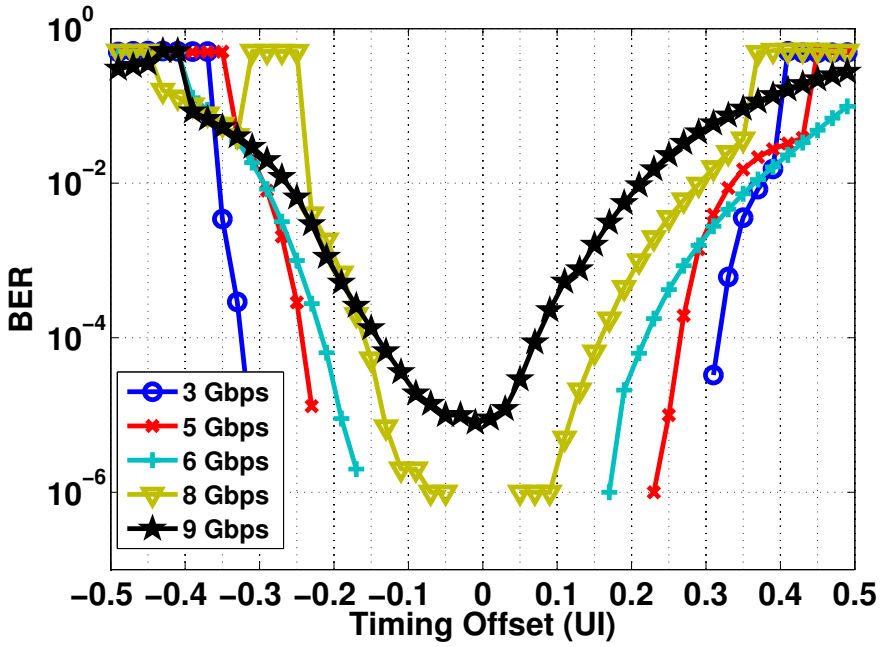


Figure 6.43. Measured bit error rate (BER) for BPSK mode

The system is next configured to capture the eye diagram for different modes of operation namely BPSK and QPSK. Fig. 6.39 to Fig. 6.42 shows the measured eye diagram for BPSK mode for data rates 3 Gbps to 10 Gbps. Each of the eye diagrams has been measured for a trillion cycles. The eye is wide open for data rates up to 9 Gbps. The waveform and the clock data were captured from the real time scope and the received bits were deciphered using an ideal comparator. Since the PRBS sequence is known a priori, the error in the captured waveform can be detected by varying the phase of the data clock. Fig. 6.43 shows the bath tub curve for different data rates. The link can operate upto a data rate of 9 Gbps with a BER of 10^{-5} and a maximum data rate of 10 Gbps with a BER of 10^{-4}. The minimum BER detection was limited by the memory capacity of the real time oscilloscope.

A similar measurement was performed for the QPSK mode on the I-channel. Fig. 6.44 to Fig. 6.46 shows the eye diagram for different data rates. Due to the phase noise in the LO path and mechanical stability issues, we can clearly see the symbol from the I and Q channels leaking into one another. This degrades the eye diagram in comparison with the BPSK mode. Fig. 6.47 shows the BER curve for the QPSK mode. The link can operate upto a maximum of 8 Gbps per channel or 16 Gbps total data rate with a BER of 10^{-4}. The power consumption of the transmitter and receiver chips is given in Fig. 6.48. As expected, the power amplifier consumes the maximum percentage of DC power in both the transmitter and the receiver. The baseband amplifiers also consume significant power as their noise figure needs to be low.

Table 6.1 compares the state-of-the-art published sub-terahertz transmitters in literature. Compared to other work, this transmitter design achieves the minimum power consumption while demonstrating transmission of 16 Gbps modulated data at these frequencies. The

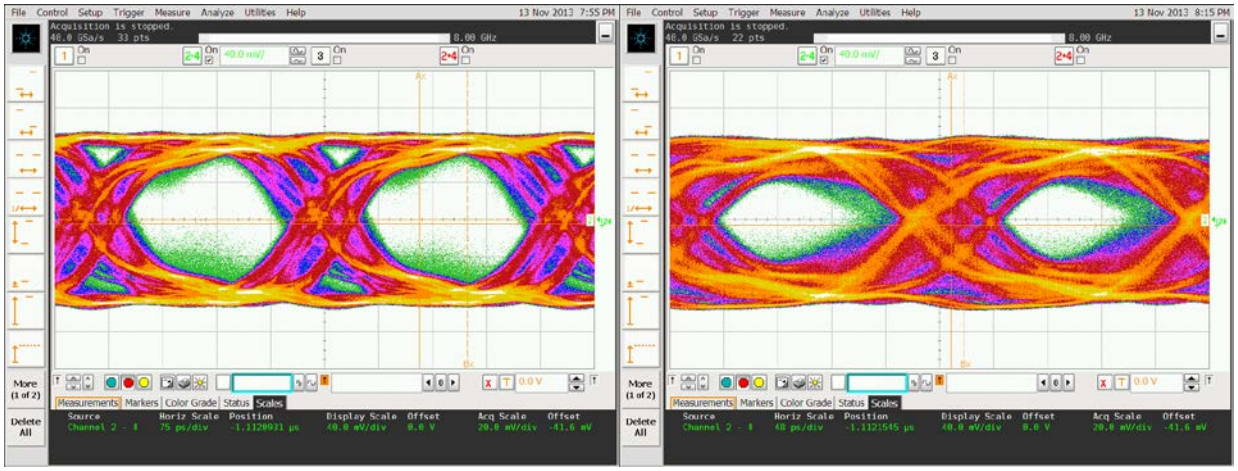


Figure 6.44. Measured receiver eye diagram (I-channel) for 3 Gbps [left] and 4 Gbps [right] data in QPSK mode

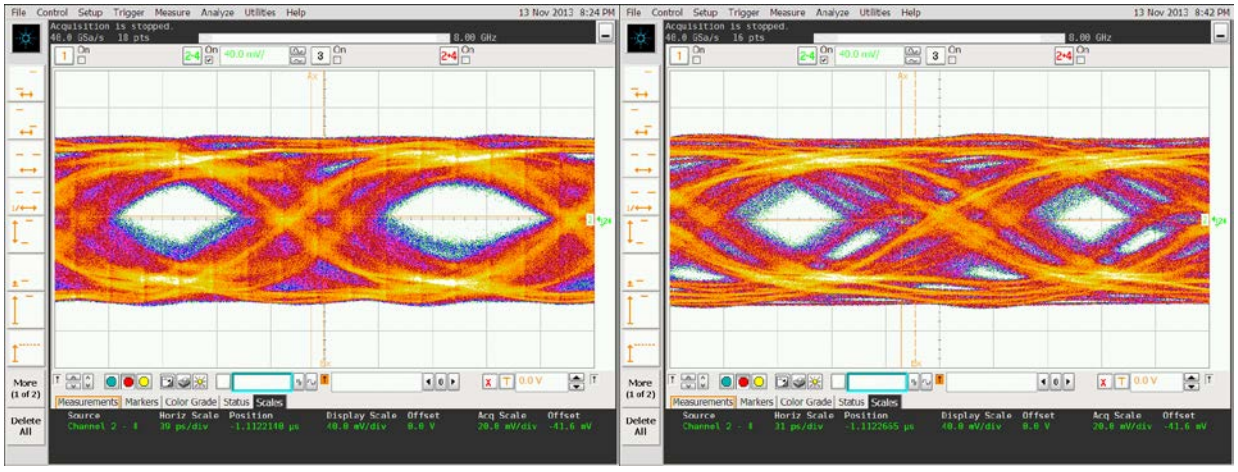


Figure 6.45. Measured receiver eye diagram (I-channel) for 5 Gbps [left] and 6 Gbps [right] data in QPSK mode

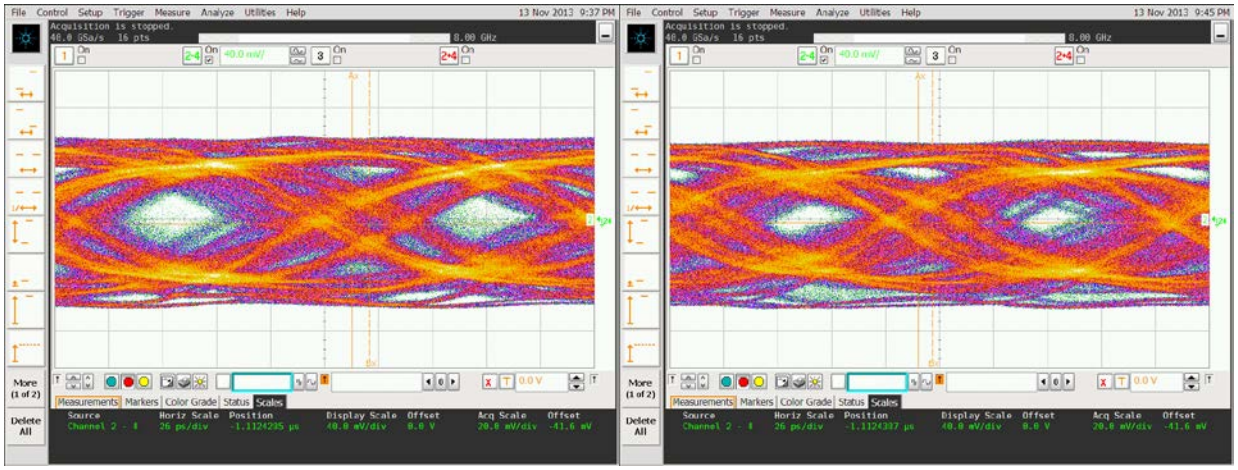


Figure 6.46. Measured receiver eye diagram (I-channel) for 7 Gbps [left] and 8 Gbps [right] data in QPSK mode

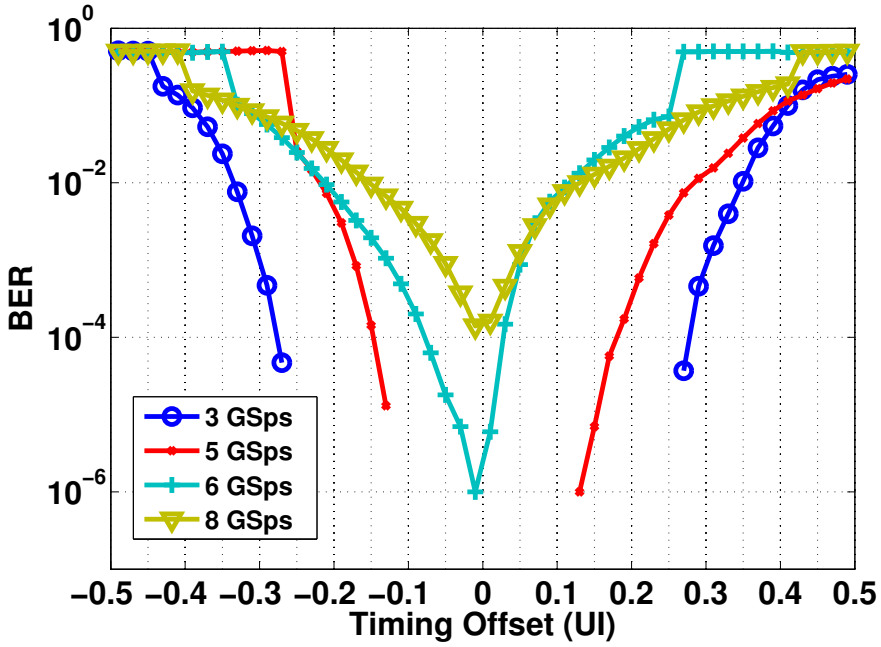
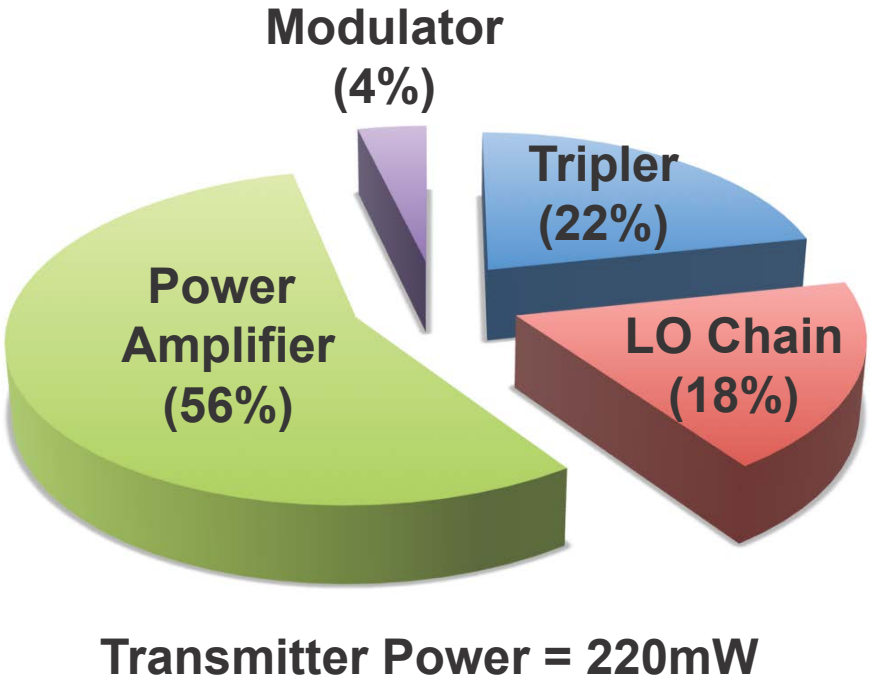


Figure 6.47. Measured bit error rate (BER) for QPSK mode



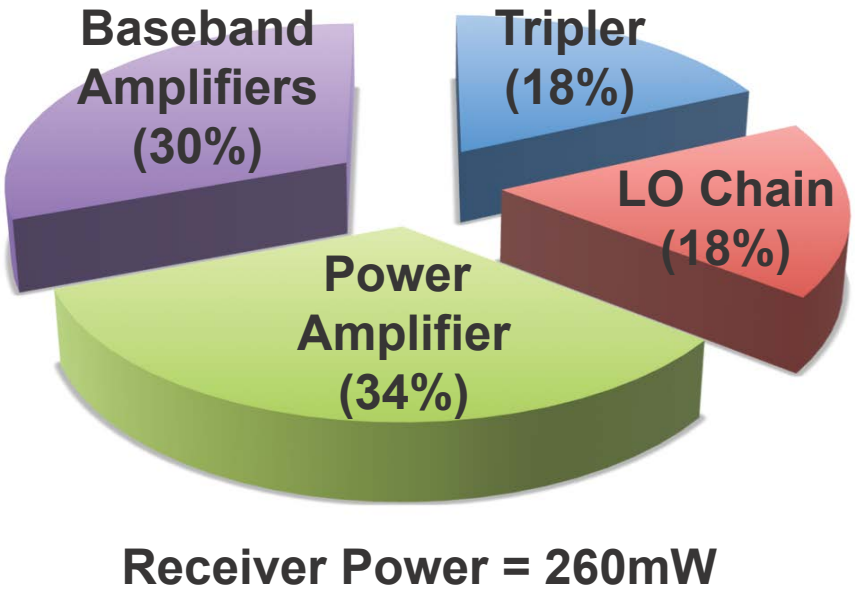


Figure 6.48. Power consumption distribution for the transmitter and receiver chips

Table 6.1. Summary of published sub-terahertz transmitters

	[37]	[66]	[67]	[68]	This work
Technology	65 nm CMOS	32 nm SOI	130 nm SiGe	65 nm CMOS	65 nm CMOS
Modulation	OOK	OOK	-	Pulse	QPSK
Frequency (GHz)	260	210	220	260	240
Pout (dBm)	0.5	4.6	-1	0.5	0
EIRP (dBm)	5	5.1	-	15.7 (Lens)	1
Pdc (mW)	688	240	630	800	220
Area (mm^2)	3	3.5	0.6	2.3	2
Antenna	On-chip	On-chip	-	On-chip	On-chip
Data rate	-	-	-	-	16 Gbps
Efficiency	-	-	-	-	14 pJ/bit

energy efficiency is 14 pJ/bit. Table 6.2 compares the state-of-the-art published sub-terahertz receivers in literature. This design achieves the maximum gain and minimum noise figure among all the other designs at these high frequencies. The design consumes 260 mW of DC power while receiving data rates up to 16 Gbps. The energy efficiency is 16 pJ/bit.

Table 6.3 compares the state-of-the-art published sub-terahertz transceivers in literature. This work shows the first demonstration of a completely functional link at 240 GHz in CMOS technology. It also shows the feasibility of using complex modulation schemes such as QPSK at these frequencies. The maximum communication range without the use of lenses is 1.5 cm. The design achieves a maximum data rate of 16 Gbps with an energy efficiency of 30 pJ/bit.

6.5 Conclusion

In this chapter, we discussed the design of a 240 GHz passive mixer and the measurement results from the transceiver. The transmit EIRP was measured to be 1 dBm and the trans-

Table 6.2. Summary of published sub-terahertz receivers

	[37]	[69]	[70]	[71]	This work
Technology	65 nm CMOS	130 nm SiGe	130 nm SiGe	65 nm CMOS	65 nm CMOS
Modulation	OOK	-	I/Q	-	QPSK
Frequency (GHz)	260	220	245	283	240
Gain (dB)	17	16	18	−6	25
NF (dB)	19	18	18	38	15
Pdc (mW)	485	216	512	97.6	260
Area (mm^2)	3	0.66	2.1	0.64	2
Antenna	On-chip	-	-	-	On-chip
Integration	Full	LNA, Mixer	LNA, Mixer, IF Amp, Hybrid	Mixer, LO, IF Amp	Full
Data rate	-	-	-	-	16 Gbps
Efficiency	-	-	-	-	16 pJ/bit

mitter operates to a maximum data rate of 16 Gbps. The power consumption is 220 mW. The receiver comprises of a mixer first direct conversion architecture with a measured gain of 25 dB and a noise figure of 15 dB. The wireless link comprising of the transmitter and receiver achieves a maximum data rate of 16 Gbps with an energy efficiency of 30 pJ/bit. This work is the first demonstration of a fully functional sub-terahertz link in CMOS technology. Compared to prior work, this design has the highest energy efficiency and the highest level of integration.

Table 6.3. Summary of published sub-terahertz transceivers

	[37]	[66]	[72]	[73]	This work
Technology	65 nm CMOS	32 nm SOI	50 nm mHEMT	Photonics	65 nm CMOS
Modulation	OOK	OOK	QAM	ASK	QPSK
Frequency (GHz)	260	210	220	300	240
Pout (dBm)	0.5	4.6	1.4	-	0
EIRP (dBm)	5	5.1	-	30	1
Rx Front	Mixer	LNA	LNA	SBD	Mixer
Pdc (mW)	1173	308	-	-	480
Area (mm^2)	6	4.62	3	-	4
Antenna	On-chip	On-chip	Off-chip + Lens	On-chip + Lens	On-chip
Antenna Gain (+Lens) (dBi)	4.5	-	30 (Lens)	34 (Lens)	1.5 Tx, 0.7 Rx
Range (cm)	-	-	50	50	1.5
Data rate	-	-	25	12.5	16 Gbps
Efficiency	-	-	-	-	30 pJ/bit

Chapter 7

Conclusion

7.1 Thesis Summary

The tremendous growth in connectivity, media sharing and social networking in the last decade has led to an explosive increase in the amount of data being shared across the globe. The increased data transfer is seen in cloud computing, internet of things applications, high performance computing and use of portable electronics such as laptops, tablets, mobile phones. Moving into the future, our thirst for ubiquitous connectivity with high data rates can be quenched only by innovations in faster devices, newer technology and high speed interconnects. In this thesis, we explored the millimeter-wave/terahertz frequency band as a potential solution for achieving high speed data communication that could complement or replace already existing wireline and optical interconnects. Specifically, communication in the 60 GHz and frequencies beyond 100 GHz were discussed. These wireless interconnects would be useful in various applications ranging from personal area networks for portable electronic devices, wireless backhaul networks for better connectivity, wireless in a box application in form factor devices and in data centers for cloud computing and big data applications.

We discussed the design of linear power amplifiers in V-band frequencies at scaled technology nodes and also explored switching power amplifier architectures. Scaling to a better technology node (in this case 28 nm) provided significant benefits in terms of achieving high bandwidth systems but resulted in lower efficiencies. This design achieved a peak gain of 24.4 dB with a bandwidth of 11 GHz which is the highest gain-bandwidth product power amplifier reported in literature. This design was also the first power amplifier implemented in 28 nm technology node. As power amplifiers are critical blocks in any transceiver design (as they usually determine the efficiency of the system), they provide insight in the choice of technology and whether one should use finer technology nodes for millimeter-wave/transceiver systems. As an alternative to linear power amplifiers (PA), switching PAs can achieve higher efficiencies at the cost of linearity. The design of an inverse class-D switching power am-

plifier was discussed with standalone measurement results. The device in a switching PA operates in a non-linear regime and modeling becomes important to accurately predict the performance of the PA. The modeling of the switch resistance and the non-quasi effects were discussed. The PA achieved an efficiency of 21.5 % with a measured output power of 12 dBm.

While circuit blocks provide valuable information with regard to the choice of technology and system architectures, the design of a complete system involves challenges at various levels. This thesis discussed some of the challenges faced in the design of terahertz systems for high-speed interconnect applications. We explored two transceiver architectures each with a different harmonic generation technique and modulation scheme. The first prototype incorporated the V-band switching power amplifier block and some of the ideas from the linear PA design. The 260 GHz transceiver prototype was the first published complete system at these frequencies. The transmitter achieved an EIRP of 5 dBm and a maximum modulation rate of 14 Gbps was achieved. A continuous wave signal was transmitted from the transmitter and demodulated at the receiver. While the design had issues with regard to LO leakages, it was instrumental in verifying the modeling approaches and in shaping the next generation architecture and board designs for highly efficient terahertz systems. The next generation terahertz system operating at 240 GHz was discussed in Chapters 5 and 6. The design used a simplified architecture on both the transmitter and the receiver and was optimized to minimize power consumption, the die area and to maximize the data rate. The design achieved an EIRP of 1 dBm and a maximum modulation rate of 12 Gbps BPSK (24 Gbps QPSK) was measured on the transmitter side. The modulated data was successfully transmitted to the receiver and a peak data rate of 16 Gbps QPSK was achieved with an energy efficiency of 30 pJ/bit. This design was the demonstration of the world's first fully functional link operating at frequencies greater than 200 GHz in CMOS technology.

While the above circuit blocks and designs paved the way for the next generation technology, we observe that the achieved data rate of 16 Gbps is pretty low given our frequency of operation. As we are operating at 240 GHz, a 10 % bandwidth should theoretically provide us upto 48 Gbps of data transfer. Even though the efficiency metric is almost four times better than the previous generation, it is still much higher compared to wireline links (typically 1-4 pJ/bit). This must be further improved to make them more competitive and promising as a technology of choice. We now discuss some future directions which would help us realize this goal.

7.2 Future Directions

As discussed earlier, the transceiver designs described in this dissertation perform the modulation at the intermediate frequency (IF) and the resulting modulated waveform is then up-converted to sub-terahertz frequencies. Hence, the complete bandwidth at the sub-terahertz frequency is not utilized. In order to increase the overall data rate and utilize the spectrum better, we can use frequency multiplexing. For example, three carriers at 73.33 GHz, 80 GHz and 90 GHz (each with 20 Gbps modulated data) can be frequency tripled

to up-convert the IF to sub-terahertz frequency. The sub-terahertz frequency spectrum they occupy includes the band from 210 GHz to 270 GHz and can potentially deliver 60 Gbps of data rate. However, this requires harmonic generation schemes which preserve the channels due to non-linear frequency tripling. As one can expect, inter-modulation distortion due to the non-linearity would certainly degrade the signal integrity. However, by using equalization schemes on the receiver, the signal could probably be recovered. Another area which requires attention is the non-linear generation of the carrier frequency. Non-linear generation schemes are inefficient and require the design of high output power, efficient PAs which are usually the efficiency determining blocks in such systems. By improving the efficiency of the non-linear generation scheme or using better technology nodes (so that the transceiver can operate in fundamental mode), a better efficiency may be achieved. As their is no improvement in f_{max} due to the scaling of CMOS technology, more research is required in the non-linear generation scheme. However, some other blocks such as mixers could benefit due the scaling of CMOS technology due to better transition frequencies. Significant effort is also required in inspecting new PA architectures such as the Distributed Switching PA [74] which could either provide a high output power or higher efficiency. The power consumption of the millimeter-wave blocks is also dictated by the gain achievable per stage of amplification. Exploring techniques where the gain of the amplifier can reach four times the unilateral gain could provide significant benefit in improving the design efficiency [75]. The design of efficient highly directional antennas is another area which requires research. Increasing the directivity of the antenna could increase the range from centimeters to meters. Antennas on package or use of silicon lenses could improve the range considerably. Phased array systems would help to improve alignment between the transmitter and the receiver and allow both broadside and end-fire communication. In this thesis, we explored air as a channel for wireless interconnect application. Using waveguides [76] with materials such as plastic, the communication range can be increased significantly due to the lower spread of the signal through the channel. Modeling of the transistors at these frequencies also requires attention to accurately predict the device performance. The simulation of the structures (especially antennas) used in this design require considerable time and simulation resources to obtain the optimal solution. Developing simplified models for known structures could go a long way in speeding up the design process. The demonstration of the two transceiver designs and blocks show the feasibility of communication at these high frequencies and pushes CMOS technology into new realms. However, the evolution of this technology requires significant research to address the various issues discussed above and eventually this would lead to commercial products in the future.

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