A Platform-Based Approach to Low-Power Receiver Design

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by

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Abstract

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Driven by the desire of people to communicate more efficiently, more flexibly and more reliably, tremendous changes are occurring in the wireless world. As one of the dominant drivers for the semiconductor industry, the wireless evolution towards higher data rate and higher capacities presents numerous opportunities. However, it also introduces many challenges to the current design technology, particularly, the demanding requirement for low power or even ultra-low power consumption. The rapid growth of various wireless services increased the need for highly integrated and low-cost solutions with very demanding performances. The fast growing market and heated competition require very short system development cycle. To cope with this constantly increasing system complexity, higher performance demands and tight time-to-market constraints, it is imperative to develop new design techniques for wireless systems to cope with these challenges.

This dissertation presents a design approach for wireless systems where the design requirements are demanding in terms of contradicting objectives. The approach is based on the paradigm of *platform based design*, featuring in the adoption of higher

levels of abstraction, better reusability and early consideration of system performance. Wireless receivers are used to demonstrate the approach proposed here. A receiver is a complicated system consisting of RF, analog and mixed-signal components. Traditionally, when developing a wireless system, system design and circuit design are conducted separately. Our research shows that effective interactions between different levels are critical to obtain an optimal system. In this research, systematic design space exploration is necessary to facilitate the trade-off evaluations and system partitioning. To demonstrate this concept, the platform-based receiver system design is presented from system level down to circuit design, focusing on the minimization of the overall power dissipation while maintaining system performance. Two application scenarios are explored. One is a receiver front-end for an MB-OFDM UWB system. The other one is an ultra-low power mostly-analog baseband design for wireless sensor networks.

In the context of the proposed design approach, several representative challenges in the wireless receiver design are investigated, which include how to improve the system robustness against various interferences, how to quickly estimate the wireless system performance in an analytical approach, how to validate a system algorithm in a heterogenous simulation environment, how to build the abstracted behavioral models and use them to perform the design space exploration, etc. The circuit level design concerns and subthreshold design techniques are also demonstrated. Finally, system-level optimization is performed using behavioral models and, to preserve fidelity, the models are constrained by the achievable performance of actual circuit implementations. The resulting two designs show that significant power savings can

be accomplished through systematic design space exploration in the platform-based design framework.

Professor Alberto Sangiovanni-Vincentelli
Dissertation Committee Chair

To my parents and my husband

Contents

List of Figures

List of Tables

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Chapter 1

Introduction

In the past several decades, wireless communication technology has brought dramatic changes to this world. It has become an integral part of everyone's life. With the rapid evolution of wireless technologies, a mobile phone is not merely a simple voice centric device, but also an Internet browser, a camera and a compact entertainment center. You can use your cellular phone to get a driving direction or find a nearby restaurant quickly when you are on the road, or enjoy a real-time TV program when you are waiting for a flight. Driven by the desire of people to communicate more efficiently, more flexibly and more reliably, tremendous changes are occurring in the wireless world.

1.1 Trends and Challenges in Wireless System Design

According to the statistics from ITU World Telecommunication, the market of wireless mobile devices has experienced an explosive growth in the last decade to fulfill people's increasing need. As shown in Fig. 1.1, the worldwide mobile subscribers have

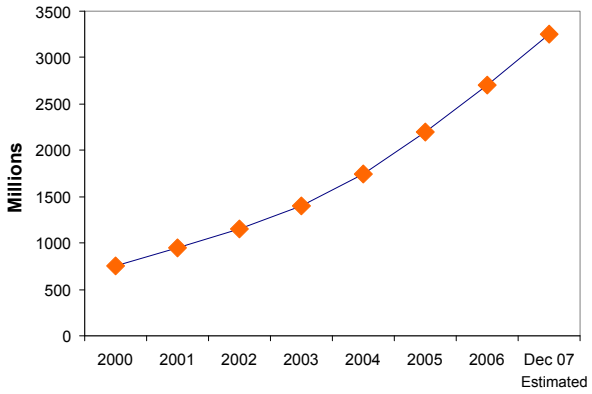


Figure 1.1. Growth of worldwide wireless subscriptions (source: ITU World Telecommunication/ICT Indicators Database)

increased from around 800 millions in 2000 to over 3 billion in 2007. Another set of data, as shown in Fig. 1.2, demonstrates the rapid growth of Wi-Fi services. The number of Wi-Fi users is expected to grow to nearly a billion in the next 5 years.

The tide of wireless evolution towards higher data rate and higher capacities has motivated numerous new research topics in related areas. The growth of various wireless services increased the need for low-cost highly integrated solutions with very demanding performance. Wireless applications have been and will remain being one of the dominant drivers for the semiconductor industry. On the other hand, the dramatic progress in IC technology has enabled small-area and low-power implementation of sophisticated systems. From the perspective of wireless system implementations, we can see several main trends as following.

1.1.1 Low Power Consumption

In portable wireless applications, low power consumption is one of the critical requirements that designers make a great deal of efforts to achieve. As advanced multimedia and entertainment applications are becoming must-have features, apparently

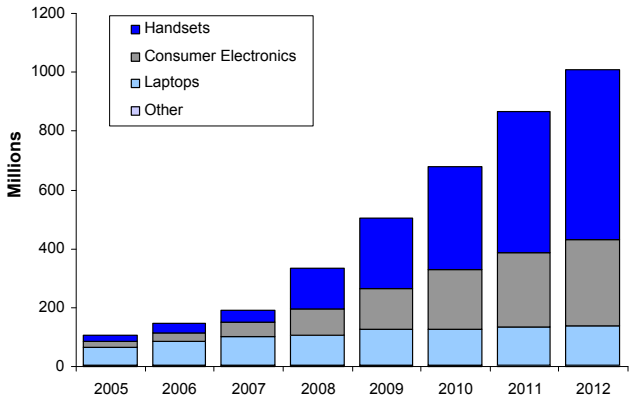


Figure 1.2. Wi-Fi market projections (source: Skyhook Wireless)

higher power demand will be inevitable to realize the multi-functions. Therefore, it is more critical to develop new low-power techniques.

Other recent emerging applications, such as wireless sensor networks [41], have gained many interesting applications, such as improved human health monitoring, fire detection in forests, environmental control in smart buildings, etc. Shrinking semiconductor cost makes these areas more attractive. In a wireless sensor network consisting of a large number of distributed nodes, replacing batteries at regular instants in battery-powered nodes is impractical. It will be advantageous for the sensor nodes to be able to scavenge the energy from the environment. For this purpose, it is critical to pursue design solutions that reduce the power consumption as much as possible. This kind of systems pose extremely aggressive power dissipation challenges.

A new generation of wireless communications, 4G system, has attracted many attentions, targeting an "all-in-one" handset that enables seamless integration and fast communication between wireless devices across diverse wireless standards in different environments (from indoor networks such as WLANs and Bluetooth, to cellular signals, radio and TV broadcasting, and satellite communications) as well as broad-

band networks. This new generation of mobile devices offering faster speed and more functions is expected to appear in the market by the end of this decade [25, 51]. Maintaining a power efficient design in the multi-function multi-standard 4G devices is one of the main tasks to tackle.

As the system performance requirements and the bandwidth demand increase, power conscious design becomes more difficult than before. Using a low voltage process technology is helpful to some extent in reducing the power consumption, but not sufficient enough if it is the only strategy. The stringent power dissipation constraints require dedicated efforts at every stage of design - system planning, architecture, software, algorithm, logic design, circuit design, and so on.

1.1.2 Increasing System Complexity

In the extremely competitive market, wireless systems are driven to higher levels of integration to achieve smaller physical size and lower cost. The integrated transceivers are quite complicated systems, including RF (Radio Frequency) blocks, analog blocks, and mixed-signal blocks together with digital circuitry on the same chip. Managing an efficient transceiver budget is one of the most compelling tasks the designers are facing. For instance, many tradeoffs have to be balanced due to the interdependency among the noise, non-linearities, gain, sensitivity, and selectivity.

The situation is even more challenging when the wireless system is designed to provide cost effective multi-function service. Besides high speed wireless communication capabilities, demanding functionalities also include positioning, aggressive multimedia and business applications, financial service, etc. When more and more functions are squeezed into a single system, the level of complexity is increased with the need to keep the system performance high (e.g. sensitivity, interference performance, etc.) and the power consumption low. The design tradeoffs and implementation options

inherent in meeting these demands highlight the extremely challenging requirements for a transceiver system.

Usually, even with the increasing complexity of the digital part, the RF and analog parts remain to be the bottleneck of the whole system design process, posing a main barrier of shrinking the entire design cycle. Especially, for a RF design, challenges lie not only in achieving successful operation at a relatively high frequency of 1-2 GHz, but also in doing so for widely varying application environments, under tight constraints such as cost and power consumption. From the system-level point of view, it is critical to understand and manage the effects from the multi-dimensional performance space of RF and analog components. To achieve that, Electronic Design Automation (EDA) methodologies and tools are desired to undertake the task managing the increasing design complexities in tight time-to-market requirements.

1.1.3 Technology into Nanometer Era

The rapid evolution of semiconductor technology is one of the main contributors to the explosive growth of wireless applications. As in Moore's law, the number of transistors on a chip has increased exponentially, doubling approximately every two years. The CMOS technology is evolving deeper and deeper into the nanometer era, 90 nm, 65nm and even 45nm. This has brought faster, denser logic for less power, at lower cost per function, and also allowed more complex systems to be integrated on a single chip.

While the advanced technology is always preferred for cost reduction and system performance improvement, the designers, especially RF designers, have to handle the significant challenge of moving the design from one technology node to the next. For digital designers, the process of technology migration is known. However, the transition to new technologies brings along significant challenges to RF and analog

designers, for instance, to maintain a reasonable dynamic range and signal to noise ratio, which are proportional to the supply voltage. With the tight time-to-market constraint, it is crucial to migrate the design generation effectively, particularly when the supply voltage is lowered with the technology scaling. Proper design methodologies and tools that can facilitate this technology migration for RF and analog design and increase designers' efficiency are still missing.

When the technology moves to the nanometer era, considering the prohibitive cost of a mask set, it is more urgent than ever to be able to complete a new product in least number of silicon re-spins, preferably a first-pass silicon. Thus it becomes imperative to improve the modeling, simulation and verification techniques to achieve a higher rate of first-pass silicon success.

1.1.4 Systematic Design Methodology

Nowadays, the system level design of transceivers is usually performed using spreadsheets. This method is limited in the number of different design possibilities it can explore within a given time. More effective design space exploration is desired since more significant improvement in cost and performance can be made in the system planning and architecture selection phases.

In comparison with their digital counterparts, the analog and RF components have a much longer design cycle. Besides developing the circuit topologies, it also takes the designers numerous efforts to adjust the device parameters and various circuit configurations. Moreover, the RF and analog circuits are also noticeably sensitive to a wide range of parameters including parasitic effects, substrate effects, packaging effects, etc. Due to the limitations of the available EDA tools for RF and analog circuits, most of the analysis and design work still highly depends on the circuit designer's judgement, making the solution less than optimal in terms of efficiency

and quality. Furthermore, whenever the block specification is changed, it takes a long time again to translate this change to the circuit parameters. The entire design process highly relies on the designer's experience.

The increasingly competitive market of wireless applications forces higher pressures on time to market. For example, the design cycle of a handset has been pushed from the typical 2 years to the target of 6 months, or even more compressed. To deal with constantly increasing complexity and time-to-market pressure, there is clearly a need for a new design methodology to support the trends and handle the challenges mentioned above. Recently, several EDA tools have been developed in this perspective [3, 17, 23]. But they provide very little help to the designers on the entire design flow and the system level optimization.

A fundamental problem of the current design methodologies is that an effective interaction is missing between system level design and circuit level design. To achieve an optimal solution on the system level, one of the biggest challenges for the designers is to understand somewhat unrelated disciplines such as RF and analog circuit design, circuit modeling and characterization, and digital communications. Having a complete design flow from system to silicon, such as the one described in this thesis, we believe we can increase the design productivity significantly.

1.2 Work of this Thesis

In this thesis, I present a systematic design approach for wireless systems where the design requirements are demanding in terms of contradicting objectives, such as high performance requirements and low power consumption. The proposed methodology helps the designers balance various tradeoffs and make the optimal choices at system level. Using this approach, the chance of first-pass success will be greatly increased.

The approach is based on the paradigm of *platform based design*, featuring in the adoption of higher levels of abstraction, better re-usability and early consideration of system performance. Besides the platform-based design flow, this dissertation also makes a claim that low power design efforts should be taken into consideration at all design layers. The rest of this dissertation is organized as follows:

In chapter 2, the main difficulties of the traditional design approach are analyzed. The idea of platform-based design is introduced and a design flow leveraging the new abstraction levels is detailed. Following that, two challenging application scenarios requiring the minimization of power consumption are explored to demonstrate the effectiveness of this approach. These two applications are in radio frequency and in low frequency respectively, representing different design challenges. I use them to demonstrate different aspects of the new approach.

The systematic design effort starts with the system level exploration in chapter 3, where the representative design challenges of receiver systems are investigated, such as functionality partitioning between analog domain and digital domain, system robustness against the various interferences, etc. For modeling and validation purpose, an analytical approach and a simulation-based approach are discussed. To perform accurate estimation of the interference effects, a new analytical approach is proposed and validated. Furthermore, the critical concerns of validating a mixed-signal system in a heterogenous simulation environment are addressed in Metropolis.

Chapter 4 demonstrates the platform exploration approaches at the architectural level and the circuit level. Behavioral models are introduced to describe the functionality of the RF/analog blocks on a higher abstraction level. The specific requirements on behavioral models are addressed, and a concrete model for an RF front-end is generated. After that, reconfigurable devices are also discussed as a candidate platform to perform architectural exploration. The second part of this chapter focuses on the

circuit level exploration. A subthreshold circuit design technique and the associated device models are presented. This part also discusses the analysis and design of the specific circuitries for the two low-power applications. As a critical step of the platform-based design flow, circuit characterization is carried out to explore the circuit level design space. As a result, the circuit performance models are generated.

In chapter 5, based on all above design explorations, optimization is done in the context of platform mapping. The resulting low power implementations are reported, testifying the effectiveness of the platform-based receiver design approach. This chapter also shows the testing results of a silicon implementation.

Finally, chapter 6 concludes the dissertation with a summary and a discussion of future research directions.

Chapter 2

Methodology

2.1 Traditional Design Approach to Transceiver Systems

2.1.1 Design Flow

The top-down design process of a wireless communication system can be summarized in the diagram (Fig. 2.1). At system level, the design specifications are usually set by the addressed wireless standard. The standard sets a profile of the surrounding wireless environments, including the adjacent channel selectivity, blocker profile, and so on. Based on these, the system designer will derive a set of transceiver specifications, such as intermodulation requirements, noise figure, linearity requirements, etc. The next task of system design is to make the functional decomposition, select the transceiver architecture and derive the specifications of each building block. Traditionally, hand calculations or spreadsheets are used during this system level architectural design. For simulation purpose, Matlab/Simulink are often used, where some block models with non-idealities are available in the library.

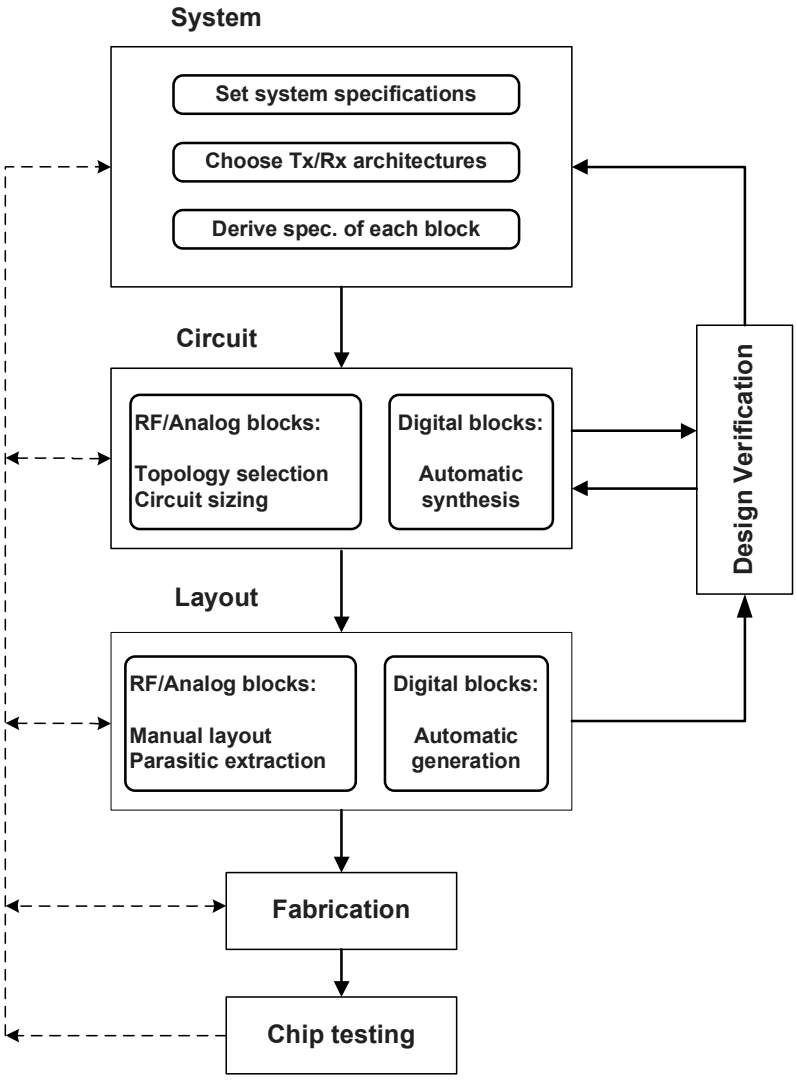


Figure 2.1. Typical design flow of a transceiver system

Having the block specifications, the design process proceeds to the block architecture exploration and circuit design. In this stage, digital circuits can be dealt with by automatic synthesis. While RF and analog circuit design heavily rely on the designers, including topology selection and circuit sizing. Simulations are exploited to get accurate performance estimates at circuit level. Low frequency analog circuits are usually simulated with SPICE (or SPICE-like tools), which provides DC, AC, noise and transient analysis. Since RF signals usually consist of a high frequency carrier

modulated with a low frequency signal, and the difference of their frequencies can be as large as several order of magnitude, the normal transient simulations are very time consuming. Some dedicated RF simulators, such as SpectreRF[15, 16], have been developed to solve this problem, providing periodic and quasi-periodic, and transient envelope analysis.

After the circuits have met the specifications, the next stage is the layout generation. Again, automatic layout generation tools are available to the digital circuits. For RF and analog circuits, the circuit performances are very sensitive to the parasitic factors. The device layout, and the placement and routing have to be performed manually. Beyond that, before the chip is sent out to fabrication, parasitic extraction and post-layout simulation of the RF/analog circuits are also needed.

2.1.2 Difficulties and Challenges

1. **System Optimization**

   To win in the competitive market, an optimal system should not only provide the desired functions with maximal performance, but also demonstrate the advantage of smaller physical size and efficient power consumption. As these objectives are conflicting to each other, a big challenge to achieve them is to balance the tradeoffs at the system level. On the other hand, it is more important in practice to achieve an implementable solution, even having to sacrifice the optimum to some extent. Changing system-level specifications in the later design stages should be avoided since that will cause big changes at the lower design levels, even a complete start from scratch. Keeping that in mind, the system architect usually sets some margins when evaluating the tradeoffs and derive the block specifications. A system designed in this way is seldom an optimal design, just an implementable one.

Another reality is that design space exploration at system level is rarely performed due to the intrinsic complexity and the time-to-market pressure. However, better solutions in terms of performance and cost can be found by exploring various architectures, attempting different performance partitions or playing with the design margins. Though it has been acknowledged that the significant impact comes from the highest design level, the design space exploration at system level is still very limited and is hard to integrate into the design flow unless a systematic approach is developed.

Due to the absence of an inter-level interaction, the optimization objectives are only addressed at a specific level if there is any. For instance, at the circuit level, lots of manpower is dedicated to analog circuit sizing to minimize the power consumption and area while meeting the performance requirements. Since this type of optimization efforts are conducted only at the "local" level, the results make limited impact on the same objectives at the "global" level. Consequently, the entire system is still less than optimum though considerable time and resources have been spent for the optimization purpose.

2. **Design Iteration**

   If we consider the entire design process, iterations (shown by dash lines in Fig. 2.1) among the different design stages also take a considerable portion of the design cycle. For instance, the block specifications can not be satisfied on the circuit level after trying different topologies and a few attempts of circuit sizing. The design will have to go back to the system level, where the architect needs to make a new performance decomposition or even change the architecture, and derive a new set of block requirements to propagate to the circuit level. Similar iterations could also occur if the post-layout simulation demonstrates a failure to meet the minimum performance requirements, that unfortunately needs to go

back to the higher levels (circuit level or even the system level) and apparently requires more efforts to fix the failure.

One of the main reasons that possibly causes the iterations is the gap between the different design levels. Usually, two different groups of people work on the system level and the circuit level. Their expertise are in different areas, e.g. system architect in communication and algorithms, and circuit designers in circuit analysis and design. The design and simulation tools are also applied on the particular level, not crossing the different levels. Consequently, there is no effective interactions to cover the gap between different levels, that possibly leads to time-consuming design iterations. The system architect does not have enough knowledge of the lower levels, and commonly, the performance and cost evaluations are still unknown at that design stage. All of these can bring about some block specifications that are infeasible at the circuit level. So, reducing the possibility of cross-level design iterations is key in meeting the increasingly tight time-to-market constraints.

3. **Circuit Sizing**

   At the circuit level, in contrast to the digital parts, the RF and analog parts are the bottleneck of the entire system design, in terms of performance, design time, and cost. The RF/Analog design consists of two phases, topology selection and circuit sizing. Topology selection is more like a heuristic process, requiring the designer's knowledge and expertise. Therefore, traditionally it is a manual process. Though there are many existing topologies for those commonly used blocks, novel topologies are continuously developed to enhance performance to meet the aggressive requirements.

   During circuit sizing, to meet the performance requirements and reduce various cost (power consumption, chip area, etc.), designers calculate and adjust

the circuit parameters, including component values and dimensions (width and length of transistors, values of resistor, capacitor and inductor, etc.) and circuit configurations (bias current, reference voltage, etc.). In RF/analog circuits, the performance is inevitably degraded by intricate sources, such as various noise sources, non-ideal effects, parasitics, etc. This makes the circuit sizing a complicated and time-consuming task. Whenever the block specifications are changed, it takes a long time for the designers to propagate the changes to the circuit parameters, even if the topology remains same.

2.2 Recent Progress

Advanced design approaches and supporting EDA tools are critical in successfully going from system planning to chip fabrication while meeting the increasingly tight time-to-market constraints. Enormous research effort has been made to provide RF/analog designers with EDA tools to ease their job at different design levels.

These tools and methodologies focus on different aspects of RF/analog design [24, 46, 52, 17, 23]. Behavioral models of RF/analog blocks are important to accelerate the system simulation and verification. Some work focused on the macromodeling techniques for RF/analog blocks [54, 21, 34, 45, 38, 50]. For communication circuits, it is critical to understand and model the nonlinear distortions. Some work analyzed and modeled various nonlinear effects [22, 55]. For RF circuits, fast and accurate simulation is highly desired by designers. Some simulation techniques have been developed [31]. In communication system, especially in RF circuits, parasitic effects can have significant impacts on the circuit performance. There are some efforts trying to analyze and model the parasitic effects [26]. From the optimization point of view, some tools were developed to help designer optimize a circuit design based upon a topology starting point [28]. There are also a number of tools and methodologies

that help design some specific blocks, for instance, [27] discussed ADC design and optimization, [29] developed a modeling approach for PLL. On the commercial side, there are also some tools, such as Agilent ADS [1], Ansoft [3], providing models and simulation environment for the analog/RF blocks.

2.3 Platform-Based Approach to Low Power Receiver Design

As mentioned above, there are a number of design and simulation tools that focus on the various design steps from system planning to silicon implementation. They improve the design process here and there, however, there is limited work that addresses the complete design flow and system-level design. Especially, there is a clear need for an efficient approach that can perform design space exploration at the system level and facilitate an effective system design. A new design approach has been developed in this thesis to address these challenges.

2.3.1 Platform-Based Design (PBD)

The methodology should be applicable seamlessly at all levels of abstractions and can capture design constraints and components at each level. In addition, the methodology must favor a system view of the design so that it can deliver an increased productivity and the capability of dealing with multiple design goals, thus always keeping in mind performance, power, reliability and cost as essential characteristics of the final solution.

The *platform based design* methodology has been proposed and applied in several application scenario [47, 49, 48]. In *platform based design*, the design problem is to

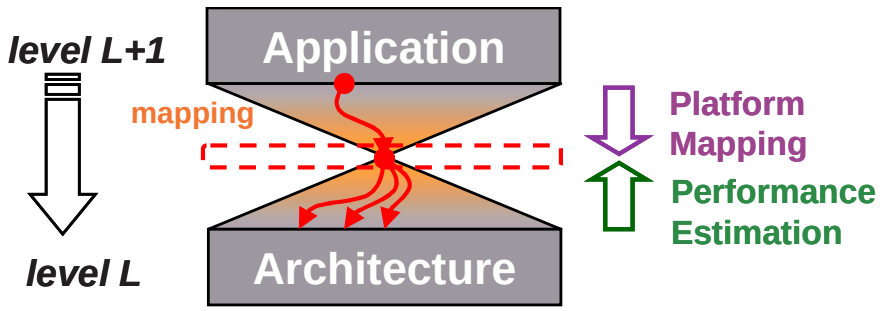


Figure 2.2. Platform-based design (PBD)

identify a stack of platforms that successively map the system from design specification to the lower levels platforms all the way to an actual implementation (e.g. silicon chips). At each layer of the platform stack, the platform needs to be configured to reflect the merits and limitations of the lower level resources. This process not only requires the matching between the functionality and the platform resources, but also keeps the performance sets from the platform resources in the design and analysis loop.

More specifically, we define a *platform* as a library of components, each decorated with a set of methods to estimate performances and behavior and to provide correct ways of composing them. Platforms can be at different level of abstractions, such as custom designed circuits or reconfigurable components (e.g. FPGAs). The design process is a *meet-in-the-middle* approach, as shown in Fig. (2.2). First, a library of components (platform) are characterized by extracting accurate models that include methods to compute physical quantities such as timing and power dissipation. This description of the components is used to offer the designer a way of exploring trade-offs when mapping the application to a legal composition of the platform components, called a *platform instance*. Because platform performances can be readily evaluated, efficient optimization can be carried out to perform *design space exploration*. The

accurate performance models available with platforms guarantee implementability of selected performances so that design can proceed to the next level down the hierarchy.

2.3.2 Platform-Based Receiver Design Flow

It is common that the system architects and the circuit designers focus on the problems coming from their "local" layers. Without digging into the problems in other layers, they can hardly optimize the design at the whole system level, but just limited at the local layers. A company rarely has the bandwidth to explore the systematic cross-layer interactions. An immediate consequence of that is the longer time-to-market, because it is quite usual that lots of manpower is spent on fixing problems caused by the ad-hoc cross-layer interference, iterating the design process, or even re-spinning. A new design approach that can cover the gaps across layers, such as between the communication layer and the circuit layer, will fulfill this need. Furthermore, a more formal design procedure is more preferable in contrast to the intuition-based system partition and constraint propagation.

From another perspective, system verification is very essential to increase the first-pass silicon success. Low level simulation of a large system is quite computationally intensive and should be avoided if possible. This problem becomes more challenging when the system consists of RF, low-frequency analog, and digital blocks. Building behavioral models at a higher abstraction level is considered as an effective solution to tackle the verification challenges.

As we all realized, the highly competitive market pushes for fast development of more powerful wireless communication systems. The design challenges and tight time-to-market can not be successfully conquered only at the circuit level through new topology development and exhaustive simulations. This indeed calls for a new design science, different from traditional design methodologies.

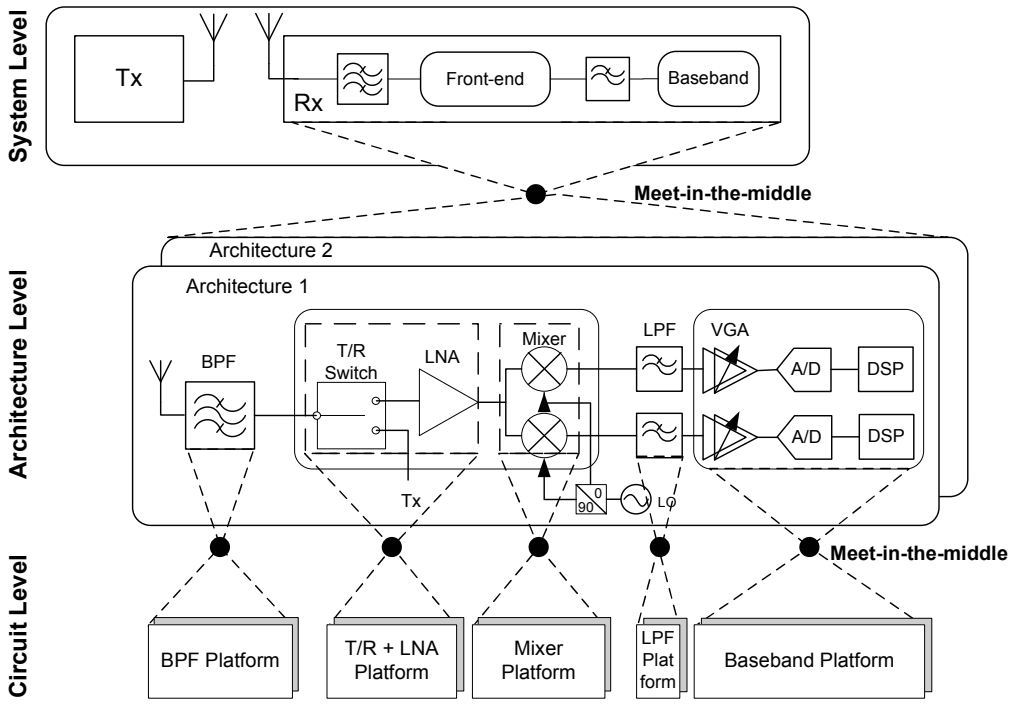


Figure 2.3. Platform-based approach to transceiver design

We propose a platform-based approach to receiver system design, as illustrated in the diagram (Fig. 2.3). The first thing is to define appropriate levels of abstractions that have to be traversed in the design process. These levels are not necessarily common to all receiver designs as they can be customized to the particular application at hand. As an example, we identify three levels of abstraction: a *system level*, an *architecture level* and a *circuit level*. This decomposition is useful to simplify design space exploration by limiting the range of alternatives that must be analyzed. Another consideration to define the proper abstraction levels is for reusing purpose. Reusing an existing platform or an already tested Intellectual Property (IP) block in a new design will greatly increase the chances of first pass success and therefore shrink the design cycle. The circuit platforms compose of different topology choices and also the same topology with different set of design parameters.

In this approach, a top-down process of mapping the receiver system specifica-

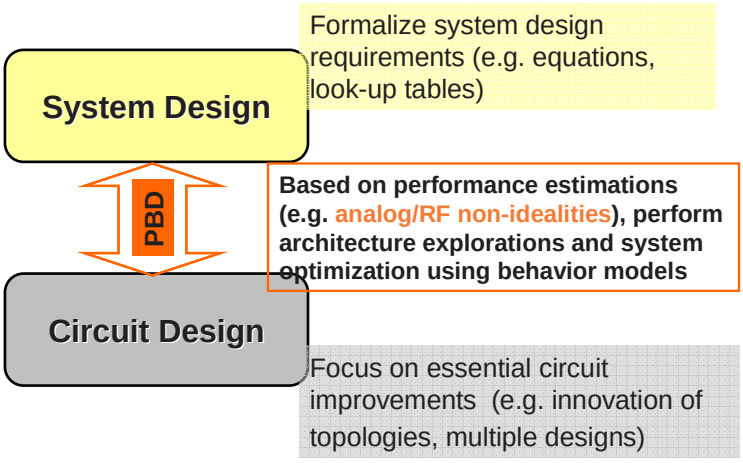


Figure 2.4. Bridge the gap between two design layers.

tions to an architecture and finally to circuit implementations is met by a bottom-up process where the building blocks are characterized in terms of their performance, size and cost. Behavioral models will be introduced as an intermediate level of abstraction to enable efficient performance evaluations (Fig. 2.4). They are parameterized executable models. The model parameters are configured by the lower-level performance obtained from the platform characterization. For example, the performance can be the non-idealities of analog/RF circuits. Lower level implementation details are abstracted away. In this way, the behavioral models are constrained by available implementation architectures. Through the behavioral models, we can make an accurate estimation of the non-idealities and implementation costs (e.g. power consumption, area) on a higher design level. During the top-down phase, design optimization is efficiently performed using behavioral models at system level, allowing effective exploration of the design space.

This proposed receiver design approach automates the design-space exploration procedure at a high abstraction level, which allows to explore a large design space at the beginning of the design cycle. As a result, system engineers can get "the big

picture" of what performance levels can be expected when making different choices along the design process.

In the next chapters, I will explore two application scenarios to demonstrate this proposed design approach. One is a low power front-end design for Ultra Wideband (UWB) receiver; the other is an ultra low power mixed-signal baseband design for wireless sensor networks.

2.3.3 Application Scenarios

1. Low Power Front-end Design for an Ultra Wideband Receiver

As one of the most exciting evolutions of wireless communications, multimedia can be transmitted over a wireless LAN. The wireless connectivity offers more flexibility and new potentials in consumer applications. Growing demands for wireless multimedia transmission are boosting the data rate requirements of wireless communications. Ultra-WideBand (UWB) wireless technology is considered to be a compelling solution to short-range communications (1-10m), which is characterized by high data rates (e.g. hundreds of megabits per second), low power consumption, high robustness to multi-path fading, and low transmission power that allows it to coexist with other wireless technologies.

There are two competing UWB radios under consideration: the direct-sequence impulse radio and the Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) radio. The UWB spectrum released by the FCC spans the range from 3.1GHz to 10.6GHz, with very low power spectral density. For the MB-OFDM UWB radio, as specified by the Multi-Band OFDM Alliance (MBOA) standard [12], the spectrum is divided into five band groups, each composed of 528MHz spaced frequency-hopping bands carrying OFDM signals (Fig. 2.5). Within each band, each carrier is modulated

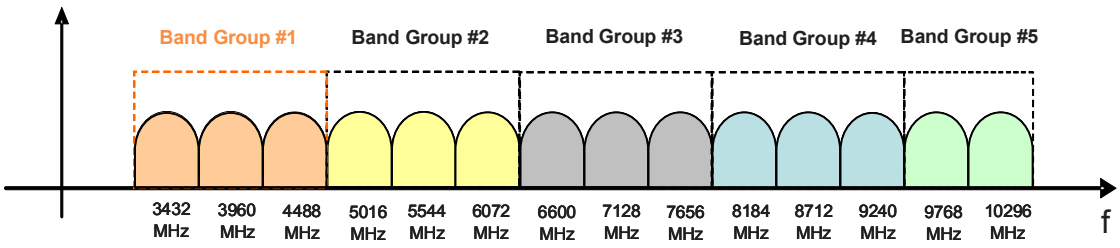


Figure 2.5. MB-OFDM UWB frequency allocation.

by QPSK. In our design, we focus on the MB-OFDM UWB systems operating in the first band group (Mode I), which spans the frequency range from 3.1GHz to 4.8GHz.

Our goal is to design a low-power UWB receiver that should be sufficiently robust against nearby interference. Typically, UWB receivers operating in band group 1 will suffer from potential interference from standards such as 802.11a/b WLAN, WiMax, Bluetooth, and so on. The interference could have significant impacts given the anticipated weak power levels of the UWB signal (maximum power spectral density is -41.3dBm/MHz). A strong narrow band interferer could be as much as 60dB above the UWB signal at the receiver antenna. This situation imposes challenging design requirements on the desensitization, linearity and dynamic range of a UWB receiver.

Design challenges also come from the need for input impedance matching and gain flatness over the broad band (3.1-4.8GHz), the design of a broadband transmit/receive (T/R) switch, and so on. Traditionally, a complex analog/RF design such as above is carried out by a trial-and-error approach and is rarely optimized. We believe that a systematic design space exploration is essential to obtain an optimal system and to improve the state of the art of wireless design technology.

As a short summary, the design of an MB-OFDM ultra-wideband receiver is challenging when we target power consumption minimization while providing enough robustness against the nearby wireless interference. In the remaining part of this thesis, I will present an optimized receiver front-end design starting from system

level analysis down to circuit implementation, using the PBD design methodology. In chapter 3, we investigate the impacts of interference at system level and propose an approach to estimate the inter-modulation products. In chapter 4, we introduce the behavioral models developed at architectural level, which will be used to perform design space exploration based on the PBD methodology. On the circuit level, low power front-end circuits are designed and their performance profiles are generated. In chapter 5, a top-down process of mapping the system-level specifications to circuit-level platforms is conducted by optimization. The optimal design will be reported.

2. Ultra-Low Power Baseband for Wireless Sensor Networks

Wireless sensor network (WSN) has attracted more and more attentions and is very promising to become a growing market in the near future. It opens up many opportunities for ubiquitous sensing and ambient intelligence, such as improved human health monitoring, fire detection in forests, traffic control, environmental observation, etc. Typically, the WSN communication features low data rates with low duty cycles.

An important design requirement of the sensor nodes is the ultra-low power consumption. In almost all applications, replacing batteries at regular instants in battery-powered nodes is inconvenient if not impossible. Some sensor nodes need to scavenge the energy from the environment. For these nodes, it is critical to pursue design solutions that reduce the power consumption as much as possible (e.g. sub-mW level). Designing these wireless nodes in nanometer CMOS technologies with decreasing supply voltages and worsening signal integrity conditions are key challenges that designers face.

Recent progress in ultra-low power transceivers for sensor networks has reduced the receiver's power consumption to the level below a milliwatt and the overall

transceiver implementation volume to below $1mm^3$ [35, 36]. This new radio utilizes a combination of micro-electromechanical (MEMS) devices and standard CMOS processes. The radio baseband (demodulation and synchronization) circuitry must be extremely small and exhibit very low power dissipation. This leads to fundamentally different baseband design approaches than the ones used in standard radios. To eliminate the need for replacing or recharging system batteries, all of the energy dissipated by the electronics must be scavenged from the environment [41][44]. This limits the average power dissipation of the sensor node to around 100μW. One of the most challenging aspects of this vision is integrating a low power RF communication link capable of connecting the autonomous nodes into a large, ad-hoc network. The baseband design in this thesis focuses on the demodulation synchronization hardware of such a system.

We believe that the constraints introduced above can only be met within a reasonable design time if a system level design methodology is used. In the following chapters of this thesis, I will explain how we leverage the platform based approach to design the baseband section for the low power Picoradio transceivers. Starting from the RF interface, our design process begins with a system level phase focusing on the functional design. The PBD approach is used to explore two alternative solutions: a predominantly digital one and a predominantly analog one. To validate the functional aspect of the design and explore the different analog vs. digital partitions, prototype implementations based on configurable platforms including an FPGA and a Field Programmable Analog Array (FPAA) are derived using the PBD approach. Finally, after evaluating performances and extrapolating results to a custom design, we map the system level description to an ultra-low power silicon implementation in a 0.13μm CMOS process.

Chapter 3

System Level Design

3.1 System Exploration

An effective system exploration is not only important to reduce the time-to-market. It can also realize more significant overall power savings than the power reduction that circuit design techniques can achieve in each individual block. There are numerous exploration concerns, whose weights vary in different wireless systems. During the system level exploration, we first need to identify the critical concerns that will generate important impacts on system performance and overall power consumption in a specific system context. In this section, I mainly discuss two typical concerns in wireless receiver systems.

3.1.1 Functionality Partitioning: Digital vs. Analog

Wireless receiver systems compose of RF front-end and low frequency back-end. For the low frequency part, the function partitioning can vary substantially, that consequently requires quite different type of corresponding architectures. The entire system design will benefit from a proper system-level partitioning, that includes parti-

tioning of the function implementation between the hardware and software domains, also includes partitioning of the signal processing between the digital and analog domains. This is one of the main concerns in the WSN baseband design.

The mostly-digital approach is very typical in most digital wireless receivers, where minimal functionalities are performed in the analog domain. After the RF front-end down-conversion, the incoming signal is digitalized by ADC and all further signal processing is conducted in digital domain. This brings about a main benefit, i.e. the digital signal processing algorithms usually offer higher flexibility and better integrity than the analog processing. A typical design challenge of a mostly-digital solution is to design an ADC with stringent performance requirements. Without pre-processing the received signal in analog domain, the ADC is required to provide a high resolution to accommodate for the fact that the down-converted signal at the ADC input has a very high dynamic range. The increased ADC resolution requirements will be translated to a considerable increase of overall power dissipation of the receiver. That is the main reason motivating the designers to consider the hybrid or mostly-analog solutions.

A different signal partitioning is that more signal processing jobs are performed in the analog domain, that is called hybrid approach (comparable amounts of digital and analog) or mostly-analog approach (analog is dominant). Though the mostly-analog approach is not widely employed, there are some successful design examples. A typical usage is to insert some analog blocks between the RF front-end and the ADC so that the down-converted signal is pre-processed before the digitalization conversion. Even further, part of the baseband tasks can be moved to the analog domain. The big advantage is the reduced performance requirements on ADC design, that consequently leads to a significant power savings. One of the disadvantages that restricts its wide adoption is that the baseband functionalities (e.g. AGC, channel equalization, etc.) and the algorithms (e.g. maximum likelihood algorithm) require complicated circuitry if implement in analog domain. The operations of most digital

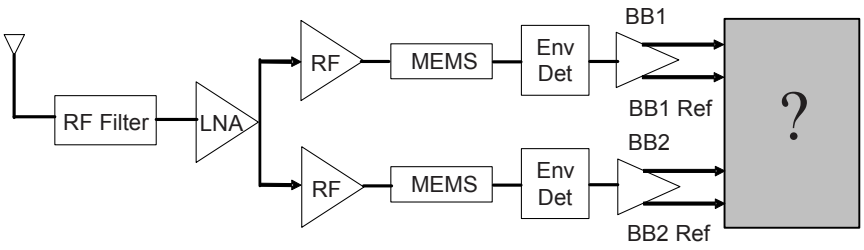


Figure 3.1. Ultra-low power receiver for wireless sensor networks (WSNs)

modulation schemes can be performed elegantly in digital domain, while same tasks become very difficult if map to analog domain. Moreover, due to the existance of various noise and non-idealities in analog circuits, the precision or even the correctness of the advanced signal processing algorithms can be corrupted. Therefore, a hybrid or mostly-analog approach requires a careful evaluation of the system, including the modulation scheme, the RF front-end, the baseband signal processing requirements, etc. In order to take advantage of the power savings in hybrid or mostly-analog solutions, the algorithms in mostly-digital solution need to be modified or a different algorithm need to be developed in order to be well mapped to the analog architectures.

The Picoradio design targets for an extremely low power system for use in wireless sensor network applications. This system operates at a maximum data rate of 50kbit/s, and a non-coherent modulation scheme is used. Simplification is considered as an effective strategy to achieve the extremely low power consumption. Generally, in order to correctly demodulate and detect the incoming signal, a digital communications receiver needs to perform a set of signal processing tasks, such as symbol synchronization, carrier phase/frequency recovery, automatic gain control (AGC), channel equalization, etc. Among the tasks, symbol synchronization is to deal with the timing offset that is caused by the mismatches between the transmitter and receiver oscillators and by the unknown time of flight between the transmitter and receiver.

As a part of the simplification strategy, an MEMS-based RF transceiver is designed to operate at 2GHz [36]. The high-Q MEMS channel-select filter greatly suppresses the out-of-band interference. The radio employs a self-mixing signal down conversion using an envelope detector. Due to the self-mixing process, frequency and phase information is removed from the incoming signal. Considering this MEMS-based architecture, a simple ON/OFF keying (OOK) modulation scheme is chosen. It allows simple detection on the receive side and efficient modulation on the transmit side, and has been proved to be very energy efficient for wireless sensor network systems. Since the startup time of the transmitter is fast, the entire transmitter is cycled on/off between transmitted symbols. Thus, the entire transmitter is powered down while transmitting a zero, effectively reducing the energy consumption of the transmitter by a factor of two.

An alternating 1010 training sequence header is used for synchronization. For simplification purpose, the main task of the baseband is just to perform the symbol synchronization. The synchronization requirements and the baseband complexity have been simplified by the radio RF front-end and the modulation scheme. For the OOK modulation, only timing and amplitude are required to be detected during synchronization. No AGC is involved, and equalization is also avoided. Such a baseband system is a suitable case to explore different signal partitioning, because the simplified synchronization requirements are able to be implemented in digital domain and in analog domain as well.

In order to achieve a synchronization system with short header length and extremely low power consumption, two different signal partitions are investigated. In the digital scheme, the signal from the envelope detector goes directly into an the analog-to-digital convertor(ADC). All the synchronization tasks are performed in the digital domain. The digital scheme with an 8-bit ADC is elaborated in [8]. Considering that ADC is a dominant power consumer, another scheme is designed to avoid

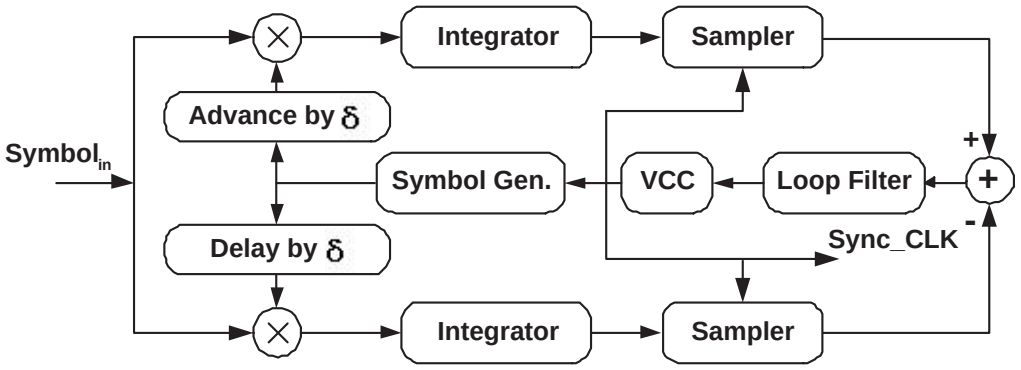


Figure 3.2. Block diagram of Early-Late Gate synchronizer

the ADC employment. In this scheme, the synchronization functionality is mainly implemented in analog circuits, with digital control. This thesis will be focused on the mostly-analog scheme.

An Early-Late Gate synchronization scheme is employed to demodulate the OOK modulation. The block diagram is shown in Fig. 3.2. The demodulator works by correlating the incoming signal with two copies of an internally generated symbol, one delayed by δ and one anticipated by δ. If the internal symbol clock is correctly synchronized, each integrator will integrate half of the symbol, so that no error signal is generated. If the symbol clock is leading (lagging), negative feedback is applied through combining the integration paths until synchronization is achieved [40].

This synchronization algorithm allows different implementations, ranging from a completely analog one (e.g. a principle implementation of the block diagram in Fig. 3.2) to a completely digital one (after the incoming signal has been sampled and converted). We explored the different possibilities of partitioning the design between analog and digital, evaluating performances as accurately as possible before final implementation on silicon. To achieve this, we modeled the algorithm at a high level of abstraction in Matlab/Simulink, and also in Metropolis (will be discussed in section 3.2.3). We excluded the all-analog solution from exploration because we needed

some flexibility in the control algorithm to adjust for variable bit rates. A mostly digital solution with digitization occurring immediately after down conversion, and a hybrid solution (predominantly analog processing) were investigated where signal processing is performed in the analog domain using a 1 bit converter (comparator) at the end of the sampler blocks to feed a digital control algorithm. The detailed investigation will be introduced in section 4.1.2.

3.1.2 System Budget: Robustness vs. Low Power

To design a low power receiver, a critical task is trading off the system requirements, including nonlinearities, Noise Figure (NF), implementation loss, gain, etc. If we target to achieve low power consumption and simultaneously provide enough robustness against the interference, we need to perform a careful system budget. In order for the architect to make the appropriate trade-offs, the various estimations in the system budget must be accurate enough. Therefore, minimizing power consumption of a robust design implies the need of thorough investigation and accurate estimation of the interference influences on the receiver's performance. This is the design scenario for our UWB receiver.

To achieve co-existence with other wireless technologies, UWB receivers should exhibit robust behavior against nearby interference. Typically, UWB receivers operating in band group 1 will suffer from the potential interference from standards such as 802.11a/b WLAN, WiMax, Bluetooth, and GSM1900 as shown in Fig. 3.3. The interference could have significant impacts given the anticipated weak power levels of the UWB signal (maximum power spectral density is -41.3dBm/MHz). A strong narrow band interferer could be as much as 60dB above the UWB signal at the receiver antenna. This situation imposes challenging design requirements on the linearity performance and the dynamic range of a UWB receiver.

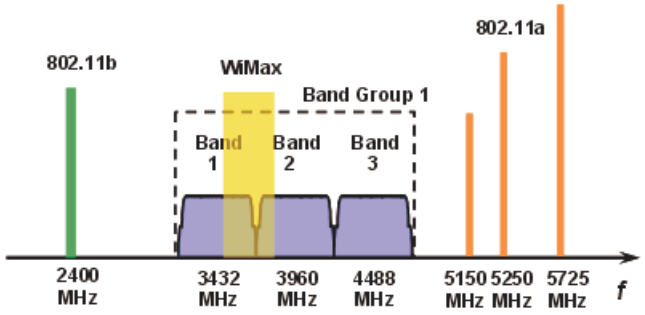


Figure 3.3. Interference scenario around UWB band group 1.

The inter-modulation and cross-modulation products of interferences introduced by nonlinearities of the receiver could significantly degrade system performance, and should be properly estimated when determining system design specifications. In absence of accurate estimation of distortion effects, designers usually set large design margins to deal with uncertainty, resulting in over-design with power consumption higher than it would be required if accurate analysis had been performed.

Usually, system designers could estimate the linearity performance by simulating the actual system. A more elegant approach is to use analytical techniques. A traditional two-tone approach is widely used to estimate nonlinear effects. However, for MB-OFDM UWB systems, performance estimation using the two-tone approach is not accurate enough. To resolve this difficulty, we need to develop a new approach to estimate the interference distortion products accurately.

To accommodate for the system tradeoff to achieve the low power design requirement and enough robustness, we carry out a thorough analysis on the intermodulation distortions of typical interferences for an MB-OFDM UWB receiver operating in band group 1, showing the resulting IMD and XMD products. As a result, the narrow-band two-tone approach can be properly adjusted to characterize UWB systems accurately. For that purpose, we provide an adjustment factor that is determined through analytical computations. Consequently, system designers could still take advantages of

the easy-to-use two-tone technique in MB-OFDM UWB systems without sacrificing accuracy. This technique is detailed in section 3.2.1.

3.2 Model and Validation

There are quite a few approaches to analyze, model, and simulate a wireless receiver system. Among the amounts of modeling tools, the widely used ones are Matlab/Simulink [4], Verilog/VHDL AMS [7] [6], Ptolemy II [5], etc. In this section, I will focus on the approaches and the corresponding modeling environment that are adopted in the Picoradio baseband design and the UWB front-end design. For the UWB system, the analytical expressions for various interference scenarios are derived and then validated by simulation. Based on this analysis, we demonstrate how the two-tone technique can be adjusted to provide accurate distortion estimations for MB-OFDM UWB systems. For the Picoradio baseband system, we model and validate the symbol synchronization algorithm in a new heterogenous design environment called Metropolis.

3.2.1 Analytical Approach

Analytical techniques have been developed to determine the power density spectrum (PSD) of an OFDM signal distorted by nonlinearities [53] [43] [30]. However, most of them focus on the crosstalk between OFDM sub-carriers and the resulting signal deterioration. There are very few studies on the distortion impacts of interference signals [9]. In this section, we present a statistical approach to calculate the interference distortion products introduced by receiver's nonlinearities. Specifically, we focus on the inter-modulation (IMD) and cross-modulation (XMD) effects.

The validity of the analytical expressions will be verified by simulation results under various interference scenarios.

As shown in Fig. 3.3, various types of interference should be taken into account: Narrow-Band Interferences (NBI), such as the ones produced by 802.11a/b, and Wide-Band Interference (WBI), such as the ones caused by other UWB transmitters. Due to the nonlinear behaviors of UWB receivers, the distortion products of these interferences could fall into the band of interest, degrading the system SNR. Considering the combination of two NBIs, since the in-band IMD products corrupt only a small fraction of sub-bands (e.g. 802.11a/b WLAN has a 20MHz bandwidth), we neglect their contributions to SNR degradation. From this point of view, UWB has the potential of tolerating distortions of NBIs. In this work, we focus on the IMD products from NBI and WBI as well as from WBI and WBI. For those strong NBIs, we also consider their possible desensitization effects when performing the system budget analysis.

I. Nonlinear Systems

Volterra series are often used to model the behavior of a nonlinear system [43]. For a memoryless weakly nonlinear component, we can represent the input/output behavior by a truncated power series around the *dc* operating point, where all the coefficients are frequency-independent. This model is being used to approximate the behavior of a wide range of components, such as LNAs, mixers, and baseband amplifiers. The coefficients could be related to the component's performance as follows:

$$S_{out} = k_1 \cdot S_{in} + k_2 \cdot S_{in}^2 + k_3 \cdot S_{in}^3$$

$$\begin{cases} k_1 = Gain \\ k_2 = \frac{k_1}{IIP2} \\ k_3 = \frac{4}{3} \cdot \frac{k_1}{IIP3^2} \end{cases} \tag{3.1}$$

where $IIP2$, $IIP3$ are input-referred second order and third order intermodulation intercept points, characterizing the nonlinearity performance.

The distortion products introduced by the second-order term are usually mapped to bands far from the wanted UWB signal passband. Therefore, we will not consider the second order nonlinearities in this work. The third-order term is responsible for most of the unwanted in-band IMD products. In this work, we only address third order nonlinearities, but we are not limited to this: our approach can be extended to higher-order nonlinear terms.

II. The Traditional Two-tone Approach

For many years, a two-tone test has been widely used to characterize nonlinearities and estimate the distortion effects in narrow-band systems. In this approach, an input stimulus consisting of two pure tones at f_1 and f_2 is fed into the system, and the outputs at specific frequencies are computed. Given the power of two-tone (f_1, f_2) input signals, P_{in_1} and P_{in_2}, the output-referred P_{IM3_out} at $(2 \cdot f_1 \pm f_2)$ can be related to IIP3 as:

$$P_{IM3\_out} = 2 \cdot P_{in_1} + P_{in_2} - 2 \cdot IIP3 + Gain \ [dB] \tag{3.2}$$

When applying a two-tone test to characterize receiver's distortion, the inputs are interference signals after the attenuation of the pre-select filter, which is usually inserted between the antenna and the receiver chain to limit the out-of-band interference that might otherwise desensitize the receiver.

When dealing with a UWB system, designers still use the well-developed two-tone approach in system budget analysis, in simulations, and in chip measurements. For instance, the IIP3 is measured by setting the first tone in the 5.8GHz ISM band

and the second tone in the lower UNII band at 5.2GHz. However, this approach is accurate only for narrow-band systems because the signals are assumed to have the same behavior over the entire bandwidth so that they could be approximated by single-frequency tones. For a UWB signal, what happens at a specific in-band frequency may not accurately represent what happens over the entire bandwidth. The two-tone estimations only take into account the interference power. This leads to an inaccurate estimation of the interference impacts. In UWB systems, the interference properties, including the spectral bandwidth and frequency locations, have influence on the distortion products. Due to the statistical behaviors of OFDM signals, the UWB systems should be analyzed by calculating the signal power spectrum.

III. Our Statistical Approach

An OFDM signal consists of the parallel transmission of several signals that are modulated at equally-spaced carrier frequencies f_n [40], i.e.,:

$$I(t) = g_T(t+\phi) \sum_{n=-\frac{N}{2}}^{\frac{N}{2}} (i_n \cos((\omega_c + \omega_n)t + \psi)) \tag{3.3}$$

$$Q(t) = g_T(t+\phi) \sum_{n=-\frac{N}{2}}^{\frac{N}{2}} (q_n \sin((\omega_c + \omega_n)t + \psi)) \tag{3.4}$$

$$x(t) = I(t) + Q(t) \tag{3.5}$$

where $\omega_n = 2\pi f_n$, N is the total number of OFDM sub-carriers, i_n and q_n are the real and imaginary parts of the baseband QPSK, $f_c = \frac{\omega_c}{2\pi}$ is the band center frequency, ϕ and ψ are random phases. $f_n = n \cdot \Delta f$, where Δf is the subcarrier frequency spacing. With the constellation point $c_n = i_n + jq_n$, the corresponding complex envelope is $g_T(t+\phi)\sum_n c_n e^{j\omega_n t}$. If the OFDM symbol total duration is T, $g_T(t)$ is a rectangular function defined as:

$$g_T(t) = rect[\frac{t}{T}] = \sqrt{\frac{1}{T}}, \quad \frac{-T}{2} < t < \frac{T}{2} \tag{3.6}$$

$$= 0, \quad elsewhere \tag{3.7}$$

With the transmitted signal power of σ^2, the single-sided power spectral density of an OFDM signal could be expressed by [43]:

$$PSD(f) = \sigma^2 \sum_{n=-\frac{N}{2}}^{\frac{N}{2}} sinc^2((f - (f_c + n\Delta f))T) \tag{3.8}$$

When the number of sub-carriers N is high, according to the central limit theorem, we hypothesize that the discrete time samples of an OFDM signal can be considered as zero-mean Gaussian random variables. Consequently, an OFDM signal can be modeled as a cyclostationary Gaussian stochastic process. Based on statistical signal processing, we could derive the functions for the power density spectrum of the distortion products. The influence of interference will be modeled as an equivalent power increase in the noise floor.

- **WBI and NBI**

Suppose the MB-OFDM UWB receiver is operating in band 1, spanning the range from 3168MHz to 3696MHz. We first analyze the inter-modulation products from a narrow-band interference and another MB-OFDM transmitter. WiMax operates in 2.4GHz, 3.5GHz and 5.8GHz bands. A WiMax transmitter in the 3.5GHz band could be an in-band or adjacent-band interference source to the UWB receiver operating in band group 1. Other than that, the NBI could also come from the out-of-band source, such as IEEE802.11a. Though it is not in the receiver's signal band, the IMD or XMD products do fall in band. In UWB communication, the OFDM symbols are transmitted through different frequency slots according to TFI (Time-Frequency Interleaving) patterns. A UWB receiver might suffer from nearby UWB transmitters in different TFI patterns. This is the main source of WBI considered in this work. In UWB systems, since the transmitter and the receiver are not turned on simultaneously, the transmitter leakage is not a major interference source (as in WCDMA).

The WBI mainly comes from other nearby UWB transmitters operating in different TFI (Time-Frequency Interleaving) patterns.

We model the NBI as a single-tone sinusoid signal, and the WBI as defined in (3.5):

$$\begin{aligned} S_{NBI}(t) &= A_{NBI}\cos(\omega_{NBI}t+\theta) \\ S_{WBI}(t) &= I_{WBI}(t)+Q_{WBI}(t) \\ &= g_T(t+\phi)\sum_{n=-\frac{N}{2}}^{\frac{N}{2}}[i_n\cos((\omega_{WBI}+n\Delta\omega)t+\psi) \\ &\quad +q_n\sin((\omega_{WBI}+n\Delta\omega)t+\psi)] \end{aligned} \tag{3.9}$$

where A_{NBI}, $f_{NBI}=\frac{\omega_{NBI}}{2\pi}$, θ are the amplitude, center frequency, and random phase of the NBI. When S_{NBI} and S_{WBI} pass through a receiver front-end with nonlinearities, according to (3.1), the third order nonlinear outputs are represented as:

$$S_{3rd}(t)=k_3[A_{NBI}\cos(\omega_{NBI}t+\theta)+[I_{WBI}(t)+Q_{WBI}(t)]]^3 \tag{3.10}$$

By representing the OFDM signal as a sum of carrier tones, we could examine the frequency translation behavior as we do in the two-tone approach. We only count the IMD terms that will fall into the band of interest, therefore, the contribution consists of:

$$S_{IM3}(t)=3k_3A_{NBI}\cos(\omega_{NBI}t+\theta)[I_{WBI}(t)+Q_{WBI}(t)]^2 \tag{3.11}$$

Expanding this expression, and neglecting out-of-band terms, we obtain the distortion products that will be responsible for the SNR degradation. There are two different cases:

Case I: As shown in Fig. 3.4, the NBI is inside (such as WiMax, f_{NBI}=3.5GHz) or adjacent to the band of interest. This case actually is cross-modulation distortion (XMD), i.e. the transfer of modulation from the WBI to the NBI due to nonlinearities. Among the distortion components expanded from (3.11), we are only interested in those adjacent to f_{NBI}.

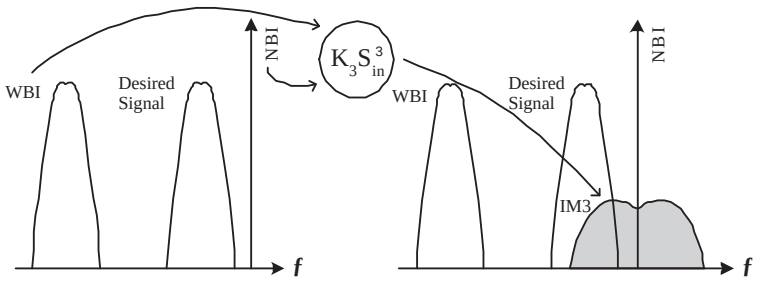


Figure 3.4. XMD products of NBI (adjacent to the desired band) and WBI.

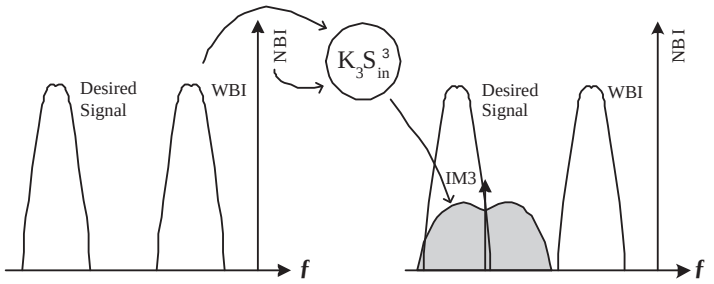


Figure 3.5. Third order IMD products of NBI and WBI.

Case II: As shown in Fig. 3.5, the NBI are out-of-band interferences (such as 802.11a, f_{NBI}=5.3GHz). We only consider the resulting IMD terms adjacent to $2f_{WBI} - f_{NBI}$, that will have effects on the desired signal band.

Next, we take case I as an example to derive the power spectral density function. According to the Wiener-Khinchin theorem, the power spectral density could be obtained by taking the Fourier transform of the autocorrelation function, $R(\tau)$, of the signal if the signal can be treated as a stationary random process [40]:

$$PSD_{IM3}(f) = \int_{-\infty}^{\infty} R_{IM3}(\tau) e^{-j2\pi f\tau} d\tau \tag{3.12}$$

The autocorrelation function of a wide-sense-stationary random process is defined by the expectation operation $E\{\cdot\}$:

$$R_{IM3}(\tau) = E\{S_{IM3}(t) S_{IM3}(t+\tau)\} \tag{3.13}$$

Without loss of generality, we set $t = 0$ when applying the autocorrelation operation to the third order IMD product $S_{IM3}(t)$ as shown in (3.11). We obtain:

$$\begin{aligned} R_{IM3}(\tau) &= E\{S_{IM3}(0)S_{IM3}(\tau)\} \\ &= 9k_3^2 A_{NBI}^2 E_\theta\{cos(\theta)cos(\omega_{NBI}\tau + \theta)\} \\ &\cdot E_{\phi,\psi,i,q}\{I_{WBI}^2(0)I_{WBI}^2(\tau) + Q_{WBI}^2(0)Q_{WBI}^2(\tau) \\ &+ I_{WBI}^2(0)Q_{WBI}^2(\tau) + Q_{WBI}^2(0)I_{WBI}^2(\tau) \\ &+ 4I_{WBI}(0)Q_{WBI}(0)I_{WBI}(\tau)Q_{WBI}(\tau)\} \end{aligned} \tag{3.14}$$

Since the coefficients of the nonlinear behavioral model are time-independent and the OFDM signal autocorrelation function is periodic in time, the autocorrelation function of the IMD products is a cyclostationary stochastic process. Therefore, the power spectral density of S_{IM3} could be obtained by making the Fourier transforms of its autocorrelation function.

Since the complex values c_n are statistically independent and the in-phase modulation i_n and the in-quadrature q_n are uncorrelated random variables, we have the following statistical properties of i_n and q_n [9]:

$$E\{i_k^n\} = E\{q_k^n\} = 0, \quad \text{when } n \text{ is odd} \tag{3.15}$$

$$= 1, \quad \text{when } n \text{ is even} \tag{3.16}$$

$$E\{i_k q_l\} = E\{i_k\}E\{q_l\} = 0 \tag{3.17}$$

$$E\{i_k i_l\} = E\{q_k q_l\} = \delta_{kl} \tag{3.18}$$

$$E\{i_k i_l q_m q_n\} = \delta_{kl}\delta_{mn} \tag{3.19}$$

where δ_{kl} is the Kronecker delta. With these properties, some terms in (3.14) are zeros, and the autocorrelation function can be simplified (detailed derivation is in Appendix A.1). The resulting components adjacent to f_{NBI} are:

$$\begin{aligned} &R_{IM3}(\tau) = \tfrac{9}{4}k_3^2 A_{NBI}^2 \cdot R_{g^2}(\tau) \cdot \textstyle\sum_{m=-\frac{N}{2}}^{\frac{N}{2}} \sum_{n=-\frac{N}{2}}^{\frac{N}{2}} \\ &\{\cos(\omega_{NBI} + (m-n)\Delta\omega)\tau + \cos(\omega_{NBI} - (m-n)\Delta\omega)\tau\} \end{aligned} \tag{3.20}$$

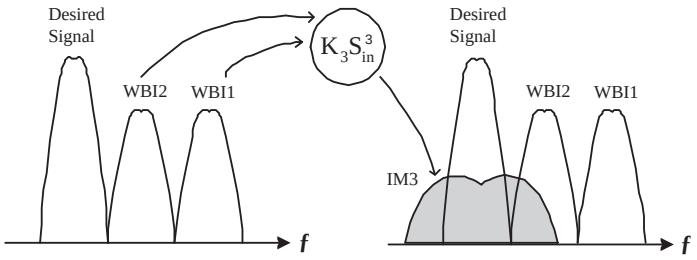


Figure 3.6. Third order IMD products of WBI and WBI.

We first calculate the autocorrelation, $R_{g^2}(\tau)$, of the function $g^2(t+\phi) = rect^2[\frac{t+\phi}{T}]$ and its Fourier transform (details are in Appendix A.1):

$$R_{g^2}(\tau) = E_\phi\{rect^2[\frac{\phi}{T}]rect^2[\frac{\tau+\phi}{T}]\} \tag{3.21}$$

$$\int_{-\infty}^{\infty} R_{g^2}(\tau)e^{-j2\pi f\tau}d\tau = sinc^2(fT) \tag{3.22}$$

Applying Fourier transforms on $R_{IM3}(\tau)$ in (3.20), the resulting PSD will be the Fourier transforms of $R_{g^2}(\tau)$ convoluted with a sequence of Dirac pulses located at frequencies $\sum_m \sum_n [f_{NBI} \pm \Delta f(m-n)]$. When the average transmitted signal power of WBI is σ_{WBI}^2, the single-sided power spectral density of IM3 products around f_{NBI} is calculated as:

$$\begin{aligned} PSD_{IM3}(f) &= \tfrac{9}{4}k_3^2 A_{NBI}^2 \sigma_{WBI}^4 \\ &\cdot \sum_{m=-\frac{N}{2}}^{\frac{N}{2}} \sum_{n=-\frac{N}{2}}^{\frac{N}{2}} sinc^2((f-(f_{NBI}+(m-n)\Delta f))T) \end{aligned} \tag{3.23}$$

To improve the computation efficiency, we derived the total number of terms at each frequency $f_l = f_{NBI} + l\Delta f$, $l \in [-N, N]$, which turns out to be $(N- \mid l \mid +1)$. A simplified expression can be derived by replacing the double summations with an equivalent single summation:

$$\begin{aligned} PSD_{IM3}(f) &= \tfrac{9}{4}k_3^2 A_{NBI}^2 \sigma_{WBI}^4 \\ &\cdot \sum_{l=-N}^{N} [(N- \mid l \mid +1) \cdot sinc^2((f-(f_{NBI}+l\cdot\Delta f))T)] \end{aligned} \tag{3.24}$$

- **WBI and WBI**

In UWB systems, since the transmitter and receiver are not turned on simultaneously, we need not worry about the transmitter leakage as a major interference source (as WCDMA does). As mentioned before, the WBI mainly comes from other competing UWB transmitters. For example, as shown in Fig. 3.6, the third order IMD product of the UWB interference in the second band and the third band will fall into the first band.

Following a procedure similar to the one we performed for NBI and WBI, we derived the PSD function for the third order IMD products of WBI and WBI (detailed derivation is in Appendix A.2):

$$\begin{aligned} &PSD_{IM3}(f) = \tfrac{9}{4}k_3^2 \cdot \sigma_{WBI_1}^2 \sigma_{WBI_2}^4 T \cdot \{ \\ &\textstyle\sum_{m=-\frac{N}{2}}^{\frac{N}{2}} \sum_{n=-\frac{N}{2}}^{\frac{N}{2}} \sum_{k=-\frac{N}{2}}^{\frac{N}{2}} S((f - (2f_{WBI_2} - f_{WBI_1} + (m+n-k)\Delta f))T) \texttt{--(A)} \\ &-\tfrac{1}{2} \textstyle\sum_{n=-\frac{N}{2}}^{\frac{N}{2}} \sum_{k=-\frac{N}{2}}^{\frac{N}{2}} S((f - (2f_{WBI_2} - f_{WBI_1} + (2n-k))\Delta f)T)\} \texttt{-----(B)} \end{aligned} \tag{3.25}$$

where function $S(fT)$ is defined as $S(fT) = sinc^2(fT) * sinc^2(fT)$. To simplify the computation, when N is a large value, we can make an approximation by ignoring term (B). We also derived the total number of terms in (A), Λ_l, at each frequency $f_l = 2f_{WBI2} - f_{WBI1} + l \cdot \Delta f$, $l \in [-\frac{3N}{2}, \frac{3N}{2}]$. The simplified PSD calculation with a single summation is:

$$\begin{aligned} &PSD_{IM3}(f) = \tfrac{9}{4}k_3^2 \sigma_{WBI1}^2 \sigma_{WBI2}^4 T \\ &\cdot \textstyle\sum_{l=-\frac{3N}{2}}^{\frac{3N}{2}} [\Lambda_l \cdot S((f - (2f_{WBI2} - f_{WBI1} + l \cdot \Delta f))T)] \end{aligned} \tag{3.26}$$

$$\Lambda_l = \begin{cases} \frac{1}{2}(l + \frac{3N}{2} + 1) \cdot (l + \frac{3N}{2} + 2), & -\frac{3N}{2} \le l \le -\frac{N}{2} \\ \frac{1}{2}(6N(l + \frac{3N}{2}) - 2(l + \frac{3N}{2})^2 - 3N^2 + 3N + 2), & -\frac{N}{2} < l \le \frac{N}{2} \\ \frac{1}{2}(3N - (l + \frac{3N}{2}) + 1)(3N - (l + \frac{3N}{2}) + 2), & \frac{N}{2} < l \le \frac{3N}{2} \end{cases} \tag{3.27}$$

In summary, power spectrum density (PSD) of the UWB distortion products can be derived using the following procedure:

- Feed the interference signals into a nonlinear model (e.g. a third-order polynomial), and derive the analytical IMD products in time domain.
- According to the Wiener-Khinchin theorem, PSD is derived by taking the Fourier transform of the IMD autocorrelation function.
- The autocorrelation functions are simplified using the statistical properties of the uncorrelated random coefficients, i_n and q_n in (3.5).

IV. Two-tone Approach Adjusted for UWB

As shown in equation 3.2, the two-tone IM3 results are determined by the interference power and $IIP3$, while the actual PSD analysis shows that the IM3 products depend also on the bandwidth and frequency locations of the interferences. Using the expressions we derived, (3.24) and (3.26), designers could make estimations quickly and accurately using numerical calculations instead of simulating the actual system. Considering the two-tone technique is a preferred method by designers, we show how the two-tone IM3 estimation in (3.2) could be adjusted so that it could be applied to UWB systems.

In the two-tone approach (3.2), the output-referred power P_{IM3_out} at frequency $2f_2 \pm f_1$ is:

$$P_{IM3\_out} = (\frac{3}{4}k_3)^2 \cdot P_{in1} \cdot P_{in2}^2 \tag{3.28}$$

Take the case of NBI and WBI (3.24) as an example. Only the distortion products falling into the band of interest contribute to the power increase of the noise floor, and should be counted into the power estimation. Given the interference band locations, the band overlap between their IM3 spectrum and the desired UWB band (Fig. 3.7),

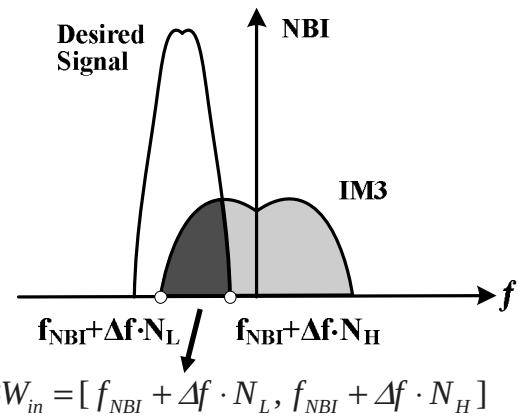


Figure 3.7. For approximation of IMD products

$BW_{in} = [f_{NBI} + \Delta f \cdot N_L,\ f_{NBI} + \Delta f \cdot N_H]$, could be easily determined. Assume a frequency interval *df* is used in the analytical power estimation, we could calculate the total in-band IM3 power from the $PSD_{IM3}(f)$, $P^{+}_{IM3} = \sum_{f \in BW_{in}}[df \cdot PSD_{IM3}(f)]$. We define a variable γ_{IM3}:

$$\gamma_{IM3} = \sum_{f \in BW_{in}}[df \cdot \sum_{l=-N}^{N}[(N- \mid l \mid +1) \cdot sinc^2((f - (f_{NBI} + l \cdot \Delta f))T)]]$$

$$P^{+}_{IM3} = \tfrac{9}{4} k_3^2 A^2_{NBI} \sigma^4_{WBI} \cdot \gamma_{IM3} \tag{3.29}$$

We define the adjustment factor as $\delta P_{IM3} = P^{+}_{IM3}/P_{IM3\_out}$. Comparing (3.29) to (3.28), with $P_{in1} = A^2_{NBI}/2$, $P_{in2} = N \cdot \sigma^2_{WBI}$, we observe that the variation (δP_{IM3}) between our statistical approach and the two-tone estimation is:

$$\delta P_{IM3} = P^{+}_{IM3}/P_{IM3\_out} = 8\frac{\gamma_{IM3}}{N^2} \tag{3.30}$$

Following the same procedure, variations in similar format could be obtained for other interference conditions (3.26). We believe that UWB system designers will be interested in these variations. Generally, the IMD or XMD power adjustment (δP_{IM3}) is determined by two factors, a constant and a summation result, both of which do not vary when the interferences change to different power levels. Therefore, given

the interference band locations, the numerical summation of the in-band PSD terms, γ_{IM3}, needs to be computed only once. With this one-time off-line computation, the two-tone technique could be used to characterize the linearity performance and to predict the resulting SNR degradation accurately.

To improve the execution efficiency further, we make an approximation to calculate the total in-band IMD power, with almost no loss of accuracy. Since the energy of $sinc^2(f - f_0)$ function is very concentrated around $f = f_0$, one approximation is to assume that its power totally falls into the overlap bandwidth BW_{in} if $f_0 \in BW_{in}$. We know the total power:

$$P_{sinc} = \int_{-\infty}^{\infty} sinc^2(fT)df = 1/T \tag{3.31}$$

Therefore, if we define Ω to be the total number of $sinc^2((f - f_l)T)$ functions satisfying $f_l = (f_{NBI} + l \cdot \Delta f) \in BW_{in}$, $BW_{in} = [f_{NBI} + \Delta f \cdot N_L,\ f_{NBI} + \Delta f \cdot N_H]$, the in-band IM3 portion in (3.29) can be approximated:

$$\begin{aligned} \gamma_{IM3} &= \textstyle\sum_{l=N_L}^{N_H} [(N - \mid l \mid +1) \cdot \Delta f \cdot sinc^2((f - f_l)T)] \\ &\simeq \Omega \cdot P_{sinc} \\ &= \tfrac{\Omega}{T} \end{aligned} \tag{3.32}$$

$$\Omega = \begin{cases} \frac{1}{2}(N - |N_H| + 1)(N - |N_H| + 2), \\ \qquad \text{when } N_L = -N,\ -N \le N_H \le 0 \\ (N+1)^2 - \frac{1}{2}(N_L^2 + N_H^2 + N), \\ \qquad \text{when } -N \le N_L \le 0,\ N_H = N_L + N \\ \frac{1}{2}(N - N_L + 1)(N - N_L + 2), \\ \qquad \text{when } 0 \le N_L \le N,\ N_H = N \end{cases} \tag{3.33}$$

It was verified by simulation that Ω provides an accurate approximation for the value of γ_{IM3} (3.29). The approximation errors are less than 0.7%. Similarly, for the case of WBI and WBI (3.26), we can also obtain the total number of in-band

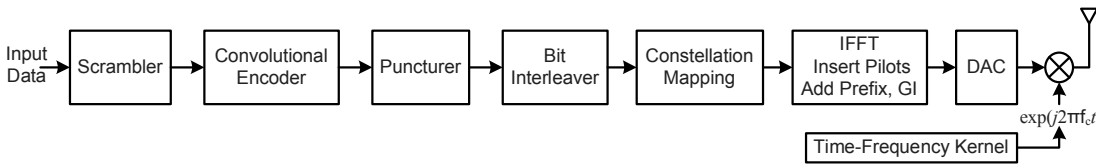


Figure 3.8. Transmitter architecture of MB-OFDM UWB system.

$sinc^2((f - f_l)T)$ functions by summing all the Λ_l (A.51) with $l \in [N_L,\ N_H]$. With these adjustments, the two-tone approach can indeed provide an accurate estimation of the IM3 products, which will facilitate the trade-off analysis when designing UWB systems.

3.2.2 Modeling in Matlab: UWB System Validation

In this section, the interference effects on an MB-OFDM UWB system are examined using Matlab simulations. The results are used to validate the statistical approach, and also to compare with the standard two-tone approach. A model of the transmission chain [11] (as shown in Fig. 3.8) is built to generate the MB-OFDM UWB signal. Spectrum of the transmitted signal is shown in Fig. (3.9).

Here, discrete samples of the complex envelope of the OFDM signal can be obtained by computing the Inverse Discrete Fourier Transform (IDFT) of the complex symbol sequence $\{c_0, ..., c_{N-1}\}$. In our simulation, 128-point IDFT was performed to generate the UWB signal. With sampling period t_s, the n-th sample $x[n]$ of the OFDM signal as shown in (3.5) and the n-th element C_n of the IDFT sequence $\{C_0, ..., C_{N-1}\}$ could be related as:

$$\begin{aligned} C_n &= \sum_{m=-\frac{N}{2}}^{\frac{N}{2}} c_m e^{j\frac{2\pi mn}{N}} \\ x[n] &= g(nt_s) \sum_{m=-\frac{N}{2}}^{\frac{N}{2}} c_m e^{j\frac{2\pi mn}{N}} = g(nt_s) C_n \end{aligned} \tag{3.34}$$

To simulate the inter-modulation distortion effects, an UWB signal (as WBI) and

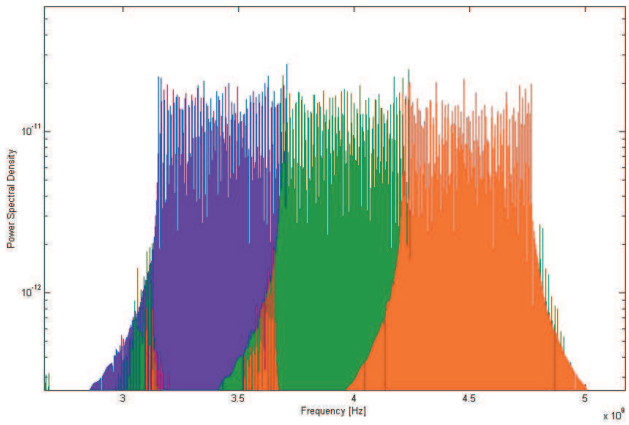


Figure 3.9. Spectrum of an MB-OFDM UWB signal (band group I).

a single-tone signal (as NBI) are passed through a nonlinear behavioral model. Subsequently, the output PSD is obtained by simulation and compared to our proposed estimation. Fig. 3.10 shows simulated PSD of an inter-modulation product.

Since simulating in the carrier frequency (GHz) is computationally intensive, the equivalent baseband UWB signals and interference are used. We also simulated the two-tone approach. In that approach, an input stimulus consisting of two pure tones at f_1 and f_2 is fed into the system, and the outputs at specific frequencies are measured. The IMD outputs at $2f_1 \pm f_2$ or $f_1 \pm 2f_2$ are measured to characterize the third order nonlinearity (P_{IM3_out}).

Fig. 3.11 and Fig. 3.12 show the in-band IM3 power at the output of the nonlinear receiver model under three different interference considerations, with different interference power (-35dBm in Fig. 3.11, -30dBm in Fig. 3.12). The two-tone results are based on the equation (3.2), which only consider the interference power and $IIP3$. Therefore, the traditional two-tone approach generates same IM3 power for different types of interferences. However, both the actual PSD simulation and our statistical approach show that the interference locations have effects on the IMD products.

The system simulation results show good agreement to our analytical calcula-

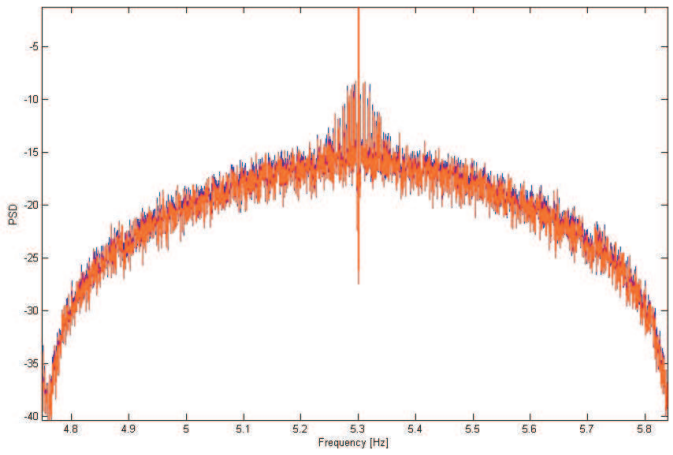


Figure 3.10. Simulated PSD of an inter-modulation product.

tions, while deviation exists if compared to the traditional two-tone approach. This validates our statistical approach of computing the PSD of IMD products. Also, these results demonstrate that the distance (in dB) between the two-tone approach and the accurate results (i.e. δP_{IM3} in dB) does not vary when the power level of interferences changes (from -35dBm (Fig. 3.11) to -30dBm (Fig. 3.12)).

3.2.3 Modeling in Metropolis

Metropolis is a heterogeneous system design environment that is deeply rooted in the platform-based design methodology [10]. It defines a meta-modeling language called Metropolis Meta-Model(MMM), which can be used to capture functional models, architectural models, and formal constraints on the models. Metropolis also provides an MMM compiler, a simulation tool and other verification and synthesis tools.

I. Metropolis Design Environment

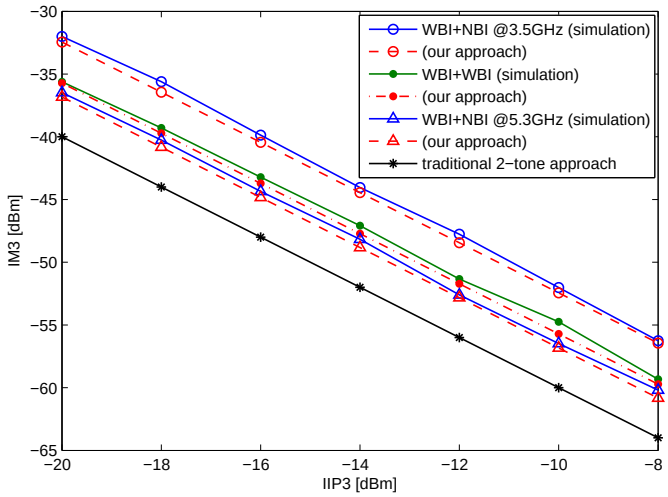


Figure 3.11. In-band IM3 power from system simulation, our analytical approach, and the traditional two-tone approach. Three interference cases: NBI(5.3GHz) and WBI (band 3); NBI(3.5GHz) and WBI(band 3); WBI (band 2) and WBI (band 3). Desired UWB signal is in band 1. Interference power is -35dBm.

Figure 3.13 shows the Metropolis infrastructure. The three pillars of Metropolis consist of

1. The design methodology

   Design methodology is the foundation of a design environment. It determines not only how to represent the models, but also how to maneuver the models. Metropolis design environment is based on the *platform based design* methodology, which emphasizes the separation between functional models and architectural models. On top of the models, formal constraints can be added to them to restrain their behaviors or to denote the desired performance or cost. One notable example of such constraints is the mapping constraint. They specify which elements in the functional model are implemented by which elements in the architectural model. Along with the mapping constraints, data can also be passed from one side to the other in order to get accurate behavior and performance. Once the optimal mapping is found, the functional model, the

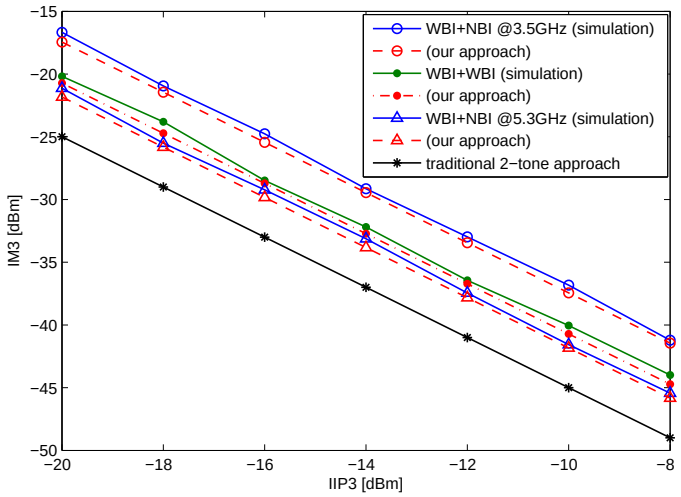


Figure 3.12. In-band IM3 power. The interference cases are same as in Fig. 3.11. Interference power is -30dBm.

architectural model and the mapping constraints will be passed to the downstream tools to generate an implementation. For a more detailed discussion of the *platform based design* methodology, please refer to section 2.3.1.

2. The meta-model of computation

   Metropolis targets the design of heterogeneous systems. Very often, the heterogeneous components in the system are best designed with different models of computation. For instance, multimedia systems are best captured by dataflow models; control systems by finite state machines; digital circuits by discrete events; analog circuits by continuous time systems; etc. Metropolis defines a meta-modeling language that aims to capture various models of computation. If we consider a model as an abstraction of a part of the reality, then meta-model, as its name suggests, is a model of a model, or a further abstraction of models. Metropolis meta-model (MMM) is such a language that can describe other models of computation.

   In MMM, a functional model is described by a set of processes and media. Each

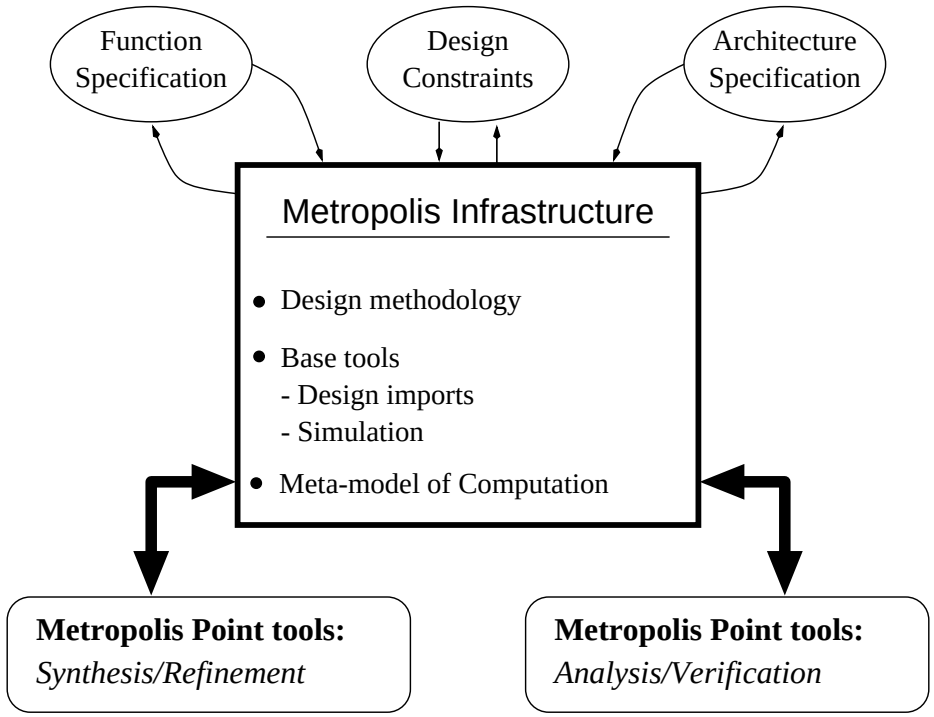


Figure 3.13. Metropolis Infrastructure

process take sequential actions, while multiple processes run concurrently and communicate to with each other via common media through ports. A communication contract, called interface, defines a set of methods that can be called through a port and must be implemented by media. The above mechanism allows MMM to separate computation captured by processes from communication captured by media, which is essential to facilitate the reuse of the models in future designs.

Formal constraints restrict the set of legal executions. They can be specified in linear temporal logic and logic of constraints. The former usually coordinates the execution of processes or relate the behavior of networks through mapping or refinement. The latter, on the other hand, focuses on quantitative characters of a system, such as performance and cost.

MMM models architectural models and functional models in a similar way.

Processes and media capture computation and communication. However, architectural models emphasize more on the services provided to the functional model and the performance and cost of the services. In MMM, the former is modeled as a set of methods offered by an architecture model, bundled into interfaces. To represent the performance and cost for each service, MMM introduces the notion of quantity, which can be used to annotate values measuring performance and cost to methods. For example, to specify that a service takes a certain amount of energy, the amount will be annotated to the method. Such annotation requests are made to an object called quantity manager, which collects all requests and fulfills them, if possible. Quantity is such a generic concept that various quantitative modeling aspects can be represented. This not only includes the classic performance numbers such as time and power, but also extended concepts such as resource arbitration, scheduling policies, etc.

Finally, evaluating a particular implementation's performance requires mapping a functional model to an architectural model. MMM can do this without modifying the functional and architectural models. It does so by defining a new model to encapsulate the functional and architectural models, and relates the two by synchronizing events between them. This new model can be considered as a top layer that specifies the mapping between the function and architecture.

3. Metropolis tools

   Metropolis provides various tools to support model import, analysis and implementation. Figure 3.14 shows the Metropolis tools framework. It consists of three major parts: the meta-model compiler, a set of back end tools, and the interactive shell.

   MMM is used for the purposes of capturing and communicating of design intent and results. It focuses on the interaction among designers working at different

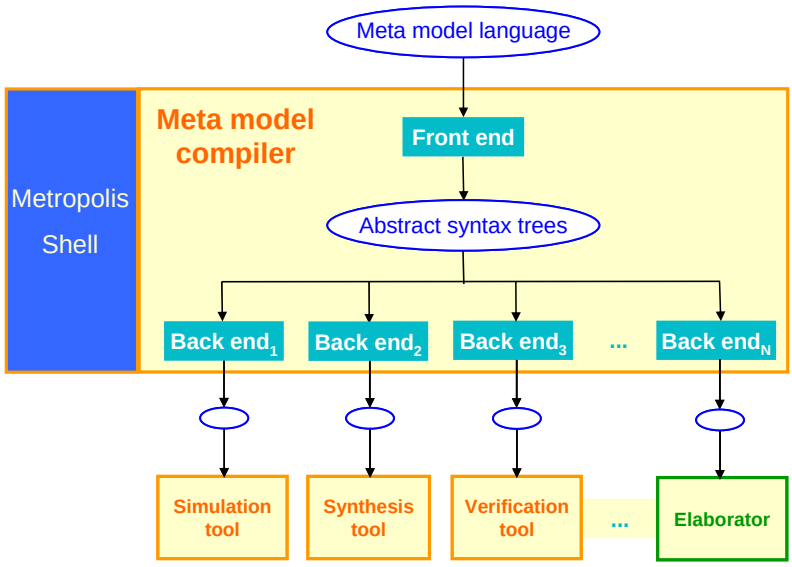


Figure 3.14. Metropolis Tools Framework

abstraction levels and among people working concurrently at the same abstraction level. The meta-model compiler is the foremost tool that takes the design and parses it into an abstract syntax tree (AST). Various back end point tools can be invoked on the AST, and produce another form of output for different purposes. The backend tools include an elaborator, a formal verification tool, a synthesis tool and a simulation tool.

II. Baseband Modeling and Algorithm Validation

Figure 3.2 shows the synchronization algorithm. We explore the different possibilities of partitioning the design between analog and digital. In this section, we model the algorithm at a high level of abstraction in Metropolis. From a mathematical point of view, a mixed-signal system like this radio baseband can be classified as a hybrid system. A typical question for modeling a hybrid system is how to deal with the different time domain, i.e. continuous time (CT) and discrete time (DT). The related

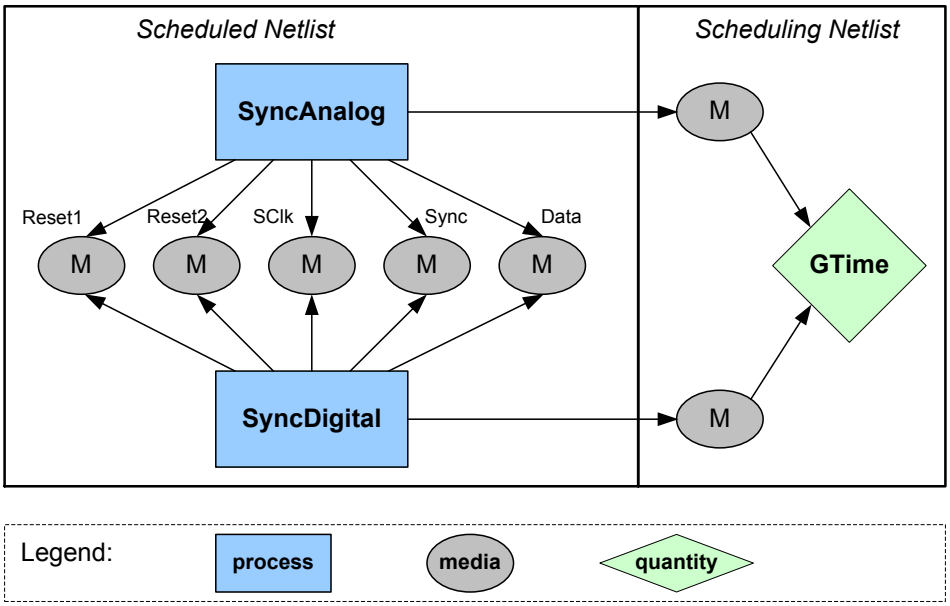


Figure 3.15. Symbol Synchronizer Model in Metropolis

issues include how to specify a proper time notion, how to deal with the interaction interface between the CT domain and the DT domain.

These issues can be nicely handled by the Metropolis design environment. In order to compare the effectiveness of the modeling mechanisms, I created two different models for the symbol synchronizer. Figure 3.15 shows the one that utilizes the advanced quantity annotation mechanism to achieve the synchronization of the CT and DT domains. Another model relies only on the basic modeling constructs provided by Metropolis, where time is handled explicitly as part of the behavior of the model. The second model has the same structure as the scheduled netlist in the first model. I will elaborate the two models in the following to demonstrate the solution to integrate CT and DT domains.

Usually, a CT problem can be specified by the Differential-Algebraic Equations (DAE). In this baseband model, the CT part is specified by the ODEs, and the digital controller is modeled by a finite state machine (FSM). In general, CT and DT systems

may both advance time to a point where a behaviorial event occurs. For instance, clock events in the digital system periodically advance time forward by a fixed amount of time (cycle); a signal in the analog system crossing a voltage level triggers an event and also brings time to the crossing time point. Therefore, to give a complete solution to the CT/DT model integration, a bi-directional time synchronization mechanism must be devised. However, in the symbol synchronizer model discussed below, I simplified the timing model such that the digital controller is the sole driving instance that may advance time, and the analog portion simply catches up with the time changes and updates the signals in the analog system to the current time. Please note that even though I made the simplification, the quantity annotation mechanism is a full-fledged solution that is capable of handling bi-directional time synchronization.

Basic Model with Timing as Explicit Parameters In the basic model, time is treated as a regular parameter in the behavior. The model has the same structure as the scheduled netlist in figure 3.15, i.e. the analog and digital portion are modeled separately by two Metropolis processes. They communicate via common media, each of which conveys one signal with a special protocol. For the two reset signals, they are written by the digital controller and picked up by the analog integrators. The communication protocol of this write operation looks like the one described below.

```
interface DT2M extends Port {
    update void writeInput (int value, double DTtime);
}

interface M2CT extends Port {
    update boolean haveWriteReq ( );
    update double getWriteTime ( );
    update double receiveInput ( );
}
```

This protocol defines one discrete-time-process-to-medium interface (DT2M)

and one medium-to-continuous-time-process (M2CT) interface. Whenever the DT process decides to write a reset signal to the analog part, it calls the *writeInput* method implemented by the medium with both the signal value and the current time as parameters. In order to guarantee that the analog process synchronizes with the digital controller, the *writeInput* method blocks inside and does not finish before the written value is consumed by the analog process. On the other hand, the analog process actively checks for incoming write request by calling the *haveWriteReq* method. If a new write request comes, the analog process will *getWriteTime* and then *receiveInput*. Only after this step, the original *writeInput* method terminates. This way, the digital and analog processes synchronize with each other to the same time.

The other three signals, SClk, Sync and Data, are updated by the analog process and read by the digital process. However, instead of following the dataflow direction, I let the digital process to pull the data whenever there is a need. Similarly, I define the following communication protocol. When the digital process needs the value of any of above signals, it will call the *readOutput* method with the time of interest. The read request will be detected by the analog process by actively running *haveReadReq*. Then the analog process will *getReadTime* and *issueOutput*. Only at this point, the *readOutput* method will return with the updated signal value from the analog process. So, again the digital process is driving the time, while the analog process follows and updates the signal values.

```
interface CT2M extends Port {
    update boolean haveReadReq ( );
    update double getReadTime ( );
    update void issueOutput (double value);
}

interface M2DT extends Port {
    update double readOutput (double DTtime);
```

```
}
```

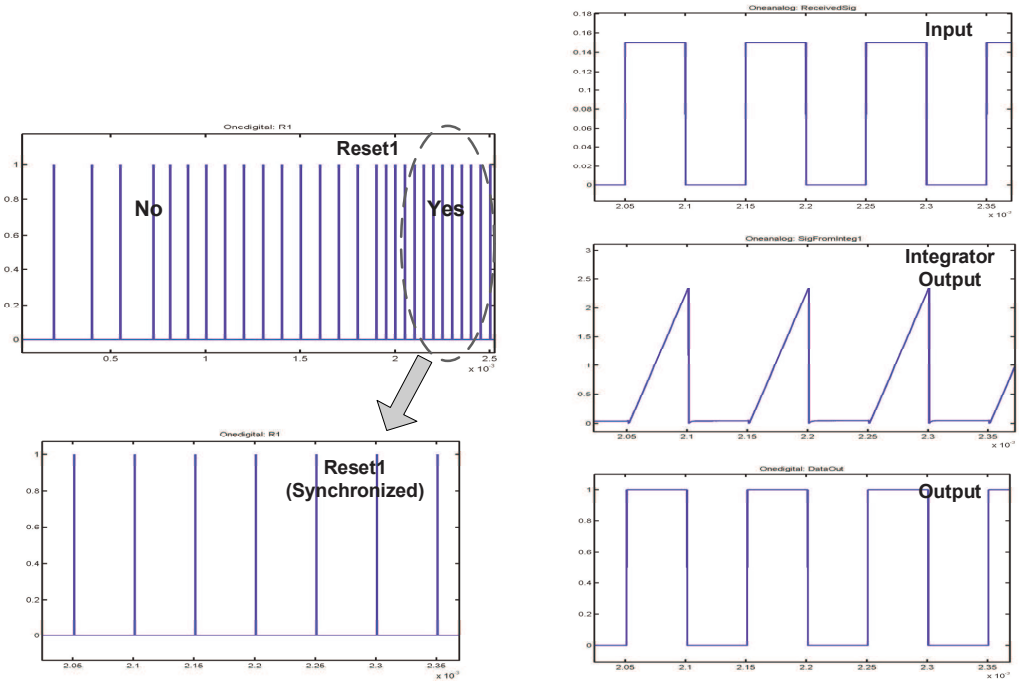
This time synchronization mechanism works very well with the symbol synchronizer model. Figure 3.16(a) shows the simulation result of a reset signal generated by the digital controller. It can be seen that the reset signal gradually converged to the steady state, i.e. synchronized with the input symbols. Figure 3.16(b) shows the input and output signals have been synchronized.

Advanced Model using Time Quantity Management One innovative design philosophy in Metropolis is that the system performance, cost and any other quantitative characters can be captured by the same design construct called *Quantity Manager*. In the symbol synchronizer design, I took advantage of this concept and converted time from an explicit parameter tightly coupled in the behavior (e.g. the arguments passed to *writeInput* and *readOutput* methods) to a global time quantity (see figure 3.15).

In this more elegant model, whenever the digital process advances time, it makes an quantity annotation request to the GTime quantity manager with the proposed next time point. The GTime quantity manager collects all such requests and decides which one to grant. The request granting criterium for global time is simple, i.e. the next most immediate time point will be granted, and all other requests for future time points will be declined. This guarantees the non-decreasing nature of time.

In the symbol synchronizer design, the digital process makes quantity annotation requests to GTime and moves time forward. When it reads or writes to the media, the analog process consults the GTime for the current time and reacts accordingly. This model generates the same simulation result as the previous one. The introduction of GTime quantity manager gives an advanced way to

synchronize DT and CT domain. At the same time, the clear separation of time (performance) and the model behavior demonstrates the design methodology of Metropolis, which potentially increases the reusability of both the behaviorial model and the performance model.



(a) (b)

Figure 3.16. Symbol Synchronizer Model Simulation Result

3.3 System-Level Conclusions

- **UWB Receiver Front-end**

When targeting a low-power design, a receiver with tight design margin may not satisfy the PER requirements in the presence of interference if the prediction of distortion effects is not accurate. In the previous sections, we presented an analytical approach to determine the impact of the interference distortion products in MB-OFDM UWB

systems caused by receiver's memoryless nonlinearities. By exploring the statistical properties of OFDM signals, accurate analytical expressions of various IMD and XMD products introduced by the third-order nonlinearities are derived. The accuracy of the technique has been verified by comparing the analytical computations with system simulation results. Based on this approach, analytical computation allows designers to predict the distortion behavior and SNR degradation without running simulation of the entire actual system.

In a UWB receiver, a pre-select Band-Pass Filter (BPF) is usually inserted between the antenna and the low-noise amplifier (LNA) to limit the strong out-band interference that otherwise might desensitize the receiver. The i-th interference power at the receiver's input is $P^{-}_{intf_i} = P_{intf_i} - A_{flt_i}$. For an optimal receiver design, we should consider not only the attenuation capabilities (A_{flt}), but also the insertion loss (IL_{BPF}) of this BPF. The 1dB compression requirement (P_{1dB}) is determined by the maximum interference to avoid the desensitization ($P_{1dB} \geq \max_i\{P_{intf_i} - A_{flt_i}\}$). This also implicitly sets a constraint for the front-end $IIP3$. Here, we use the two-tone approach to estimate the various IM3 products $P_{IM3(ij)}$, with proper adjustments $\delta P_{IM3(ij)}$ (in dB).

The noise contribution from the reciprocal mixing effects is neglected because the out-band interference is at a large frequency offset. The various third order IMD products, $P_{IM3(ij)}$, are the dominant contributors to P_{IM_total}. To analyze the system budget and derive the linearity specifications, the following equations are used to estimate the effects of the front-end IIP3, sensitivity, noise figure (NF_{frnd}), filter attenuations (A_{flt_i}), filter insertion loss (IL_{BPF}), and the receiver implementation loss IL_{RX} (sensitivity = -80.5dBm at bit rate $R_b = 110Mb/s$ [12]):

$$
\begin{aligned}
&((-174 + 10log_{10}(R_b) + IL_{BPF} + NF_{frnd}) + P_{IM\_total})[dBm] \\
&\quad \leq -80.5dBm + 6dB - IL_{RX} - E_b/N_o \\
&IIP3 \geq \max_i\{P_{intf_i} - A_{flt_i}\} + 12dB \\
&P_{IM3(ij)} = 2P^-_{intf_i} + P^-_{intf_j} - 2IIP3 + \delta P_{IM3(ij)}
\end{aligned}
\tag{3.35}
$$

In the presence of interference, we operate the receiver at 6dB above sensitivity. $E_b/N_o \geq 4dB$ is chosen to satisfy $PER < 8\%$ for a 1024 byte packet.

Among the various narrow-band interferences, we should try to get rid of the large in-band NBIs (e.g. WiMax) to avoid the possible significant degradation of system performance. An efficient technique is interference detection and mitigation [33]. In our work, we assume that the large in-band NBIs are dealt with by dedicated techniques, and not taken into account when we perform the receiver budget analysis. The major interference sources under our consideration are WBIs and out-band NBIs. For instance, to estimate the dominant P_{IM3}, we use a WBI with power $P_{intf_1} = -35dBm$ and an out-band NBI with power $P_{intf_2} = -17dBm$.

In the later top-down optimization process, the front-end performance involved in (3.35) will be estimated by behavioral models, and the design requirements formulated by these relations will be automatically balanced. Therefore, we do not need to manually solve the equations and distribute the specifications to each building block.

- **Baseband for WSNs**

The primary goal of the WSN receiver is to detect and demodulate the received OOK signal (with a BER below 10^{-4}). For the power dissipation, it has been estimated that wireless sensor nodes consuming less than 1mW can achieve reasonable operations by scavenging energy (e.g. light) from surrounding environments [41]. The goals of the baseband synchronization system are to maintain the inherent sensitivity of the

receiver, demodulate the OOK data, minimize the synchronization time, and operate at extremely low power consumption and bias current levels.

As discussed in a previous section, compared to a normal receiver baseband, the complexity of this WSN baseband synchronization has been reduced to facilitate a low power consumption. For the OOK modulation, only timing and amplitude are required to be detected during synchronization. Moreover, to reduce the power consumption as much as possible, instead of tracking them for the entire packet, they will be estimated only once since timing and amplitude are static over the length of the packet. Besides that, a careful trade-off of data rate, packet length, clock accuracy has been performed to accommodate for a low power implementation of synchronization scheme [8]. The total header length of the chosen synchronization scheme is 31, including 10 for threshold estimation, 14 for timing estimation, and 7 for packet synchronization.

Besides synchronization, another desirable feature of this baseband system is to perform carrier sense, that is a requirement from the MAC layer protocol. The transmitted data streams have at least 5 ones in any continuous 10 symbols. This allows us to achieve carrier sense by integrating the channel energy and comparing to a given threshold. This feature will be addressed in our implementation.

Chapter 4

Platform Exploration

4.1 Architecture Level Exploration

4.1.1 Analog/RF Behavioral Model

An effective way to perform the architectural exploration is to create realistic models of circuit components that can capture the analog/RF 2nd order effects using the suitable mathematical techniques. The objective of analog/RF behavioral modeling is to represent circuit functionalities with abstract mathematical models while hiding the circuit details. Given a specific circuit, we can build behavioral models with different levels of details to fit various application requirements. For example, the simplest mode is to describe the ideal functionality. If the application needs to capture some second order effects, static weak nonlinearity can be included into the model. A more complex model can address the dynamic weak nonlinearity. Even further, the model can become very complex if it includes strong nonlinearity and noise effects. Therefore, modeling approach should be carefully selected to make a balance between model accuracy and complexity, also between computational speed and effi-

ciency. Moreover, different application scenarios request different type of behavioral models.

Behavioral Model for System Verification

A typical usage of building behavioral models is to facilitate the system verification. Simulation of the entire system is usually required to verify the critical functionalities or performances. In the past decades, the device models and transistor-level simulation have evolved to increased accuracy, but the simulation speed has not gained enough improvement. This makes it impractical to perform transistor-level simulation for a large system. For a mixed-signal system consisting of RF, analog, and digital blocks, verifying the entire system via transistor-level simulation is an extremely difficult process and can become intractable due to the limitation of simulation capacity. An effective solution is to seek helps from higher-level abstractions.

Behavioral models are developed to accelerate simulation-based system verification significantly, offering isolation from the details of the lower-level implementation. This type of high-level abstractions mainly capture the functionalities of the analog/RF blocks, while also including some non-ideal effects. The high-level descriptions should perform well in the co-simulation with the digital part. This type of behavioral model is often named as macromodel, approximately describing equivalent input-output behavior with much lower computation cost while hiding the internal architectural details as much as possible. For verification purpose, the models must be accurate enough, and sufficiently compact to achieve substantial simulation speedups.

A macromodel is typically constructed for a specific topology and a fixed set of circuit parameters. Automatic model generation techniques have been developed to generate the analog/RF macromodels, where the models are extracted from the circuits so that a high degree of model consistency is maintained. A parameterized

macromodel is more desirable for the reuse purpose in that the model can be calibrated to fit the changes in the circuit without having to rewrite the model from scratch. The process of automatic model generation consists of two phases. One is to build or select a proper model template, and the second phase is to extract the model parameters from lower-level models/circuits and instantiate the template.

Up to date, there is no modeling technique capable of generating a generic macromodel suitable for all analog/RF circuits, instead, specific modeling approaches and templates should be adopted for different class of circuits. Many model order reduction (MOR) techniques have been developed for linear time-invariant (LTI) systems [39, 21, 34] and linear time-varying (LTV) systems [45, 38], such as Asymptotic Waveform Evaluation (AWE) approach [39], Krylov-subspace model [37], Truncated Balanced Realizations (TBR), Trajectory Piecewise Linear (TPWL) model [42], Piecewise Polynomial (PWP) model [19], etc. Volterra series models [50, 56, 55] and modified Volterra models [32] are also widely used to characterize weakly nonlinear analog/RF circuits. To obtain the model parameters, there are two types of extraction approaches. Simulation-based approach is basically a black-box approach, without resorting to the circuit schematic details. In contrast, the analytical approach needs to understand the circuit topology and then derive the mathematical descriptions. The quality of a behavioral model is highly conditioned by the parameter extraction process.

Behavioral Model for PBD

In the PBD methodology for wireless system design, the need for behavioral models is in a different scenario, i.e. design exploration and system optimization. High-level decisions and tradeoffs can be made efficiently by evaluating system specifications through the use of a set of behavioral models that correspond to a variety of circuit

topologies and configurations. A library of well-built behavioral models represented in some standard language will enable convenient design reuse.

At the system level of PBD, the design requirements are specified in the performance metrics. In the context of PBD, these system-level specifications and constraints need to propagate to the implementation layer (e.g. transistor level). System level design decisions for receivers involve gain, noise and non-linearity partitioning along the receiver chain so that optimum performances can be achieved at minimum cost (e.g. minimum power consumption). Optimal partitioning is indeed hard if transistor-level simulation is the only available support. From another perspective, during the bottom-up process, the implementation costs and performance limitations should be delivered to the system level so that the feasibility of an optimal system solution is ensured. The strategy to fulfill these two-fold demands is to bring in the behavioral models at an intermediate level of abstraction. The role of these behavioral models makes them different from the macromodels for verification usage in that they should be able to derive the higher-level performance from the lower-level performance of a set of building blocks. During the design exploration process, there can be a stack of hierarchical models at different levels of abstraction. It is a model refinement process for the system design constraints to propagate step by step until a valid design is reached.

Generally, a behavioral model for the PBD usage can be any mathematical description with the support of sufficient lower-level architecture information. A parameterized executable model is preferred. The model parameters should be defined by the lower-level platform characterization (e.g. circuit simulation). The primary requirement for the behavioral model is that it should provide a mapping assistant between the system-level constraints and lower-level design specifications. Considering this specific requirement, it is more preferable to have the set of model parameters closely configured by the lower-level performance space because the constraint prop-

agation is easy to accomplish. The performance set should capture non-idealities and second order effects, such as gain, bandwidth, noise, etc. In this context, the performance space is an abstract model of the lower-level architecture platform, constraining the achievable ranges of the behavioral model parameters. In this way, the behavioral models introduce at the functional level a number of non-idealities due to the actual circuit implementation.

The behavioral model can be built as a structural model, composed of the behavioral models of different building blocks. For each individual building block, the model configuration parameters come from a set of lower-level performances of the corresponding block. These models should describe the important non-ideal effects in order to evaluate the system performance in a realistic way. Composing these models together, an architectural model is constructed, and proper evaluation of this model will provide the performance estimation at a higher level of abstraction. Using the model in the reverse way, different partitions of system specifications can be attempted, resulting the system design requirements propagate to lower levels.

Based on these behavioral models, architecture exploration can be accomplished by investigating the various compositions of the building blocks, that makes an architectural platform. Each structural model describes one possible implementation of the system level model. During the design space exploration, only performance space of a lower level is available while the implementation details and the configuration space are hidden behind the platform abstraction. The simulation with behavioral models at system-level can help in selecting the correct architecture to implement the analog/RF functions with constraints on the amount of acceptable non-idealities.

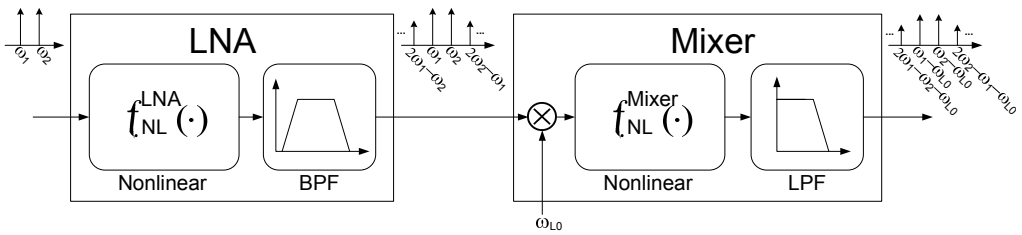


Figure 4.1. A behavioral model of the UWB receiver front-end.

RF Front-End Modeling

To capture the weakly nonlinear behaviors of the receiver front-end, a model with polynomial nonlinearity and filtering stages is built, as shown in Fig. 4.1. The front-end architectural space will consist of different LNA and mixer topologies, that will be discussed in the section 4.2. The coefficients of the behavioral models are configured by the circuit performances which are obtained from the platform characterization.

The main purpose of building these behavioral models is to provide an abstract yet accurate representation of the corresponding building blocks so that the front-end performance could be quickly estimated, without running the intensive simulations at transistor level. Specifically, in the PBD flow, the high-level optimization is performed efficiently by employing the behavioral models, which therefore link the system specifications to circuit implementations.

As shown in Fig. 4.1, the front-end behavioral model is the composition of LNA and mixer models. A third order polynomial is used to model the nonlinear behaviors, represented as $f_{NL}^{LNA}(\cdot)$ and $f_{NL}^{Mixer}(\cdot)$ in Fig. 4.1:

$$V_{out}(t) = a_1 \cdot V_{in}(t) + a_2 \cdot V_{in}^2(t) + a_3 \cdot V_{in}^3(t)$$

$$\begin{cases} a_1 = Gain \\ a_2 = \frac{a_1}{V_{IIP2}} \\ \mid a_3 \mid = \frac{4}{3} \cdot \frac{|a_1|}{V_{IIP3}^2} \end{cases} \tag{4.1}$$

The coefficients a_1, a_2, a_3 are related to the circuit performance, $Gain$, V_{IIP2} (IIP2 in Volt), V_{IIP3} (IIP3 in Volt), which are all extracted from SpectreRF simulation of the LNA and the mixer circuits.

The overall performance of the RF front-end will be estimated using its behavioral model. There are several different approaches to implement the performance estimation. And the estimation can be conducted in time domain or frequency domain. As the front-end behavioral model is a cascaded structure of the LNA block and the mixer block, an equation-based approach is to derive the analytical expressions of the overall performance in terms of the building block performance. This provides a quick evaluation of the front-end performance. For instance:

$$NF_{total} \simeq NF_{LNA} + \frac{(NF_{Mixer} - 1)}{Gain_{LNA}} \tag{4.2}$$

$$\frac{1}{V^2_{IIP3\_total}} \simeq \frac{1}{V^2_{IIP3\_LNA}} + \frac{Gain^2_{LNA}}{V^2_{IIP3\_Mixer}} \tag{4.3}$$

To obtain a more accurate estimation of the front-end performance, we developed a simulation-based approach. This approach has been implemented and executed in Matlab. Since simulating RF behaviors in the time domain is computationally intensive, we decided to conduct the behavior simulation in the frequency domain. The frequency-domain representation and modeling technique provide a very effective way to deal with the wide-band input/output signals.

When designing or measuring a RF block, signals of pure tones are usually used as the stimuli. Take the nonlinear model of LNA as an example. We suppose an input of two pure tones $V_{in}(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$ is plugged into a LNA which is modeled by equation (4.1.1):

$$\begin{aligned} V_{out}(t) = {} & a_1 \cdot (A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)) + a_2 \cdot (A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t))^2 \\ & + a_3 \cdot (A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t))^3 \end{aligned} \tag{4.4}$$

Frequency	Product
0	$\frac{1}{2}a_2\sum_{i=1}^{N}(A_i\angle\phi_i)^2$
f_i	$(A_i\angle\phi_i)[a_1+\frac{3}{4}a_3(A_i\angle\phi_i)^2+\frac{3}{2}a_3\sum_{j=1,j\neq i}^{N}(A_j\angle\phi_j)^2]$
$2f_i$	$\frac{1}{2}a_2(A_i\angle\phi_i)^2$
$f_i \pm f_j$	$a_2(A_i\angle\phi_i)(A_j\angle(\pm\phi_j))$
$3f_i$	$\frac{1}{4}a_3(A_i\angle\phi_i)^3$
$2f_i \pm f_j$	$\frac{3}{4}a_3(A_i\angle\phi_i)^2(A_j\angle(\pm\phi_j))$
$f_i \pm 2f_j$	$\frac{3}{4}a_3(A_i\angle\phi_i)(A_j\angle(\pm\phi_j))^2$
$f_i \pm f_j \pm f_k$	$\frac{3}{2}a_3(A_i\angle\phi_i)(A_j\angle(\pm\phi_j))(A_k\angle(\pm\phi_k))$

Table 4.1. Output harmonic and inter-modulation products.

Given the input spectrum $V_{in}(\omega_1)$ and $V_{in}(\omega_2)$, the output responses at the various frequencies of interest can be derived from equation 4.4. For instance, LNA outputs at frequencies ω_1 and $(2\omega_1-\omega_2)$ are:

$$\begin{aligned} V_{out}^{LNA}(\omega_1) &= V_{in}(\omega_1)(a_1+\tfrac{3}{4}a_3V_{in}(\omega_1)^2+\tfrac{3}{2}a_3V_{in}(\omega_2)^2) \\ V_{out}^{LNA}(2\omega_1-\omega_2) &= \tfrac{3}{4}a_3V_{in}^2(\omega_1)V_{in}(\omega_2) \end{aligned} \tag{4.5}$$

Following the same principle, we generalized the above tone-based computation to multiple input tones, $V_{in}(t)=\sum_{i=1}^{N}A_i\cos(\omega_i t+\phi_i)$ $(N\geq 2)$. We derived the output products at various frequencies, as shown in table 4.1. In the table, we use $A_j\angle(\pm\phi_j)$ to represent the signal $A_j\cos(\omega_j t\pm\phi_j)$.

This simulation-based approach has been implemented in Matlab. The coefficient of each output tone is directly provided. Running this approach, we can obtain the frequency-domain output signals of the cascaded front-end model (Fig. 4.1). Knowing the input and output spectrum, the overall nonlinear performances of the RF front-end can be immediately estimated by probing the output spectrum at proper frequencies (after down-conversion). For instance, the two inputs to LNA are $f_1=4.8GHz$, $f_2=5.2GHz$, the mixer LO frequency is $f_{LO}=4.49GHz$, the front-end $IM3$ product can be obtained by measuring the overall behavioral model output at $90MHz$.

To validate the RF front-end model accuracy, we built a number of platform instances for the individual building blocks and the overall front-end. Circuit-level sim-

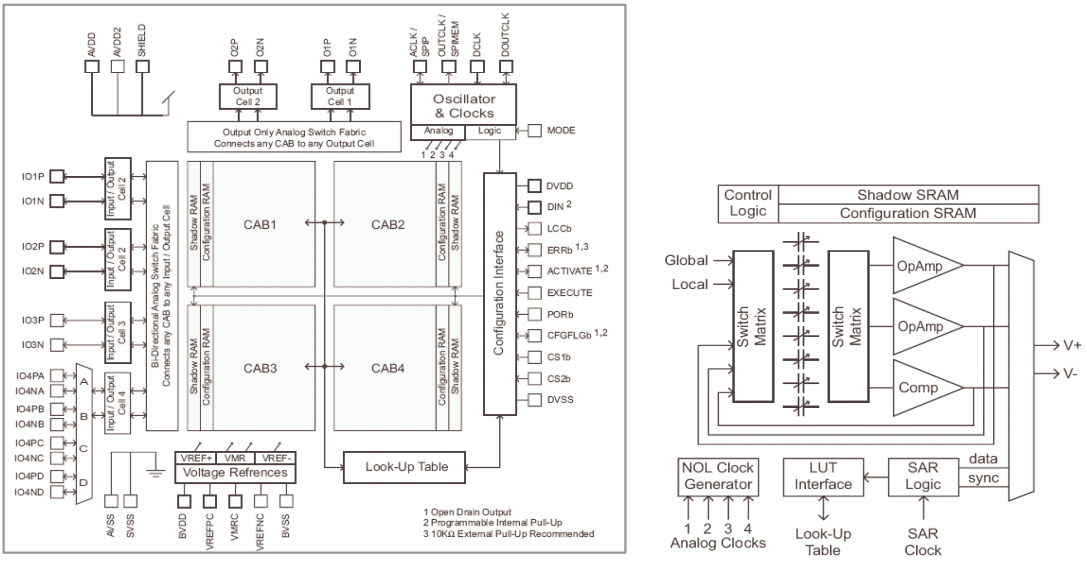
ulations on these platform instances have been conducted in SpectreRF. The obtained performances were compared to the behavioral model simulations in Matlab. Particularly, we are interested in the outputs at the fundamental frequency and the third order inter-modulation products ($IM3$). The simulations showed that the behavioral models of the individual blocks (LNA, Mixer) can achieve a high accuracy (errors are within $\pm 5\%$). For the entire RF front-end, among a total number of 60 front-end platform instances, around 86% simulation results of the behavioral model can achieve $\pm 15\%$ accuracy. Thereupon, we validated that the performance estimation through behavioral models is accurate enough for the top-down system optimization purpose.

4.1.2 Reconfigurable Platform

Another effective assist to perform architectural exploration is reconfigurable platforms. Through exploiting a reconfigurable mixed-signal platform, the different trade-offs of functionality partition and signal partition can be effectively investigated. As is well known, Field Programmable Gate Array (FPGA) has been adopted in many systems to provide flexibility. The analog equivalent of FPGA, Field Programmable Analog Array (FPAA), has been developed by some companies, e.g. Anadigm [2]. The design of complex analog systems is simplified since the design process is moved from the component level to the functional level. With the ability to implement analog functions in reconfigurable architectures, time to market can be drastically reduced and the design flexibility is improved compared to an analog ASIC or a discrete implementation. Another important feature is, without interrupting the operation of the system, FPAAs can be under real-time control of the system. This run-time reconfigurability provides more flexibility, and may give various performances for one

design. This reconfigurable analog platform allows effective co-design of analog and digital components, perfectly complementing digital platforms.

The basic architecture of an Anadigm FPAA consists of pre-built Configurable Analog Modules (CAMs), which provide common analog elements, such as filter stages, amplifier stages, summing/difference stages, voltage multiplication, rectifiers, oscillators, references, etc. With FPAAs, designers can describe analog functions like gain stages and filters without considering the lower level of components such as Op-Amps, capacitors, resistors, current mirrors, etc. Physically, the Anadigm FPAA is based on a CMOS-based fully differential switched-capacitor technology with an analog switch fabric. Here, RC-equivalent networks are provided via switching capacitance. Its unique feature, analog programmability, is also provided by this switched capacitor technique. The design tool AnadigmDesigner2 is available to use the FPAA.



(a) FPAA(AN221E04) Chip Overview [2]

(b) Overview of a Configurable Analog Block [2]

Figure 4.2. FPAA overview

For the Picoradio baseband design, after validating the algorithm (as discussed in section 3.2.3), the system is mapped on the FPAA-FPGA platform to perform the

architectural exploration. To investigate the tradeoffs, the analog/digital boundary is moved to attempt two solutions: mostly-analog and mostly-digital. Performance annotation was performed on the FPAA to introduce basic non-idealities so as to build an analog platform.

An important observation we obtained from the performance extraction of the FPAA is that, the algorithm reported in Fig. 3.2 cannot be directly mapped as a mostly-analog solution on the FPAA because the FPAA is a switched capacitor fabric operated in the discrete time domain. In particular, restrictions on sample and hold instants imposed by FPAA clocks required adapting the synchronizer scheme. Fig. 4.3 shows the platform-based mapping process of the synchronization scheme to an FPAA-FPGA platform instance. The original scheme (Fig. 3.2) is adjusted to meet the architecture constraint of the reconfigurable platforms.

In the final implementation the input signal is low-pass filtered before informing two integrator paths, whose reset triggers are controlled by the FPGA. One path is delayed by one symbol period to implement an equivalent scheme to the δ delay in Fig. 3.2. Finally, a comparator determines the difference between paths. The digital control algorithm performs a binary search on the delay between the two paths by controlling the reset signal of the integrators. In this analog synchronization scheme, the digital part also performs another function, packet synchronization. That is realized by correlating the received data with a 7-bit sequence. The refined system was then simulated and mapped on the platform. The analog block exploited the mapping tools provided by Anadigm that allow direct implementation of filters, amplifiers, and other functionalities. The digital controller, a finite state machine, was translated from Stateflow into VHDL with an in-house converter, and then the FPGA configuration was obtained through Xilinx tools.

The reconfigurable platform selected for implementation is rich enough to allow

implementing the alternate, mostly digital solution as well. We exploited the ADC available on the FPAA and a finite state machine to perform synchronization, allowing a conversion speed of 1 MS/s with 8 bits of accuracy. Both solutions were tested and interfaced with the custom low power receiver front-end. Overall, the hybrid solution performed better than the purely digital one, showing an improvement of sensitivity of 7dB over the digital implementation. In both cases, performances were limited by a DC offset that could not be removed without developing a custom board for testing. The hybrid solution was able to operate close to the sensitivity of the prototype receiver. Moreover, it allowed reconfigurability of the signal path in terms of filtering and gain so as to adapt to varying signal strengths and bit rates.

As a conclusion, the reconfigurable implementation of this mixed-signal system successfully demonstrated how different tradeoffs between analog and digital could be exploited to implement the baseband section. The encouraging results motivated the selection of the hybrid architecture considering that it can achieve synchronization requirements with lower power consumption due to avoiding the ADC.

4.2 Circuit Level Exploration

Low power consumption should be taken into consideration at all design layers. The lowest abstraction level considered is custom circuit design. On the circuit level, dedicated design techniques can help to accomplish a low power or ultra low power system. The design techniques are in two folds, topology selection and circuit sizing. Topology selection is more like a heuristic process, requiring the designer's knowledge and expertise. Therefore, traditionally it is a manual process. During circuit sizing, to meet the performance requirements and reduce various cost (power consumption, chip area, etc.), designers calculate and adjust the circuit parameters, including component values and dimensions (width and length of transistors, values of resistor, capacitor

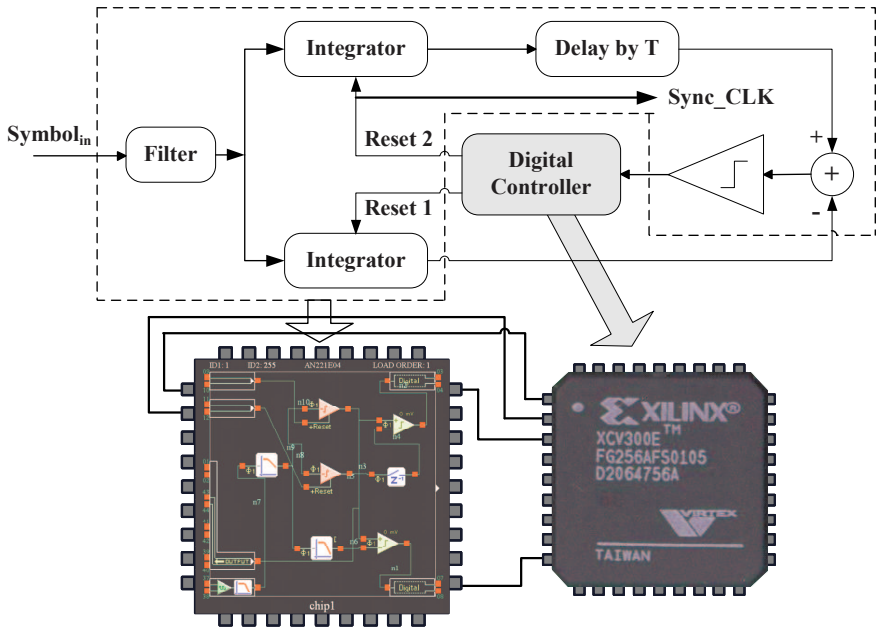


Figure 4.3. Adapted Early-Late Gate synchronizer mapping on the FPAA-FPGA platform

and inductor, etc.) and circuit configurations (bias current, reference voltage, etc.). Due to the intrinsic complexity of RF/analog circuit operation, the circuit sizing is a complicated and time-consuming task. Consequently, the RF/analog circuit design is a manpower-intensive process. Whenever the block specifications are changed, it takes a long time for the designers to propagate the adjusted specifications to the circuit parameters, even if the topology remains same.

In this perspective, the concept of platform can fit well in helping automate or semi-automate the RF/analog circuit level design. The platform based approach is able to efficiently exploit an enriched design space and provide an insight to the optimal regions of feasible performance, allowing designers to save time in sizing a given topology to achieve an optimization goal. Moreover, a platform consisting of different circuitries will enable a better design reuse in the future.

In this section, we will exploit some low power design techniques, and also demonstrate how we perform design space exploration on the circuit level. A library of

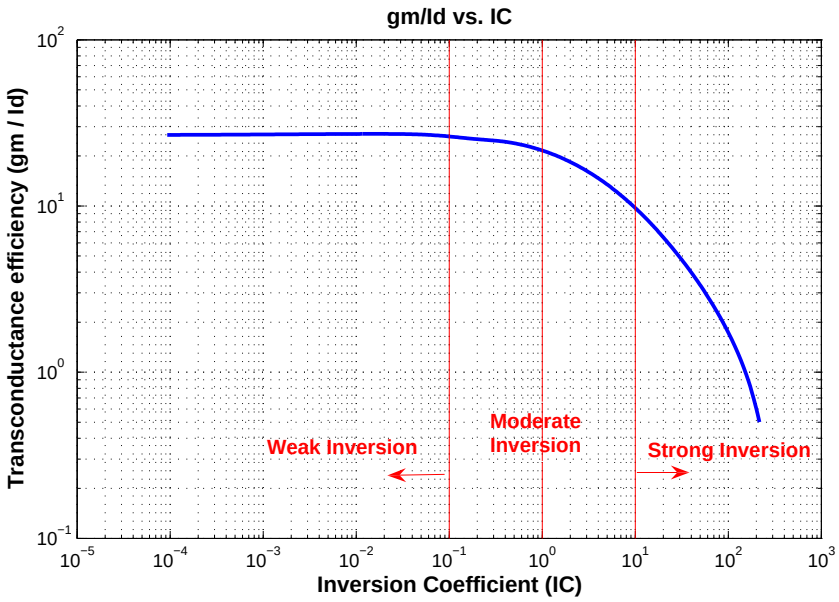


Figure 4.4. Transconductance efficiency ($\frac{g_m}{I_D}$) vs. inversion coefficient (IC)

RF/analog platform components is built to provide an accurate and efficient encapsulating layer. It will be used to map the higher-level functionalities in the later phase of platform-based design flow.

4.2.1 Ultra-Low Power Analog Circuit Design

Subthreshold Circuit Design

The characteristics of a MOSFET are determined by its bias condition. Usually, MOSFETs are biased in strong inversion. The device operation can be described by the square law model. While for low power design consideration, operating a circuit in subthreshold has been proved to be very effective in reducing the power consumption of analog circuits. For analog design, power consumption can be measured by the device drain current I_D. The performance of most analog circuits is directly related to the device small-signal transconductance g_m. Therefore, a useful evaluation is the device transconductance efficiency, that is defined by $\frac{g_m}{I_D}$. We will show that increased

transconductance efficiency can be achieved by biasing the circuit in moderate to weak inversion.

To investigate the device characteristics over the entire bias range, an independent variable, inversion coefficient (IC), is defined to describe the relative degree of inversion for a given bias condition. Fig. 4.4 shows $\frac{g_m}{I_D} \sim IC$ for a typical $0.13\mu m$ process. This plot is obtained by varying the device bias current over a large range. As shown in the plot, $IC = 1$ is defined as the middle of the moderate inversion ($0.1 < IC < 10$), $IC \ll 1$ represents the weak inversion region, and $IC \gg 1$ is considered as strong inversion. Based on the trend of $\frac{g_m}{I_D}$, a design strategy is to bias the critical devices in moderate to weak inversion to achieve enhanced transconductance efficiency and reduced bias current simultaneously.

This low power design technique can be generally applied to analog circuits in low signal frequency and also high frequency. However, there is an important concern when applying to high frequency circuits (e.g. RF). In high frequency design, a critical merit is the device speed. It is usually represented by the device transit frequency (f_T), that is defined as the frequency where the current gain of the device falls to unity. Throughout the different device inversion levels, the trend of f_T is opposite to the trend of $\frac{g_m}{I_D}$. Consequently, when biasing the high frequency circuits, a tradeoff between the device transconductance efficiency $\frac{g_m}{I_D}$ and the transit frequency f_T should be carefully made because f_T in the weak inversion region is much lower than its peak value.

The characteristic $\frac{g_m}{I_D} \sim IC$ depends only on device type (NMOS or PMOS), technology and temperature. Therefore, it provides a universal aid to describe all the devices of one type in a given technology. To facilitate the ultra-low power baseband design, this characteristic has been investigated for a $0.13\mu m$ CMOS technology and a set of plots are obtained from simulation. Fig. 4.5 shows the plots $\frac{g_m}{I_D} \sim IC$ for

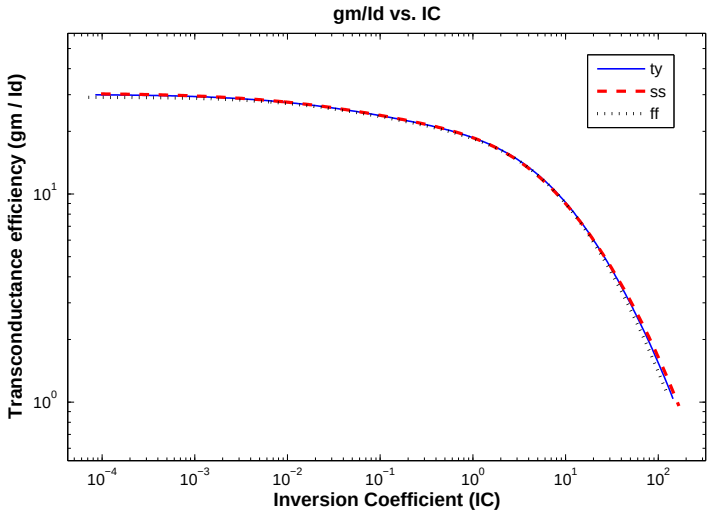


Figure 4.5. $\frac{g_m}{I_D} \sim IC$ plots of different process corners (typical, slow, fast)

various technology corners. It shows that the plot remains almost identical when the technology across different corners (fast, typical, slow). And Fig. 4.6 shows the plots of different device types. Due to higher mobility, NMOS devices have higher I_0 than PMOS.

Device Model

In strong inversion, current flow of a MOSFET is governed by drift current. In subthreshold region, the channel charge is much less than the charge in the depletion region. The current transport mechanism is dominated by diffusion, that is caused by a gradient in minority-carrier concentration.

To facilitate low power circuit design, an accurate device model is critical to describe the devices operating in moderate and weak inversion. The usually used BSIM3V3 device model can not meet our requirements. We adopted the EKV analytical model [20], which works well across all the different inversion levels. It is a charge sheet model, and all the modeling parameters have some physical meanings. The BSIM3V3 device model is an empirical model with hundreds of parameters.

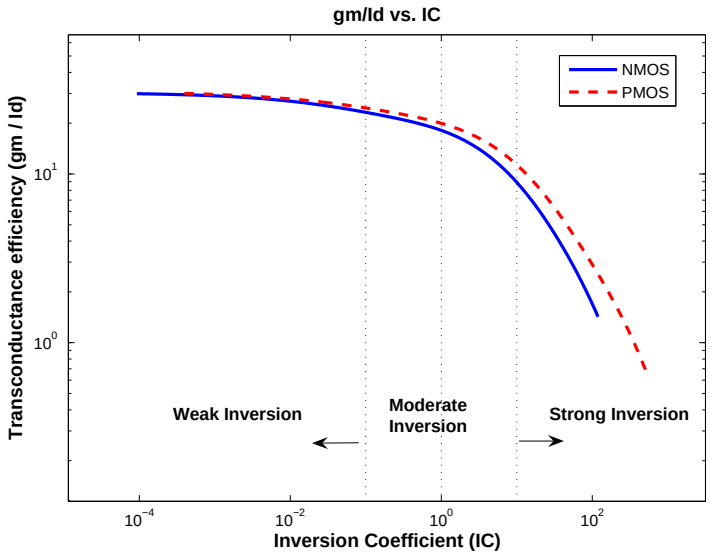


Figure 4.6. $\frac{g_m}{I_D} \sim IC$ plots of different device types (NMOS and PMOS)

Compared to that, the EKV model requires fewer parameters, and the parameter extraction is also easier. Therefore, the EKV model is more suitable for analysis and quick hand calculation. BSIM3V3 models the device $I \sim V$ characteristics, describing the device currents as functions of the terminal voltages. In that model, the voltage V_{GS} is an independent variable. This kind of $I \sim V$ model is suitable for circuit simulator usage. While the EKV model is a current-based model, where the inversion coefficient IC is chosen as an independent design variable. This model is more suitable for analog circuits in that almost all the analog circuits are current-biased circuits.

In weak inversion, the drain current I_D of a MOSFET is described by:

$$I_D = I_0(\frac{W}{L})e^{\frac{V_G - V_{th}}{nU_T}}(e^{\frac{-V_S}{U_T}} - e^{\frac{-V_D}{U_T}}) \tag{4.6}$$

The normalized inversion coefficient IC can be defined as a function of the device dimensions, technology parameters and the device operating point:

$$IC = \frac{I_D}{I_0(\frac{W}{L})} = \frac{I_D}{2n\mu_0 C_{ox} U_T^2(\frac{W}{L})} \tag{4.7}$$

In these equations, V_{th} is the device threshold voltage. $(\frac{W}{L})$ is the device aspect ratio. U_T is the thermal voltage, $U_T = \frac{kT}{q}$. n is the subthreshold slope factor. We can assume it is a constant value, though n has slight gate bias dependency, decreasing with increasing gate bias. I_0 is defined the specific current, which is the normalized drain current of the device that is biased at the center of moderate inversion ($IC = 1$).

Correspondingly, the transconductance efficiency can be derived as following:

$$\frac{g_m}{I_D} \cong \frac{1 - e^{-\sqrt{IC}}}{nU_T\sqrt{IC}} \tag{4.8}$$

$$\cong \frac{1}{nU_T(\sqrt{IC + \frac{1}{4}} + \frac{1}{2})} \tag{4.9}$$

$$\cong \frac{1}{nU_T} \qquad (weak\ inversion) \tag{4.10}$$

$$\cong \frac{1}{nU_T\sqrt{IC}} \qquad (strong\ inversion) \tag{4.11}$$

In the EKV analysis, besides the small-signal quasi-static model (including transconductance, intrinsic capacitances, etc.), it also provides compact expressions for first-order non-quasi static effects, thermal noise, second order effects (including velocity saturation, channel length modulation, short channel effects, etc). The model extensions also consider deep-submicron factors, including device non-uniformities, poly-depletion and quantum effects, charge-sharing for short and narrow channel, drain induced barrier lowering, etc.

The model shows that the drain-source saturation voltage of the device is approximately proportional to $\sqrt{IC}$ in strong inversion, while it is a constant value independent of the inversion level in weak inversion. Since the device in weak inversion has a low saturation voltage, it has the advantage to operate with a reduced supply voltage ($< 1V$), especially in a cascode structure.

Besides the tradeoff between $\frac{g_m}{I_D}$ and f_T, there is also another main concern re-

garding the choice of IC. Operating a device in the weak inversion is expensive in terms of the implementation area since a large $(\frac{W}{L})$ ratio is needed to obtain a small IC. In this sense, biasing the device in moderate inversion is a good compromise between power consumption and silicon area. Moreover, if we consider the technology mismatch, the current mismatch is dominated by the mismatch in threshold voltage $(\frac{\Delta I_D}{I_D} = \frac{\Delta V_{th}}{nU_T})$. The mismatch of threshold voltage (ΔV_{th}) is worst in the deep weak inversion. Considering these tradeoffs, a lower moderate inversion around $0.1 < IC < 1$ is a proper region to operate the device in.

IC-based Circuit Design Approach

The EKV model is valid in all regions of device operation. Especially, it can accurately model the device in moderate and weak inversion, while it has been shown that BSIM3V3 model is unable to fit an extended range of transconductance in moderate inversion. The EKV device model has been shown to produce great fit at all levels of inversion. Therefore, with the EKV model, it is possible to develop a unified design approach exploring the device operation from the strong to the weak inversion.

Using this current based model, there are three degrees of freedom in design: inversion coefficient IC, drain current I_D, channel length L. An IC-based low power design approach is developed to perform circuit sizing, where IC of each device is considered as an additional dimension of design freedom. The approach is shown in Fig. 4.8.

Firstly, based on the simulation of devices in proper bias condition, the EKV model parameters can be extracted through using some fitting algorithm, such as nonlinear least-square algorithm (function *lsqnonlin* in Matlab). For the low power baseband design, the model has been fitted to a $0.13\mu m$ technology, and the Philips MOS MODEL 11 (a surface potential-based model) is used in the simulation. The

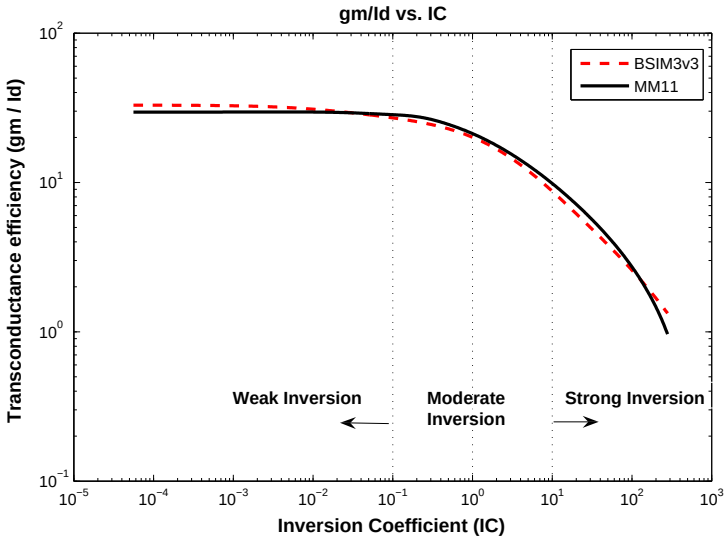


Figure 4.7. $\frac{g_m}{I_D} \sim IC$ plots of BSIM3v3 model and MM11 model

characteristic plots $\frac{g_m}{I_D} \sim IC$ for two different device models are shown in Fig. 4.7. With the extracted parameters, the EKV equations can be used for quick hand calculation. Moreover, as presented in section 4.2.1, these models play a critical role in the subthreshold circuit characterization.

After the model parameter extraction, the specific current I_0 for different types of devices is obtained. That will be used in the IC-based design approach:

- Based on the power budget of a given circuit topology, an initial value of the drain current of each device can be determined. Through the performance analysis of the circuit, the device transconductance g_m can be initially set to a value to meet the performance requirements (e.g. DC gain, f_T).

- Checking the characteristic plot, $\frac{g_m}{I_D} \sim IC$, the corresponding inversion level IC can be obtained. From the other side, the EKV model parameters have been extracted, and the specific current I_0 has been available. Therefore, knowing I_D and I_0, we can derive $IC_0 = \frac{I_D}{I_0}$. With IC obtained from the $\frac{g_m}{I_D} \sim IC$ plot, the device aspect ratio $(\frac{W}{L})$ can be obtained through equation 4.7, $(\frac{W}{L}) = \frac{IC_0}{IC}$.

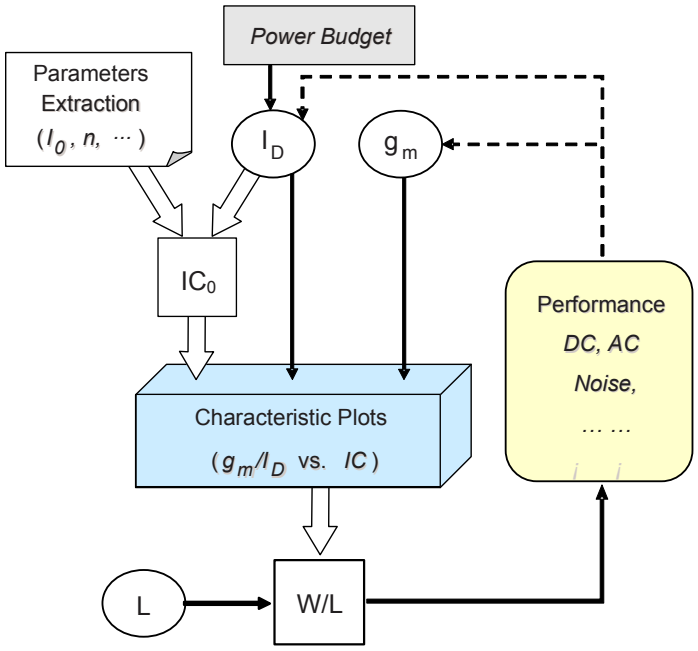


Figure 4.8. IC-based low power design approach

- The channel length (L) of the device is another important design parameter. It should be determined by considering various related performance, including DC gain, noise, mismatch, layout area, and so on. After choosing L, the channel width W is determined from the aspect ratio.

- Finally, the various performance of this circuit is evaluated through analytical calculation or simulation tools.

If the performance can not meet the requirements, the design parameters g_m, I_D, and L should be properly adjusted, and a new set of design parameters can be determined by following the same procedure.

In this design flow, the device operation is not limited to a specific inversion region. Instead, we take advantage of the entire inversion range. Sizing is a unified procedure over the full range of IC. From another perspective, if the designer has an intuitive idea about biasing the device in a specific inversion region, an estimation of IC can be provided. In this case, it is not necessary to set an initial g_m. Alternatively, knowing

the set of design parameters, including IC, I_D, and L, we can also perform the circuit sizing using a similar procedure.

Ultra-Low Power Baseband Circuit Design

To meet the aggressive power consumption requirements of wireless sensor networks and to provide a solution suitable to the target node size, we performed another mapping of the Early-Late Gate synchronization algorithm starting from the hybrid solution, which showed encouraging results from the architectural exploration. We exploited the freedom of designing a custom circuit by choosing a continuous time implementation for the analog sub-system since this choice was likely to provide lower power consumption.

Necessary adjustments were made to the functionality shown in Fig. 4.3. The first two analog pathes implement the feedback synchronization algorithm and perform the timing estimation. On the third path, we use an integrator to average the energy over 10 symbols of alternating 0s and 1s, and the energy is compared to a threshold. This performs the carrier sense capability required by the MAC layer in the protocol. The carrier sense threshold is left programmable so that the MAC layer can make a tradeoff between the probability of miss detect and the probability of false detect. The estimated threshold value is sampled and held for use throughout the data portion of the packet. During data reception, symbols are matched filtered and sliced against the estimated threshold using a comparator. The final diagram is shown in Fig. 4.9.

The custom baseband chip was designed in a $0.13\mu m$ CMOS technology with 1.0V power supply. The analog circuits consist of integrators, a sample & hold, a track & hold, comparators and a precision-gain amplifier (Fig. 4.9). To minimize power consumption, weak inversion operating region was widely exploited throughout the circuit design using the IC-based design approach. In this design, we normally bias the

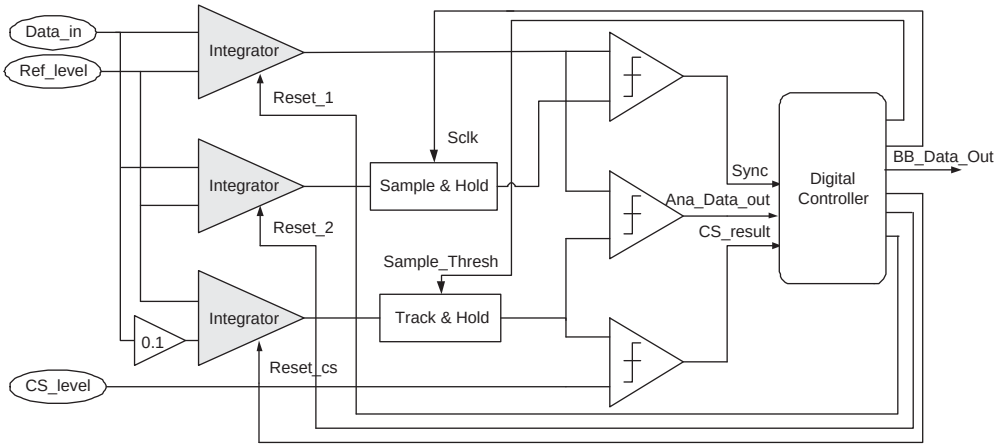


Figure 4.9. Block diagram of the baseband silicon implementation

devices to achieve the transconductance efficiency $\frac{g_m}{I_D} = 20 \sim 30$. The most critical block of the baseband is integrator, in terms of both performance and power consumption. To maximize power efficiency, we adopted an $G_m - C$ structure integrator. OTAs are widely used in analog systems, lots of research work has been done in the OTA design. We investigated several different topologies, including a telescopic OTA structure, a folded cascade structure, and a symmetrical CMOS structure (Fig. 4.10).

One primary design challenge came from the integrators due to the relatively long integration time set by the system data rate (50kbps). The synchronization scheme requires a maximum voltage droop of 2mV over one symbol period (20 μs). With the CMOS process used, a basic $G_m - C$ circuit fails because of excessive discharge rate of the integration capacitor due to the finite output impedance of the OTA. A cascode structure was utilized to increase the output impedance of the OTA and control the droop rate of the output node without resorting to unrealistically high values of integration capacitance. The integration gain is set by the integration capacitor (C_{intg}) and the OTA transconductance G_m, which can be easily tuned by changing the bias current and the sizing ratio between the loading transistors, M_3 and M_5, M_4 and M_6, as shown in the following equation.

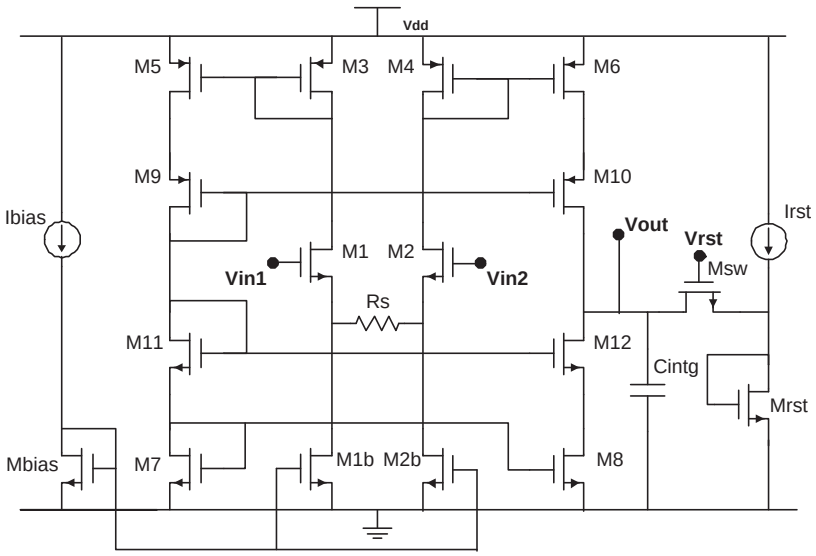


Figure 4.10. Schematic of $G_m - C$ integrator with a symmetrical OTA

$$\frac{dv_{out}}{dt} = \frac{i_{c_{intg}}}{C_{intg}} = \frac{G_m \cdot V_{in}}{C_{intg}} \tag{4.12}$$

Another critical issue with the integrators is the reset path. All three integrators must be reset to the same constant level, independent of the integrated voltages. The potential solution of resetting the capacitor to a node of the OTA results in unacceptable time constants because of the large capacitor and the high impedance at that node. Instead, the integration capacitor is reset to a dedicated branch where a diode connected NMOS (M_{rst}) generates a reference voltage, at the expense of additional bias current. In this way, the reset process can be controlled independently.

On the carrier-sense path, the input signal should be attenuated by 0.1 and then integrated for 10 symbols, providing the reference level for the output signal of the 1st path. One way to realize the 0.1 attenuation is to set a bias ratio between the 1st path and the 3rd path, resulting in a ratio between the Gm of two OTAs. However, this approach demands a fairly high linearity of the integrators to meet the algorithm requirements. The inaccuracy will add offset to the reference level and hence to the

output signal. There is another way to achieve the same functionality. To guarantee integrator gain matching and linearity matching between the first two integrator paths and the carrier-sense path, the same integrator cell was used on all paths. And a dedicated preamplifier was designed to attenuate the input signal by a factor of 10, then the following integrator will integrate for 10 symbols.

As shown in the diagram, comparator is another important block of this baseband design. We designed a comparator comprising a fully differential preamplifier followed by a CMOS latch (Fig. 4.11). The comparator also consists of a cross-coupled S-R latch stage, that is not shown in the schematic.

In this mixed-signal baseband, the digital controller consisted of a finite state machine synthesized using standard flows. The digital control algorithm performs a binary search on the delay between the two paths by controlling the reset signal of the integrators. Finally, the entire baseband implementation is verified by conducting co-simulation of analog circuits and the digital controller. A simulation result is shown in Fig. 4.12, where the input data stream is a 50kHz square wave. When the symbol synchronization is achieved, the Lock signal is set to 1. The square wave output after synchronization is shown in the last waveform. The simulation is performed in various input settings (different amplitude, delay, offset, etc). The synchronization can be accomplished even when the input symbol is as small as 10mV.

Design Space Exploration

Usually, circuit designers need to spend lots of time to manually determine the device sizings and bias conditions in order to achieve optimal circuit performance and low power consumption. Using the PBD flow, this work can be performed by the high-level optimizer, which will automatically decide the optimal sizings and biasings. We performed circuit characterization using the circuit simulators (Spectre/SpectreRF)

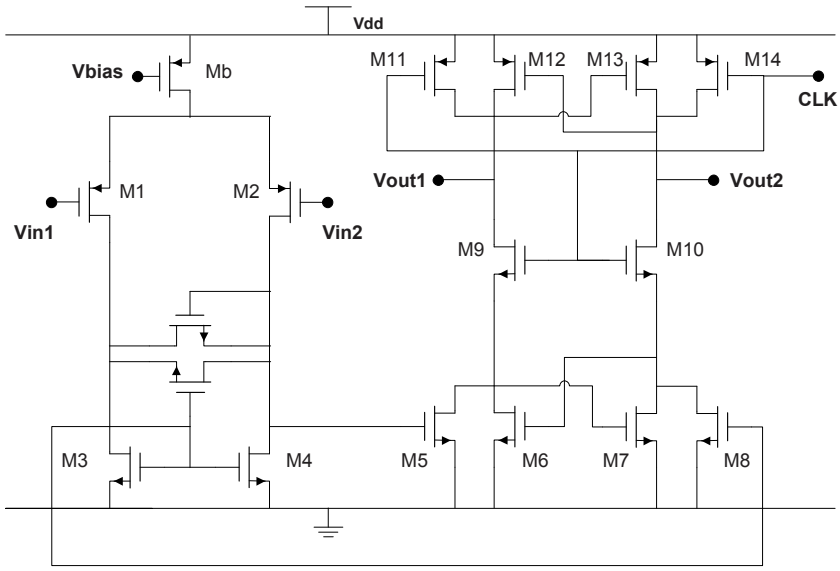


Figure 4.11. Schematic of comparator

and an analog platform characterization framework [18] [13], which is capable of generating circuit configurations and extracting the various performance from the simulation results. The procedure of generating the circuit performance profile can be summarized as following:

- Construct a configuration space spanning by the design parameters such as length and width of transistors, parameters of inductors and capacitors, bias conditions, etc.
- Introduce constraints among the design parameters (e.g. bounding ranges for device sizes, proper operating conditions) to reduce the number of configuration variables and increase the characterization efficiency. The constraints can be simple analytical models that are obtained as a by-product of circuit design.
- By applying the configurations to a proposed circuit topology, a library of circuits with same topology are obtained. Run transistor-level simulations to generate the performance space.

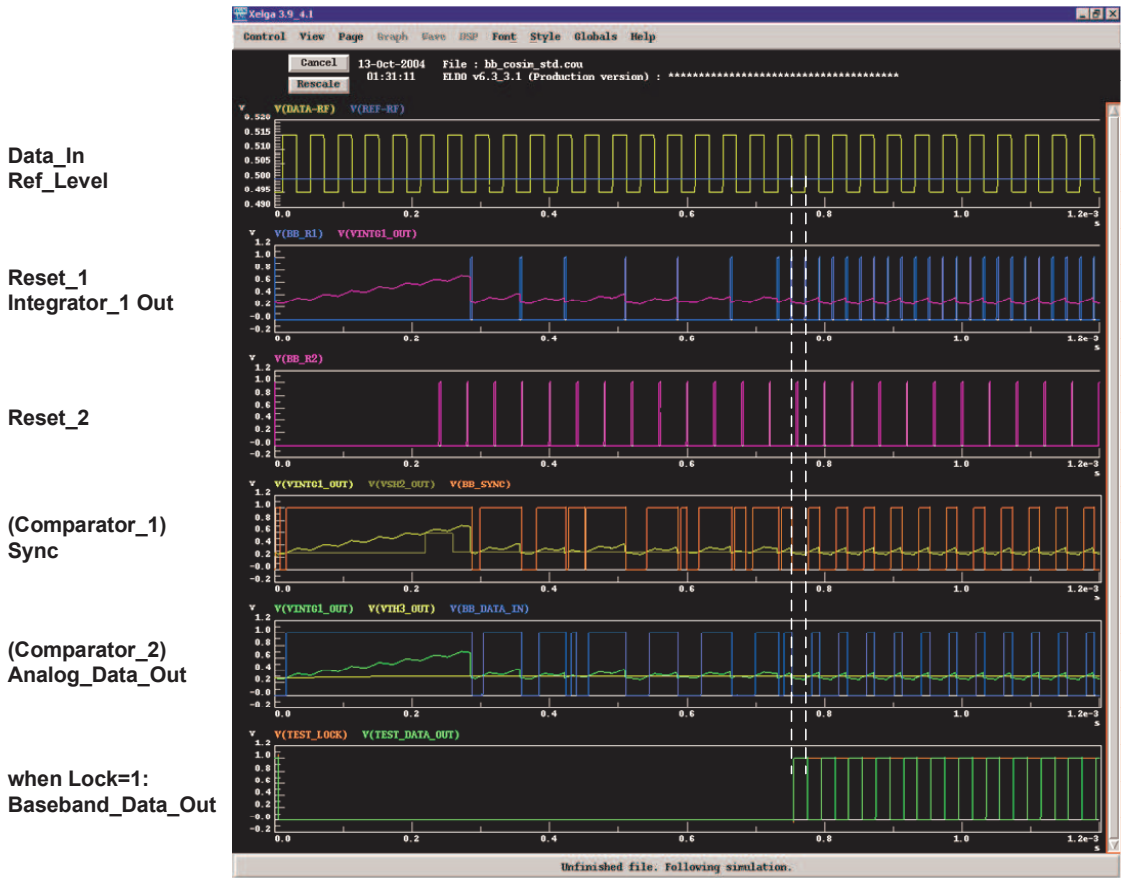


Figure 4.12. Simulation results of the baseband circuits

Using the analog platform characterization framework [18], we can obtain the manifold of performance that can be achieved by that circuit topology, where each point in the performance space corresponds explicitly to a set of design parameters.

For the mostly-analog synchronization scheme, the integrators are essential blocks, whose performance will have critical influence on the whole baseband system. Moreover, in terms of power consumption, the integrators are the dominant blocks. Since the WSN demands extremely low power dissipation, I applied the power constraint as the most important factor to the OTA block, while noise should be controlled within a tolerable level. The performance models of the different OTA structures (i.e. telescopic, folded-cascode, symmetric structure) are generated, giving us good

insight into the limitations and benefits of the different OTA topologies, and help us to determine optimal configurations so as to further minimize power dissipation. From another perspective, through the platform-based design exploration, we hope to get a bottom-up performance characterization of the low-voltage low-power OTAs, so that future design can use the models to estimate performance at a higher level of abstraction.

We made a design space exploration of the integrator to balance several design tradeoffs. To maximize the integration gain while maintaining the input dynamic range required by receiver RF frontend, an optimization of the transconductance G_m was needed. As shown in (4.12), the integration gain can also be improved by choosing a relatively small C_{intg}. However, this will increase the output voltage droop. These tradeoffs needed to be carefully exploited. To characterize the circuit, we defined a feasible configuration space spanning from the integrator design parameters, considering the combination of different biasing, different device sizings and values of the integration capacitance (C_{intg}). Since the characterization cost is exponentially dependent on the size of these parameter combinations, to improve the characterization efficiency, a set of constraints was imposed to restrict the configurations, which include defining bounding ranges for devices size, defining biasing conditions, and using "long" low-leakage transistors for M_{9-12} to reduce the voltage droop. EKV models [20] were exploited to model the device operation and derive the constraints. Then, with the analog platform characterization framework [13], this configuration space was statistically sampled and circuit simulations were carried out in Spectre to obtain a feasible performance space. An example performance projection is shown in Fig. 4.13. In this example, the performance space of the symmetrical topology is in the dimensions of output voltage droop, integration peak level, which is proportional to integration gain, and power consumption.

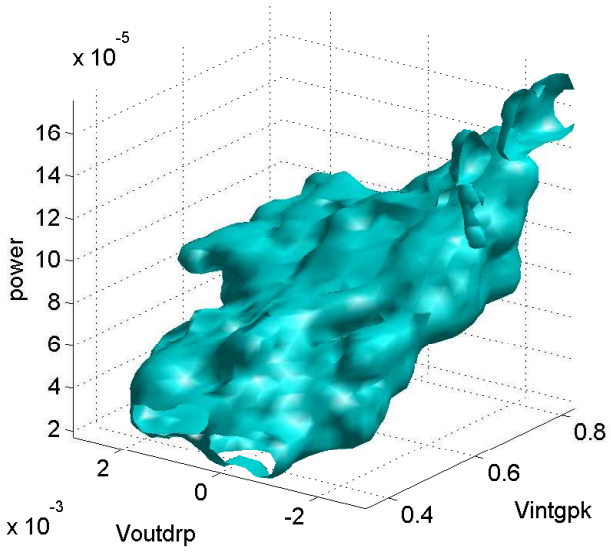


Figure 4.13. Integrator performance space projection. The volume shows a feasible range of the integrator performance in terms of output voltage droop, integration peak level, and power consumption

Using performance models, we carried out a preliminary exploration that allowed us to determine optimal regions in the feasible space. Among the different OTA structures, the symmetrical OTA is selected due to the higher power efficiency. After that, to minimize the power consumption, local optimization of the circuit sizing and bias was carried out manually. This resulted in an optimized integrator current consumption of $16\mu A$ and $C_{intg} = 20pF$. The capacitor value was carefully chosen so that it occupies a reasonable layout area and the integration peak level is in the desired voltage range.

4.2.2 Low Power RF Front-End Design

To realize a power-efficient design, a direct-conversion architecture is selected for the MB-OFDM UWB receiver (Fig. 4.14). The RF front-end includes a T/R switch, a LNA, quadrature mixers and buffers. As the T/R switch and LNA dominate the

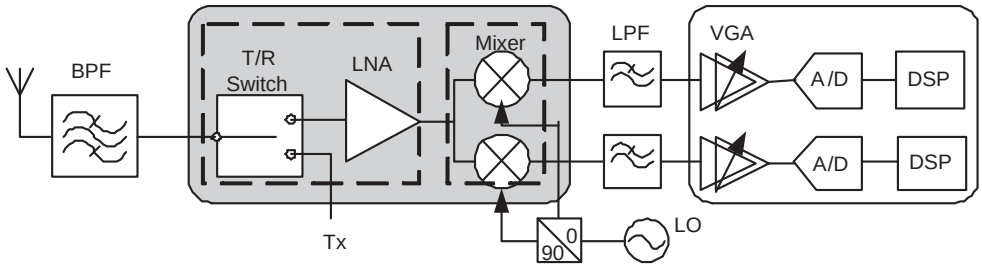


Figure 4.14. Direct conversion UWB receiver architecture.

overall noise performance of the receiver, low insertion loss of the T/R switch and low NF of the LNA are considered as essential design requirements. Besides that, these components must provide input matching over the broad operating band.

Based on a previous LNA design [57], we co-designed a T/R switch with a wideband LNA, as shown in Fig. 4.15. The passive components L1, L2, Ls, and Cs serve as the wideband input matching network. The T/R switch transistors M1 and M2 are also part of the matching network. The LNA employs the stagger tuning technique to achieve good gain flatness over a broad band, which consists of two stacked common-source stages with different resonance frequencies. The first common-source stage consists of the transistor M3 and the inductor L3, resonating at the lower frequency bound of the wide operating band. M4 and L4 serve as the second stage, resonating at the upper frequency bound. RF signal passes through these two amplification stages serially. Consequently, good gain flatness is achieved over a broad band. Our strategy to achieve power savings is to stack these two stages to make them share the bias current. In this topology, noise performance is dominated by the first stage and linearity is dominated by the latter stage.

Following the LNA, quadrature mixers down-convert the RF signal to baseband. An output buffer (M5) is added to LNA to prevent serious performance decay at high frequency caused by the mixer. To isolate the flicker noise and the second

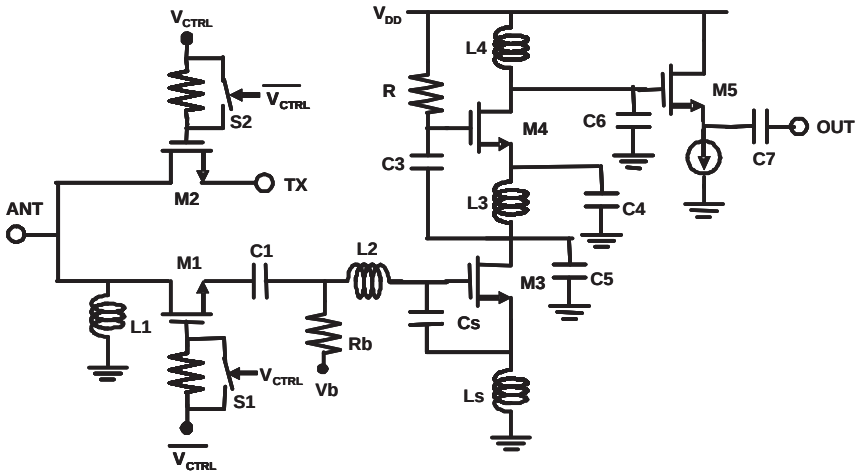


Figure 4.15. Schematic of the T/R switch and the stagger tuning LNA.

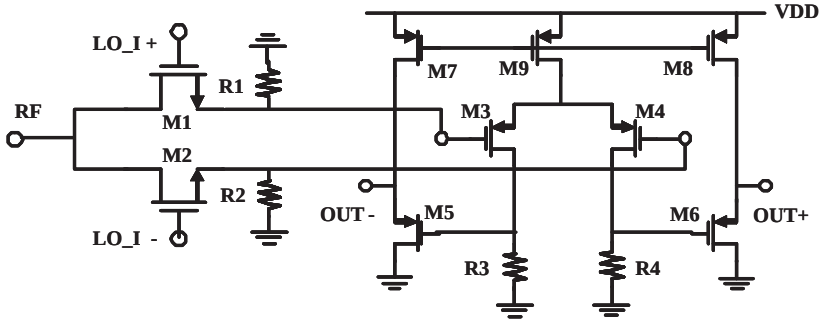


Figure 4.16. Schematic of the Mixer and buffer.

order intermodulation from the LNA, a DC blocking capacitor is inserted between the LNA and the mixer. A passive mixer (Fig. 4.16) is adopted for the advantage of wide bandwidth, low flicker noise, high linearity, and its zero DC power dissipation. A low-noise amplifier buffer (M3∼M8) is designed for the measurement purpose as well as further boosting the mixer gain. Here, to facilitate a relatively low biasing LO signal to drive the mixer, two large resistors, R1 and R2, are used to provide ground bias.

RF Circuit Characterization

For the WSN baseband design, the circuit-level design space exploration is mainly on the most critical blocks, i.e. integrators. When designing the UWB receiver front-end, the characterization is performed for the entire front-end. And the obtained performance model is used to constrain the higher-level behavioral model. Based on this, system-level optimization is conducted in a later design phase.

A multi-dimensional configuration space is constructed including the vectors of device parameters and other important design parameters to allow intelligent construction of the performance profile. For example, the configuration vectors of LNA consist of the bias voltages, length and width of transistors, geometry parameters and parasitic resistance of inductors, capacitor parameters, and so on. In this RF frontend characterization, we developed Analog Constraint Graphs (ACGs) [14] to impose bounding ranges and and other conservative constraints so that the configuration space is limited to a reasonable size and characterization efficiency is increased. The ACG technique exploits constraints through bipartite undirected graphs. Algebraic relations among parameters are introduced so that the overall number of variables is reduced. An ACG of the amplifier buffer is shown in Fig. 4.17.

For RF circuits, the constraint equations also take into account the relevant parasitic effects to ensure accuracy that is similar to the one obtained by direct circuit simulation (SpectreRF) on the circuit level model. In addition, proper fitting process was performed to adjust the analytical device models to be consistent to the models used in simulation. For example, when applying foundry design kits to the SpectreRF simulation, we found that the inductance and the inductor quality factor deviated from the analytical model due to the geometrical parameters, such as metal width, number of turns, metal spacing, and diameter. Based on a 0.13μm MMRF

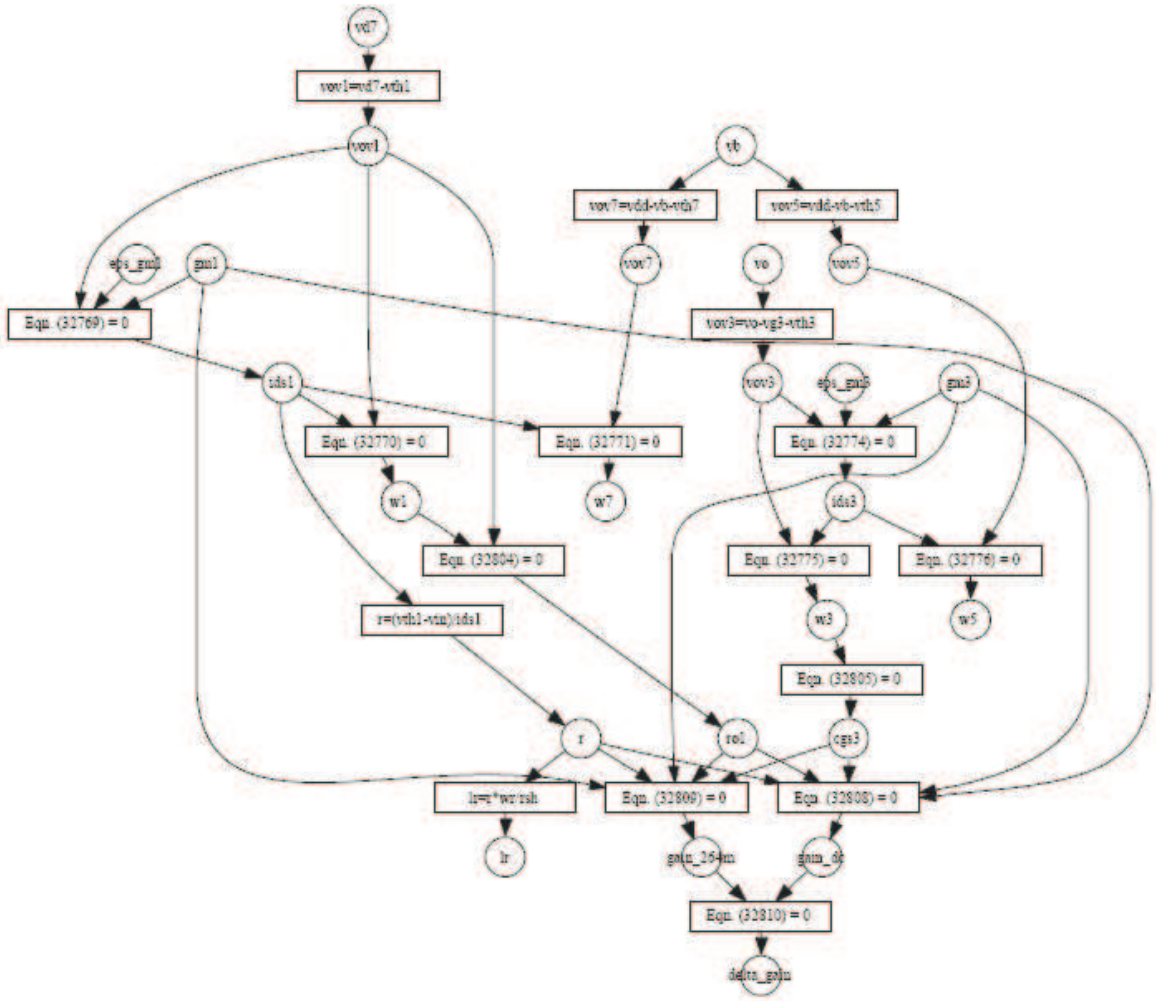


Figure 4.17. ACG of the mixer buffer

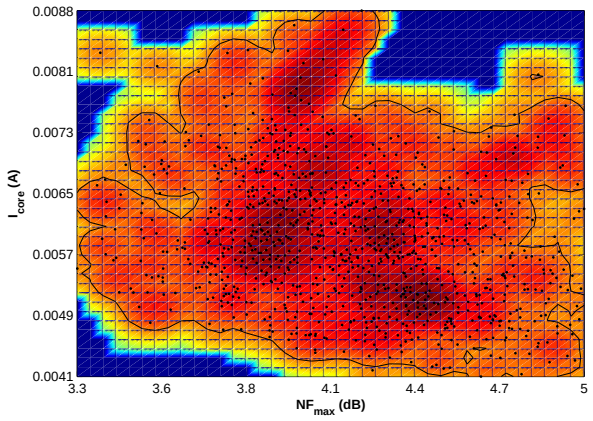


Figure 4.18. A projection of LNA performance space. The area restricted by the boundary shows the achievable NF_{max} and current dissipation.

CMOS device models, a model fitting approach is developed to effectively involve the parasitic effects and make the analytical device models match the simulation results:

- The circuit small-signal model is created with all known parasitics, and the model parameters are tuned to fit the key performances (e.g. S21 and S11) obtained from SpectreRF.
- Symbolic equations of the tuned models are built using MATLAB toolbox, and these equations are plugged to facilitate the numerical operations of the ACG equations.

For both LNA (together with T/R switch) and mixers, the generated performance profile includes the critical circuit characteristics (e.g. gain), the important non-idealities (e.g. NF_{max}, NF_{min}, IIP2, IIP3), and implementation costs (e.g. power, area). As an example, Fig. 4.18 shows a projection of the high-dimensional performance profile of LNA into NF_{max} and the current dissipation. It is shown that the achievable minimum NF_{max} is 3.4dB, and the minimum current consumption is around 4.2mA.

During the later top-down process, these performance profiles will be used to

config the coefficients of the higher-level behavioral models. Consequently, using the behavioral models, the front-end optimization is restricted to visit only the feasible circuit performances (within the profile boundaries). With these performance profiles, another benefit is that automatic selection of the optimal design parameters will be performed quickly since no circuit simulation is required.

As a summary, the circuit level characterization accomplishes a mapping from the circuit configuration space to the performance space. And the obtained performance models will be used to config the higher-level behavioral models. We do not need to size the devices to achieve an optimal circuit performance manually. Instead, we generated a performance profile for each circuit, i.e., the manifold of performance that can be achieved by the circuit. Each point of the performance space corresponds explicitly to a set of device parameters. Consequently, automatic selection of the optimal device parameters during the later top-down process can be performed quickly since it will not need any circuit simulation. When doing a system-level optimization, we only search into the extracted performance models, while the configuration models of circuit level are hidden behind.

Chapter 5

Optimization and Implementation

In the previous sections, the bottom-up phase of the platform-based receiver system design is presented. RF/analog platforms at circuit level and architectural level have been created. Behavioral models are introduced so that the level of abstraction is raised and the performance evaluation can be achieved efficiently. Based on this, efficient optimization can be carried out to realize the system level design space exploration. The accurate performance models obtained from the platform characterization guarantee the implementability of a selected system design.

In this section, with the support of the bottom-up platform characterizations, a top-down process of mapping the system-level specifications to circuit platforms will be demonstrated. This is the *meet-in-the-middle* principle of PBD. Optimization is performed on user defined cost functions while satisfying the performance requirements using behavioral models that reflect the architectural and circuit solutions available to us. Here, the optimization problem will be defined in the performance space because all the unnecessary implementation details have been hidden behind the platform abstractions. At the end of the optimization process, an optimal per-

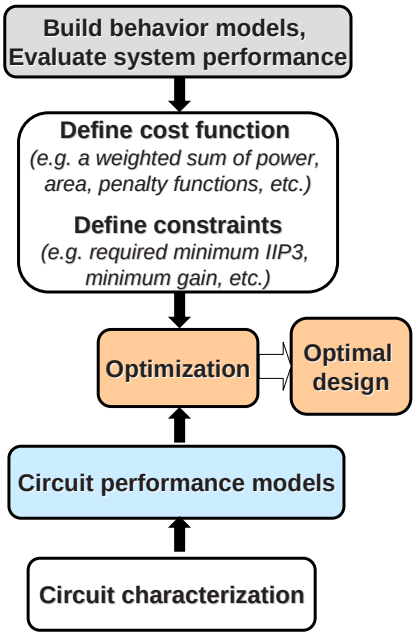


Figure 5.1. Platform mapping

formance vector is obtained and a set of corresponding configuration parameters will also be available for a concrete implementation.

5.1 Meet-in-the-middle Optimization

Based on the PBD framework, the top-down design mapping of the UWB front-end can be performed by an optimization process, as illustrated in Fig. 5.1. Knowing the performance profile of BPF based on the existing designs (IL_{BPF} = 1.0-1.8dB), and typically IL_{RX}=2.5dB, we transformed the system design specifications to the performance requirements of the UWB receiver front-end. Then, an optimization process using the behavioral models mapped the requirements to the circuit platforms, as illustrated in Fig. 5.2. Our optimization goal is to minimize the front-end cost function $\mathcal{F}(power, area, NF, Gain)$ while satisfying the design requirements:

$$\min\{\mathcal{F}(\cdot) = \alpha_1 \cdot power + \alpha_2 \cdot area + \alpha_3 \cdot \Phi_1(NF) + \alpha_4 \cdot \Phi_2(Gain)\}$$

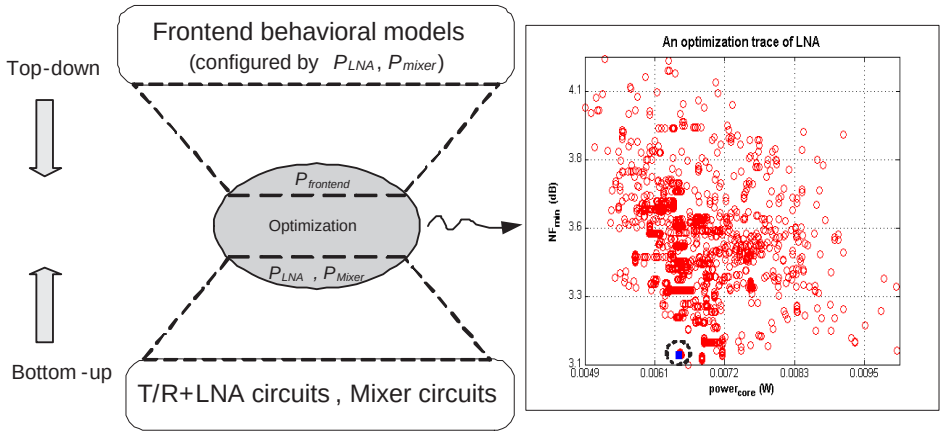


Figure 5.2. *meet-in-the-middle* optimization process for the UWB front-end. The performance space P_{LNA} and P_{mixer} are generated from the circuit characterization. The front-end performance $P_{front-end}$ is evaluated by means of its behavioral model. On the optimization trace, the square marker (within the dashed circle) indicates the optimal NF_{min} and power consumption of LNA.

s.t.

$$\begin{cases} Equ.(3.35) \\ IIP3 \geq -23dBm \\ NF \leq 5.0dB,\ Gain \geq 24dB \end{cases} \tag{5.1}$$

where Φ_1, Φ_2 are the penalty functions we defined for front-end NF and Gain, and α_i reflects the contribution weights from different cost terms. We used a stochastic global optimizer, Simulated Annealing, which was customized for the PBD framework. After optimization, an optimal performance vector of the front-end and the performance breakdown between the LNA and the mixer were provided. Correspondingly, with the support of the circuit performance space, the configuration parameters of all the circuits were obtained so that an optimal design of the UWB front-end circuits was immediately available. The simulated performance is compared to a manually optimized implementation (an industrial design), as shown in Table. 5.1. A total power savings of 22.3% was achieved.

As shown here, using the PBD methodology, design optimization is efficiently performed using behavioral models at the system level and taking into consideration

architectural constraints and implementation costs at the circuit level. With the circuit platforms, the feasibility of the optimization results is guaranteed, which is an essential and unique benefit associated with PBD. If the system design specification is modified, we just need to define a new optimization problem and run the optimizer again, then a new optimal circuit solution will be available without running any circuit simulation.

Table 5.1. Performance Comparison

Front-end perf.	**Previous chip**	**Optim. design**
Band (GHz)	3.1-4.8	3.1-4.8
Voltage Gain (dB)	23.0-27.6	27.5-29.2
NF (dB)	5.0-6.9	4.36-5.05
IIP3 (dBm)	-22.0 - -19.6	>-22.5
P_{1dB} (dBm)	-34.3 - -31.8	>-34.6
S11 (dB)	<-7.5	<-11.8
Power (mW)	13.9	10.8
Technology	0.13μm CMOS	0.13μm CMOS

This concludes our design of the RF front-end for an MB-OFDM UWB receiver using the platform-based methodology. At system level, the interference impacts were investigated and statistical analysis was performed to evaluate the inter-modulation products of various interferences. We also demonstrated how the narrow-band two-tone approach should be properly adjusted to be applied to UWB systems. For the receiver front-end, we presented the building blocks design, the platform characterization process, and the abstract behavioral models. Finally, by mapping the system requirements to circuit platforms, we obtained a UWB front-end consuming 10.8mW with 1.2V voltage supply in a 0.13μm CMOS technology, achieving a 22.3% savings of power compared to a manually optimized industrial design. This optimal RF front-end design successfully demonstrated the effectiveness of the platform-based receiver design approach.

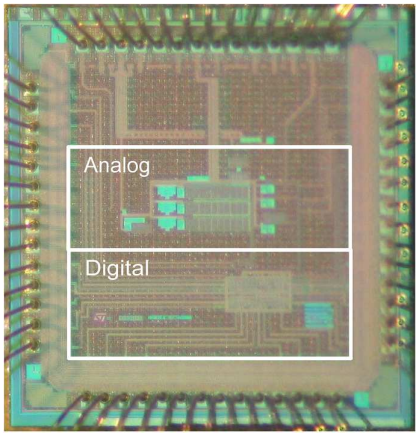


Figure 5.3. Die photograph

5.2 Silicon Implementation

Our baseband design for wireless sensor networks was fabricated in a $0.13\mu m$ CMOS process. The die photograph of the baseband is shown in Fig. 5.5. The chip area is pad limited to 2.0mm^2 (the active die area is 0.8mm^2).

System-level tests were performed using the measurement setup shown in Fig. 5.4. A Rohde & Schwarz RF signal generator synthesizes the transmitter, which is driven by square wave modulation. The custom transceiver chip [35] is set in receive mode. The output of the receiver is fed into the mixed-signal baseband. A Xilinx FPGA is used to generate the 500kHz clock and system reset signal for the baseband and a 25kHz square wave modulation signal to drive the transmitter, which produces the RF signal of 2GHz. The data output from baseband is fed back to the FPGA and compared to the original modulation signal. This provides synchronization verification and bit error rate (BER) testing capability.

Fig. 5.5 shows the baseband operation with the radio. The synchronization process is demonstrated through the reset signal in Fig. 5.5(a). Fig. 5.5(b) shows the baseband operation after synchronization is successfully achieved. The first waveform shows the noisy input data stream (50kbps) with amplitude of around 20mV. The reset signal to

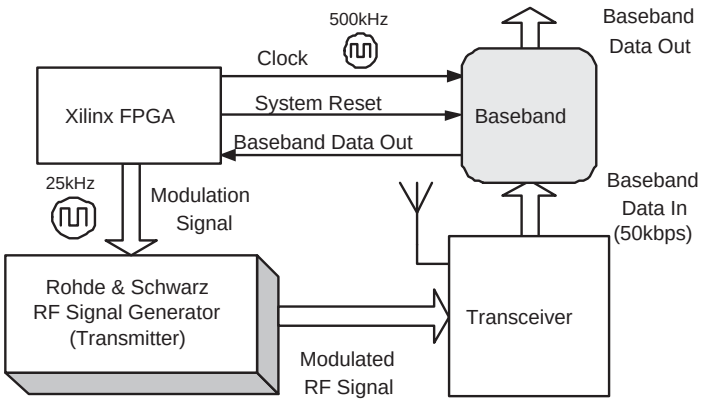
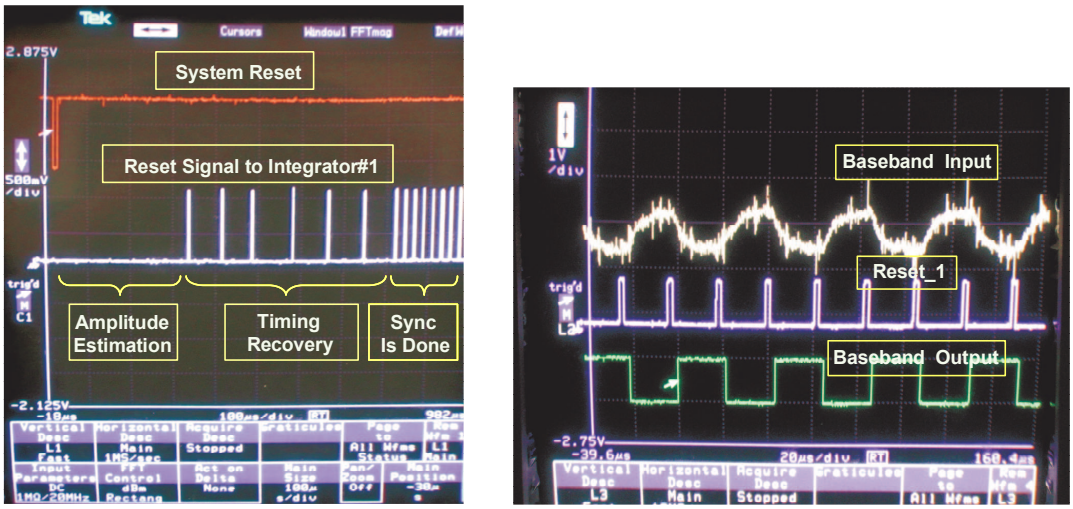


Figure 5.4. Measurement setup

the first integrator is shown as the second waveform. The synchronization is successful if this reset signal has the same timing as the rising (or falling) edge of input data. The last waveform is the data output from the baseband. As designed, there is a one-bit delay between the input and output data. The synchronization header length is 10 bits for amplitude estimation and 20 bits for timing estimation in the worst case. The minimum input level is around 20mV, which is limited by the integrator offset. Based on the measurement setup, the baseband is able to synchronize down to the sensitivity of the transceiver (-78dBm).

Using the internally-generated biasing, the analog circuits draw 180μA of current from the 1.0V supply, and the digital part draws 13μA. By externally setting lower bias currents, the baseband is still able to synchronize with a power consumption as low as 120μW. Decreasing the data rate further reduces power consumption. At a 20kbps data rate the baseband consumes only 80μW. In addition, another possibility to cut down power consumption is by turning off the second path and the first comparator after synchronization as they are not needed after synchronization is achieved. This would result in a reduction in power consumption of around 25%.

In conclusion, this mixed-signal baseband for wireless sensor networks demonstrated how an ultra-low power design can be accomplished by using the platform-



(a) Synchronization process (b) After synchronization

Figure 5.5. Baseband operation with the radio

Table 5.2. Baseband Design Summary

Technology	$0.13\mu m$ CMOS
Power Supply	1 V
Chip Area	2.0 mm^2 (pad limited)
	active die area 0.8 mm^2
Total Power	$\sim$ 193 μW (internally biasing)
	$\sim$ 120 μW (externally biasing)
Synch. Header	Amplitude estimation: 10 symbols
	Timing recovery: 20 symbols (worst case)

based design paradigm. The system design proceeded by successive refinements and mapping, from the initial algorithm selection and analog/digital signal partition to a preliminary mapping on a reconfigurable prototype platform and finally to a silicon implementation for ultra-low power consumption.

Chapter 6

Conclusions

6.1 Conclusions

The rapid evolution of wireless communication technology has changed people's life and helped explore many new adventures. However, the demands for higher speed communication and more efficient multi-function services posed many challenges on the design industry. This dissertation proposes a new design methodology for overcoming these challenges.

With the constantly increasing system complexity, the biggest challenge of designing a wireless transceiver system is to meet the demanding requirements of high performance and low power consumption simultaneously. Moreover, to grab a competitive marketing position, such a system design must be accomplished in a tight time-to-market window. We believe that these contradicting objectives can be accommodated by taking advantages of system-level design exploration and better reuse. A methodology based on the paradigm of platform based design has been investigated in this dissertation.

In this research, the platform-based design flow for transceiver systems was demon-

strated from the system level down to the circuit level. It is critical to estimate at a higher abstraction level the performance impact from the circuit implementations. The gap between system level and circuit level is bridged by the architectural platforms, where behavioral models are built to describe the functionality, whereas the performance and cost estimation of lower levels are captured by the performance model and used to constrain the behavioral models. The evaluation of system tradeoffs is performed at high level of abstraction. Besides the platform-based design flow, this dissertation also demonstrated that low power consumption should be taken into consideration at all design layers, for instance, performing an accurate estimation of the interference effects at system level, evaluating different signal partitions at the architectural level, adopting proper subthreshold design techniques at circuit level, etc.

The methodology was successfully applied to two designs in radio frequency and in low frequency respectively. The RF design is a front-end part of a UWB receiver. The main design challenges are posed by the low power consumption, ultra-wide band operation, and the robustness against other wireless services. We took advantages of the behavioral models, which expose the circuit non-idealities at the system level. The low frequency design is the baseband design for the wireless sensor networks. The challenge mainly lies in the ultra-low power consumption for energy scavenging purpose. A mixed-signal design was investigated to meet the design objectives.

The methodology presented in this dissertation provides a systematic way to evaluate system tradeoffs and make rigorous system-level optimization, which otherwise have to rely on the experience and intuition of the system architect. The results in this dissertation demonstrated very promising solutions, which reduce power consumption further beyond the original design choices.

For a new system that has not been well developed, a potential benefit of the auto-

matic design space exploration is that new insights and innovative solutions might be exposed. This offers the capability to develop new state-of-the-art systems. Although the techniques presented in this dissertation were investigated in the context of low power transceiver systems, they can certainly be extended to other RF/analog/mixed-signal systems.

6.2 Future Research Directions

With further enhancement, this platform based approach will certainly open a new door for wireless system design. There are several issues for future research:

- Extend the platform characterization to achieve seamless shift to a new technology. The circuit characterization tool and the resulting performance space can provide good assistances to automatically exporting existing designs to a more advanced technology. This feature will greatly facilitate designers to mitigate the product into a new generation.

- Develop supporting features in the heterogeneous design environment, MetroII. An RF/analog/mixed-signal system exploration using the proposed methodology can be well fit, described and simulated in MetroII.

- Combine proper model order reduction techniques into the current behavioral model generation. The objective is to obtain a compact model that can capture the non-ideal effects of RF/analog circuits and provide enough accuracy. The implementation of the model should be able to plug into the current platform-based flow, and a higher-level evaluation based on this behavioral model should require reasonable computational resources.

Appendix A

Inter-modulation Products

A.1 WBI and NBI

We model the NBI as a single-tone sinusoid signal, and the WBI as defined in (3.5):

$$\begin{aligned} S_{NBI}(t) &= A_{NBI}\cos(\omega_{NBI}t+\theta) \\ S_{WBI}(t) &= I_{WBI}(t)+Q_{WBI}(t) \\ &= g_T(t+\phi)\sum_{n=-\frac{N}{2}}^{\frac{N}{2}}[i_n\cos((\omega_{WBI}+n\Delta\omega)t+\psi) \\ &\quad +q_n\sin((\omega_{WBI}+n\Delta\omega)t+\psi)] \end{aligned} \tag{A.1}$$

where A_{NBI}, ω_{NBI}, θ are the amplitude, center frequency, and random phase of the NBI. When S_{NBI} and S_{WBI} pass through a receiver front-end with nonlinearities, according to (3.1), the third order nonlinear outputs are represented as:

$$S_{3rd}(t) = k_3[A_{NBI}\cos(\omega_{NBI}t+\theta)+[I_{WBI}(t)+Q_{WBI}(t)]]^3 \tag{A.2}$$

We only count the IMD terms that will fall into the band of interest, therefore, the contribution consists of:

$$S_{IM3}(t) = 3k_3A_{NBI}\cos(\omega_{NBI}t+\theta)[I_{WBI}(t)+Q_{WBI}(t)]^2 \tag{A.3}$$

Expanding this expression, and neglecting out-of-band terms, we obtain the distortion products that will be responsible for the SNR degradation. There are two different cases:

Case I: As shown in Fig. 3.4, the NBI is inside or adjacent to the band of interest. Among the distortion components expanded from (A.3), we are only interested in those adjacent to ω_{NBI}.

Case II: As shown in Fig. 3.5, the NBI are out-of-band interferences. We only consider the resulting IMD terms adjacent to $2\omega_{WBI} - \omega_{NBI}$.

According to the Wiener-Khinchin theorem, the power spectral density can be obtained by taking the Fourier transform of the autocorrelation function, $R(\tau)$, of the signal if the signal can be treated as a stationary random process:

$$PSD_{IM3}(f) = \int_{-\infty}^{\infty} R_{IM3}(\tau) e^{-j2\pi f\tau} d\tau \tag{A.4}$$

The autocorrelation function of a wide-sense-stationary random process is defined by the expectation operation $E\{\cdot\}$:

$$R_{IM3}(\tau) = E\{S_{IM3}(t) S_{IM3}(t+\tau)\} \tag{A.5}$$

Without loss of generality, we set $t = 0$ when applying the autocorrelation operation to the third order IMD product $S_{IM3}(t)$ as shown in (A.3). We obtain:

$$\begin{aligned}
R_{IM3}(\tau) &= E\{S_{IM3}(0) S_{IM3}(\tau)\} \\
&= 9k_3^2 A_{NBI}^2 E_\theta\{cos(\theta) cos(\omega_{NBI}\tau + \theta)\} \\
&\quad \cdot E_{\phi,\psi,i,q}\{I_{WBI}^2(0) I_{WBI}^2(\tau) + Q_{WBI}^2(0) Q_{WBI}^2(\tau) \\
&\quad + I_{WBI}^2(0) Q_{WBI}^2(\tau) + Q_{WBI}^2(0) I_{WBI}^2(\tau) \\
&\quad + 4 I_{WBI}(0) Q_{WBI}(0) I_{WBI}(\tau) Q_{WBI}(\tau) \\
&\quad + 2 I_{WBI}^2(0) I_{WBI}(\tau) Q_{WBI}(\tau) + 2 Q_{WBI}^2(0) I_{WBI}(\tau) Q_{WBI}(\tau) \\
&\quad + 2 I_{WBI}(0) I_{WBI}^2(\tau) Q_{WBI}(\tau) + 2 I_{WBI}(0) Q_{WBI}(0) Q_{WBI}^2(\tau)\}
\end{aligned} \tag{A.6}$$

With the properties of Kronecker delta (3.19), some terms in (A.6) are zeros, and the autocorrelation function can be simplified to

$$\begin{aligned}
R_{IM3}(\tau) &= E\{S_{IM3}(0)S_{IM3}(\tau)\} \\
&= 9k_3^2A_{NBI}^2E_\theta\{\cos(\theta)\cos(\omega_{NBI}\tau+\theta)\} \quad \texttt{--(I)} \\
&\quad \cdot E_{\phi,\psi,i,q}\{I_{WBI}^2(0)I_{WBI}^2(\tau)+Q_{WBI}^2(0)Q_{WBI}^2(\tau) \quad \texttt{--(II-A)} \\
&\quad +I_{WBI}^2(0)Q_{WBI}^2(\tau)+Q_{WBI}^2(0)I_{WBI}^2(\tau) \quad \texttt{--(II-B)} \\
&\quad +4I_{WBI}(0)Q_{WBI}(0)I_{WBI}(\tau)Q_{WBI}(\tau)\} \quad \texttt{--(II-C)}
\end{aligned} \tag{A.7}$$

Now, let's look at each term in the above equation, term (I) is:

$$\begin{aligned}
&E_\theta\{\cos(\theta)\cos(\omega_{NBI}\tau+\theta)\} \\
&= E_\theta\{\tfrac{1}{2}[\cos(\omega_{NBI}\tau+2\theta)+\cos(\omega_{NBI}\tau)]\} \\
&= \tfrac{1}{2}\cos(\omega_{NBI}\tau)
\end{aligned} \tag{A.8}$$

Term (II-A):

$$\begin{aligned}
&E_{\phi,\psi,i,q}\{I_{WBI}^2(0)I_{WBI}^2(\tau)\} \\
&= E_\phi\{g_T^2(\phi)g_T^2(\tau+\phi)\}\cdot \\
&\quad E_{\psi,i,q}\{\textstyle\sum_{k,l,m,n} i_ki_li_mi_n\cos^2\psi\cos[(\omega_{WBI}+n\Delta\omega)\tau+\psi]\cos[(\omega_{WBI}+m\Delta\omega)\tau+\psi]\} \\
&= R_{g^2}(\tau)\textstyle\sum_{k,l,m,n}E_i\{i_ki_li_mi_n\}\cdot \\
&\quad E_\psi\{\cos^2\psi\cos[(\omega_{WBI}+n\Delta\omega)\tau+\psi]\cos[(\omega_{WBI}+m\Delta\omega)\tau+\psi]\}
\end{aligned} \tag{A.9}$$

In equation A.9,

$$\begin{aligned}
&E_i\{i_ki_li_mi_n\} = \delta_{kl}\delta_{mn}+\delta_{km}\delta_{ln}+\delta_{kn}\delta_{lm}-2\delta_{kl}\delta_{km}\delta_{kn} \\
&E_\psi\{\cos^2\psi\cos[(\omega_{WBI}+n\Delta\omega)\tau+\psi]\cos[(\omega_{WBI}+m\Delta\omega)\tau+\psi]\} \\
&= E_\psi\{\tfrac{1}{2}(\cos 2\psi+1)\tfrac{1}{2}(\cos[(2\omega_{WBI}+(n+m)\Delta\omega)\tau+2\psi]+\cos[(n-m)\Delta\omega\tau])\} \\
&= \tfrac{1}{4}E_\psi\{\cos 2\psi\cos[(2\omega_{WBI}+(n+m)\Delta\omega)\tau+2\psi]+\cos 2\psi\cos[(n-m)\Delta\omega\tau] \\
&\quad +\cos[(2\omega_{WBI}+(n+m)\Delta\omega)\tau+2\psi]+\cos[(n-m)\Delta\omega\tau]\}
\end{aligned} \tag{A.10}$$

Since $E_\psi\{\cos 2\psi \cos[(n-m)\Delta\omega\tau]\} = 0$, $E_\psi\{\cos[(2\omega_{WBI} + (n+m)\Delta\omega)\tau + 2\psi]\} = 0$, the above equation is transformed to:

$$
\begin{aligned}
&Eqn.(A.10) \\
&= \tfrac{1}{4}\{\tfrac{1}{2}E_\psi\{\cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau\} + \tfrac{1}{2}E_\psi\{\cos[(2\omega_{WBI} + (n+m)\Delta\omega)\tau + 4\psi]\} \\
&\quad +0 + 0 + E_\psi\{\cos(n-m)\Delta\omega\tau\}\} \\
&= \tfrac{1}{4}\{\tfrac{1}{2}\cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau + 0 + \cos(n-m)\Delta\omega\tau\} \\
&= \tfrac{1}{8}\cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau + \tfrac{1}{4}\cos(n-m)\Delta\omega\tau
\end{aligned}
\tag{A.11}
$$

Plug equations (A.11) into equation (A.9),

$$
\begin{aligned}
&E_{\phi,\psi,i,q}\{I^2_{WBI}(0)I^2_{WBI}(\tau)\} \\
&= R_{g^2}(\tau)\textstyle\sum_{k,l,m,n}(\delta_{kl}\delta_{mn} + \delta_{km}\delta_{ln} + \delta_{kn}\delta_{lm} - 2\delta_{kl}\delta_{km}\delta_{kn})\cdot \\
&\qquad [\tfrac{1}{8}\cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau + \tfrac{1}{4}\cos(n-m)\Delta\omega\tau] \\
&= R_{g^2}(\tau)\textstyle\sum_{m,n}[\tfrac{1}{8}\cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau + \tfrac{1}{4}\cos(n-m)\Delta\omega\tau]\cdot \\
&\qquad (\textstyle\sum_{k,l}(\delta_{kl}\delta_{mn} + \delta_{km}\delta_{ln} + \delta_{kn}\delta_{lm} - 2\delta_{kl}\delta_{km}\delta_{kn})) \\
&= R_{g^2}(\tau)\textstyle\sum_{m,n}[\tfrac{1}{8}\cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau + \tfrac{1}{4}\cos(n-m)\Delta\omega\tau]\cdot(N\cdot\delta_{mn} + 1 + 1 - 2\delta_{mn}) \\
&= R_{g^2}(\tau)\textstyle\sum_{m,n}[\tfrac{1}{8}\cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau + \tfrac{1}{4}\cos(n-m)\Delta\omega\tau]\cdot((N-2)\cdot\delta_{mn} + 2) \\
&= R_{g^2}(\tau)\{\textstyle\sum_{m,n}[\tfrac{1}{8}\cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau\cdot((N-2)\cdot\delta_{mn} + 2)] \\
&\quad + \tfrac{N(N-2)}{4} + \textstyle\sum_{m,n}\tfrac{1}{2}\cos(n-m)\Delta\omega\tau\}
\end{aligned}
\tag{A.12}
$$

We use the following notations to represent the above equation:

$$
\begin{aligned}
&E^W_{I_0I_\tau} = \textstyle\sum_{m,n}[\tfrac{1}{8}\cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau\cdot((N-2)\cdot\delta_{mn} + 2)] \\
&E^D_{I_0I_\tau} = \tfrac{N(N-2)}{4} \\
&E^N_{I_0I_\tau} = \textstyle\sum_{m,n}[\tfrac{1}{2}\cos(n-m)\Delta\omega\tau] \\
&E_{\phi,\psi,i,q}\{I^2_{WBI}(0)I^2_{WBI}(\tau)\} = R_{g^2}(\tau)\{E^W_{I_0I_\tau} + E^D_{I_0I_\tau} + E^N_{I_0I_\tau}\}
\end{aligned}
\tag{A.13}
$$

Similarly, another term of (II-A) in equation (A.7) can be derived:

$$
\begin{aligned}
&E_{\phi,\psi,i,q}\{Q^2_{WBI}(0)Q^2_{WBI}(\tau)\} \\
&= E_{\phi}\{g^2_T(\phi)g^2_T(\tau+\phi)\}\cdot \\
&\quad E_{\psi,i,q}\{\textstyle\sum_{k,l,m,n} q_k q_l q_m q_n \sin^2\psi \sin[(\omega_{WBI}+n\Delta\omega)\tau+\psi]\sin[(\omega_{WBI}+m\Delta\omega)\tau+\psi]\} \\
&= R_{g^2}(\tau)\textstyle\sum_{k,l,m,n} E_q\{q_k q_l q_m q_n\}\cdot \\
&\quad E_{\psi}\{\sin^2\psi \sin[(\omega_{WBI}+n\Delta\omega)\tau+\psi]\sin[(\omega_{WBI}+m\Delta\omega)\tau+\psi]\} \\
&= R_{g^2}(\tau)\textstyle\sum_{k,l,m,n}(\delta_{kl}\delta_{mn}+\delta_{km}\delta_{ln}+\delta_{kn}\delta_{lm}-2\delta_{kl}\delta_{km}\delta_{kn})\cdot \\
&\qquad E_{\psi}\{\tfrac{1}{2}(1-\cos 2\psi)\tfrac{1}{2}[\cos[(n-m)\Delta\omega\tau]-\cos[(2\omega_{WBI}+(n+m)\Delta\omega)\tau+2\psi]]\} \\
&= R_{g^2}(\tau)\textstyle\sum_{k,l,m,n}(\delta_{kl}\delta_{mn}+\delta_{km}\delta_{ln}+\delta_{kn}\delta_{lm}-2\delta_{kl}\delta_{km}\delta_{kn})\cdot \\
&\qquad \tfrac{1}{4}E_{\psi}\{\cos 2\psi\cos[(2\omega_{WBI}+(n+m)\Delta\omega)\tau+2\psi]-\cos 2\psi\cos[(n-m)\Delta\omega\tau] \\
&\quad -\cos[(2\omega_{WBI}+(n+m)\Delta\omega)\tau+2\psi]+\cos[(n-m)\Delta\omega\tau]\} \\
&= R_{g^2}(\tau)\textstyle\sum_{k,l,m,n}(\delta_{kl}\delta_{mn}+\delta_{km}\delta_{ln}+\delta_{kn}\delta_{lm}-2\delta_{kl}\delta_{km}\delta_{kn})\cdot \\
&\qquad \{\tfrac{1}{8}\cos(2\omega_{WBI}+(n+m)\Delta\omega)\tau+\tfrac{1}{4}\cos(n-m)\Delta\omega\tau\}
\end{aligned}
\tag{A.14}
$$

Compare equation (A.14) to (A.10) and (A.11), we find that $E_{\phi,\psi,i,q}\{Q^2_{WBI}(0)Q^2_{WBI}(\tau)\} = E_{\phi,\psi,i,q}\{I^2_{WBI}(0)I^2_{WBI}(\tau)\}$.

Next, we look at the terms (II-B) in equation (A.7). It can be proved that $E_{\phi,\psi,i,q}\{I^2_{WBI}(0)Q^2_{WBI}(\tau)\} = E_{\phi,\psi,i,q}\{Q^2_{WBI}(0)I^2_{WBI}(\tau)\}$.

$$
\begin{aligned}
&E_{\phi,\psi,i,q}\{I^2_{WBI}(0)Q^2_{WBI}(\tau)\} = E_{\phi,\psi,i,q}\{Q^2_{WBI}(0)I^2_{WBI}(\tau)\} \\
&= E_{\phi}\{g^2_T(\phi)g^2_T(\tau+\phi)\}\cdot \\
&\quad E_{\psi,i,q}\{\textstyle\sum_{k,l,m,n} i_k i_l q_m q_n \cos^2\psi \sin[(\omega_{WBI}+n\Delta\omega)\tau+\psi]\sin[(\omega_{WBI}+m\Delta\omega)\tau+\psi]\} \\
&= R_{g^2}(\tau)\textstyle\sum_{k,l,m,n} E_i\{i_k i_l\}E_q\{q_m q_n\}\cdot \\
&\quad E_{\psi}\{\cos^2\psi \sin[(\omega_{WBI}+n\Delta\omega)\tau+\psi]\sin[(\omega_{WBI}+m\Delta\omega)\tau+\psi]\} \\
&= R_{g^2}(\tau)\textstyle\sum_{k,l,m,n}\delta_{kl}\delta_{mn}\cdot \\
&\qquad E_{\psi}\{\tfrac{1}{2}(\cos 2\psi+1)\tfrac{1}{2}[\cos[(n-m)\Delta\omega\tau]-\cos[(2\omega_{WBI}+(n+m)\Delta\omega)\tau+2\psi]]\} \\
&= R_{g^2}(\tau)\textstyle\sum_{k,l,m,n}\delta_{kl}\delta_{mn}\cdot \\
&\qquad \tfrac{1}{4}E_{\psi}\{-\cos 2\psi\cos[(2\omega_{WBI}+(n+m)\Delta\omega)\tau+2\psi]+\cos 2\psi\cos[(n-m)\Delta\omega\tau] \\
&\quad -\cos[(2\omega_{WBI}+(n+m)\Delta\omega)\tau+2\psi]+\cos[(n-m)\Delta\omega\tau]\} \\
&= R_{g^2}(\tau)\textstyle\sum_{k,l,m,n}\delta_{kl}\delta_{mn}\cdot \\
&\qquad \{-\tfrac{1}{8}\cos(2\omega_{WBI}+(n+m)\Delta\omega)\tau+\tfrac{1}{4}\cos(n-m)\Delta\omega\tau\} \\
&= R_{g^2}(\tau)\textstyle\sum_{m,n}[-\frac{1}{8}\cos(2\omega_{WBI}+(n+m)\Delta\omega)\tau+\frac{1}{4}\cos(n-m)\Delta\omega\tau]\cdot\delta_{mn}\sum_{k,l}\delta_{kl} \\
&= R_{g^2}(\tau)\textstyle\sum_{m,n}[-\frac{1}{8}\cos(2\omega_{WBI}+(n+m)\Delta\omega)\tau+\frac{1}{4}\cos(n-m)\Delta\omega\tau]\cdot\delta_{mn}\cdot N \\
&= R_{g^2}(\tau)\{\textstyle\sum_{m,n}[-\frac{1}{8}\cos(2\omega_{WBI}+(n+m)\Delta\omega)\tau\cdot N\cdot\delta_{mn}]+\frac{N^2}{4}\}
\end{aligned}
\tag{A.15}
$$

Again, we use short notations:

$$
\begin{aligned}
&E^W_{I_0Q_\tau} = \textstyle\sum_{m,n}[-\frac{1}{8}\cos(2\omega_{WBI}+(n+m)\Delta\omega)\tau\cdot N\cdot\delta_{mn}] \\
&E^D_{I_0Q_\tau} = \tfrac{N^2}{4} \\
&E_{\phi,\psi,i,q}\{I^2_{WBI}(0)Q^2_{WBI}(\tau)\} = E_{\phi,\psi,i,q}\{Q^2_{WBI}(0)I^2_{WBI}(\tau)\} \\
&= R_{g^2}(\tau)\{E^W_{I_0Q_\tau}+E^D_{I_0Q_\tau}\}
\end{aligned}
\tag{A.16}
$$

Finally, we derive the term (II-C) in equation (A.7):

$$
\begin{aligned}
&E_{\phi,\psi,i,q}\{I_{WBI}(0)Q_{WBI}(0)I_{WBI}(\tau)Q_{WBI}(\tau)\} \\
&= E_{\phi}\{g_T^2(\phi)g_T^2(\tau+\phi)\}\cdot \\
&\quad E_{\psi,i,q}\{\textstyle\sum_{k,l,m,n} i_k q_l i_m q_n \cos\psi \sin\psi \cos[(\omega_{WBI}+m\Delta\omega)\tau+\psi]\sin[(\omega_{WBI}+n\Delta\omega)\tau+\psi]\} \\
&= R_{g^2}(\tau)\textstyle\sum_{k,l,m,n} E_i\{i_k i_m\}E_q\{q_l q_n\}\cdot \\
&\quad E_{\psi}\{\cos\psi\sin\psi\sin[(\omega_{WBI}+n\Delta\omega)\tau+\psi]\cos[(\omega_{WBI}+m\Delta\omega)\tau+\psi]\} \\
&= R_{g^2}(\tau)\textstyle\sum_{k,l,m,n}\delta_{km}\delta_{ln}\cdot \\
&\qquad E_{\psi}\{\tfrac{1}{2}\sin 2\psi\tfrac{1}{2}[\sin[(n-m)\Delta\omega\tau]+\sin[(2\omega_{WBI}+(n+m)\Delta\omega)\tau+2\psi]]\} \\
&= R_{g^2}(\tau)\textstyle\sum_{k,l,m,n}\delta_{km}\delta_{ln}\cdot \\
&\qquad \tfrac{1}{4}E_{\psi}\{\sin 2\psi\sin[(2\omega_{WBI}+(n+m)\Delta\omega)\tau+2\psi]+\sin 2\psi\sin[(n-m)\Delta\omega\tau]\} \\
&= R_{g^2}(\tau)\textstyle\sum_{k,l,m,n}\delta_{km}\delta_{ln}\cdot\tfrac{1}{8}\cos(2\omega_{WBI}+(n+m)\Delta\omega)\tau \\
&= R_{g^2}(\tau)\textstyle\sum_{m,n}\tfrac{1}{8}\cos(2\omega_{WBI}+(n+m)\Delta\omega)\tau\sum_{k,l}\delta_{km}\delta_{ln} \\
&= R_{g^2}(\tau)\textstyle\sum_{m,n}\tfrac{1}{8}\cos(2\omega_{WBI}+(n+m)\Delta\omega)\tau\cdot 1 \\
&= R_{g^2}(\tau)E^W_{I_0Q_0I_\tau Q_\tau}
\end{aligned}
\tag{A.17}
$$

Now, plug equations A.8, A.13, A.14, A.16 and A.17 into equation A.7,

$$
\begin{aligned}
&R_{IM3}(\tau) = 9k_3^2A_{NBI}^2\tfrac{1}{2}\cos(\omega_{NBI}\tau)\cdot \\
&R_{g^2}(\tau)\{2(E^W_{I_0I_\tau}+E^D_{I_0I_\tau}+E^N_{I_0I_\tau})+2(E^W_{I_0Q_\tau}+E^D_{I_0Q_\tau})+4E^W_{I_0Q_0I_\tau Q_\tau}\}
\end{aligned}
\tag{A.18}
$$

We consider the two different cases. For Case I, only those components adjacent to ω_{NBI} are of interest. All components around $2\omega_{WBI}$ (i.e. $E^W_{I_0I_\tau}$, $E^W_{I_0Q_\tau}$, $E^W_{I_0Q_0I_\tau Q_\tau}$) will be ignored. Therefore, (A.18) for Case I:

$$
\begin{aligned}
&R_{IM3}(\tau) \\
&= \tfrac{9}{2}k_3^2A_{NBI}^2\cos\omega_{NBI}\tau\cdot R_{g^2}(\tau)\cdot 2\cdot E^N_{I_0I_\tau} \\
&= \tfrac{9}{2}k_3^2A_{NBI}^2\cos\omega_{NBI}\tau\cdot R_{g^2}(\tau)\textstyle\sum_{m,n}\cos(m-n)\Delta\omega\tau \\
&= \tfrac{9}{2}k_3^2A_{NBI}^2\cdot R_{g^2}(\tau)\textstyle\sum_{m,n}[\cos\omega_{NBI}\tau\cos(m-n)\Delta\omega\tau] \\
&= \tfrac{9}{4}k_3^2A_{NBI}^2\cdot R_{g^2}(\tau)\textstyle\sum_{m,n}[\cos(\omega_{NBI}+(m-n)\Delta\omega)\tau+\cos(\omega_{NBI}-(m-n)\Delta\omega)\tau]
\end{aligned}
\tag{A.19}
$$

If we consider the case at ω_{NBI}, there are some additional components from (A.18):

$$\begin{aligned} & R_{IM3\_\omega_{NBI}}(\tau) \\ &= \tfrac{9}{2}k_3^2 A_{NBI}^2 \cos\omega_{NBI}\tau \cdot R_{g^2}(\tau) \cdot 2(E_{I_0 I_\tau}^D + E_{I_0 Q_\tau}^D) \\ &= \tfrac{9}{2}k_3^2 A_{NBI}^2 \cos\omega_{NBI}\tau \cdot R_{g^2}(\tau) \cdot 2(\tfrac{N(N-2)}{4} + \tfrac{N^2}{4}) \\ &= \tfrac{9}{2}k_3^2 A_{NBI}^2 R_{g^2}(\tau)(N^2 - N)\cos\omega_{NBI}\tau \end{aligned} \tag{A.20}$$

Next, according to (A.4), we calculate the Fourier transform for (A.19). $g_T(t)$ is a rectangular function, T is the OFDM symbol total duration:

$$g_T(t) = rect[\frac{t}{T}] = \sqrt{\frac{1}{T}}, \quad \frac{-T}{2} < t < \frac{T}{2} \tag{A.21}$$

$$= 0, \quad elsewhere \tag{A.22}$$

$R_{g^2}(\tau)$ is the autocorrelation of the function $g_T^2(t+\phi) = rect^2[\frac{t+\phi}{T}]$:

$$R_{g^2}(\tau) = E_\phi\{rect^2[\frac{\phi}{T}]rect^2[\frac{\tau+\phi}{T}]\} \tag{A.23}$$

$$= \frac{1}{T} \cdot tri(\frac{\tau}{T}) \tag{A.24}$$

where $tri(\frac{\tau}{T})$ is a triangular function, defined as:

$$tri(\frac{\tau}{T}) = 1 - \frac{|\tau|}{T}, \quad |\tau| < T \tag{A.25}$$

$$= 0, \quad elsewhere \tag{A.26}$$

Fourier transform:

$$\mathcal{F}\{R_{g^2}(\tau)\} = \int_{-\infty}^{\infty} R_{g^2}(\tau)e^{-j2\pi f\tau}d\tau \tag{A.27}$$

$$= \int_{-\infty}^{\infty} \frac{1}{T} tri(\frac{\tau}{T})e^{-j2\pi f\tau}d\tau \tag{A.28}$$

$$= sinc^2(fT) \tag{A.29}$$

$$\begin{aligned} & \mathcal{F}\{\cos(\omega_{NBI} + (m-n)\Delta\omega)\tau\} = \textstyle\int_{-\infty}^{\infty} \cos((\omega_{NBI} + (m-n)\Delta\omega)\tau)e^{-j2\pi f\tau}d\tau \\ &= \tfrac{1}{2}[\delta(f - \tfrac{\omega_{NBI}+(m-n)\Delta\omega}{2\pi}) + \delta(f + \tfrac{\omega_{NBI}+(m-n)\Delta\omega}{2\pi})] \\ &= \tfrac{1}{2}[\delta(f - (f_{NBI} + \Delta f(m-n))) + \delta(f + (f_{NBI} + \Delta f(m-n)))] \end{aligned} \tag{A.30}$$

Applying Fourier transforms on $R_{IM3}(\tau)$ in (A.19), the resulting PSD will be $\mathcal{F}\{R_{g^2}(\tau)\}$ convoluted with a sequence of Dirac pulses located at frequencies $\sum_m \sum_n [f_{NBI} \pm \Delta f(m-n)]$. When the average transmitted signal power of WBI is σ^2_{WBI}, the single-sided power spectral density of IM3 products around frequency f_{NBI} is calculated as:

$$\begin{aligned} PSD_{IM3}(f) &= \tfrac{9}{4} k_3^2 A_{NBI}^2 \sigma_{WBI}^4 \\ &\cdot \sum_{m=-\frac{N}{2}}^{\frac{N}{2}} \sum_{n=-\frac{N}{2}}^{\frac{N}{2}} sinc^2((f - (f_{NBI} + (m-n)\Delta f))T) \end{aligned} \tag{A.31}$$

For Case II, only those components around $(2\omega_{WBI} - \omega_{NBI})$ are of interests. Therefore, all components around $2\omega_{WBI}$ (i.e. $E^W_{I_0 I_\tau}$, $E^W_{I_0 Q_\tau}$, $E^W_{I_0 Q_0 I_\tau Q_\tau}$) will be taken into account, while the components around ω_{NBI} (i.e. $E^N_{I_0 I_\tau}$) and the components ($E^D_{I_0 I_\tau}$, $E^D_{I_0 Q_\tau}$) will be ignored. We first derive:

$$\begin{aligned} & R_{g^2}(\tau)\{2E^W_{I_0 I_\tau} + 2E^W_{I_0 Q_\tau} + 4E^W_{I_0 Q_0 I_\tau Q_\tau}\} \\ &= R_{g^2}(\tau) \cdot \\ &\quad \{2 \textstyle\sum_{m,n} [\frac{1}{8} \cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau \cdot ((N-2)\cdot \delta_{mn} + 2)] \\ &\quad + 2 \textstyle\sum_{m,n} [-\frac{1}{8} \cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau \cdot N \cdot \delta_{mn}] \\ &\quad + 4 \textstyle\sum_{m,n} [\frac{1}{8} \cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau]\} \\ &= R_{g^2}(\tau) \cdot \textstyle\sum_{m,n} [\cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau \cdot (1 - \frac{1}{2}\delta_{mn})] \end{aligned} \tag{A.32}$$

Therefore, equation (A.18) for case II is:

$$
\begin{aligned}
&R_{IM3}(\tau) \\
&= 9k_3^2 A_{NBI}^2 \tfrac{1}{2} \cos\omega_{NBI}\tau \cdot R_{g^2}(\tau)\{2E_{I_0I_\tau}^W + 2E_{I_0Q_\tau}^W + 4E_{I_0Q_0I_\tau Q_\tau}^W\} \\
&= 9k_3^2 A_{NBI}^2 \tfrac{1}{2} \cos\omega_{NBI}\tau \cdot R_{g^2}(\tau) \cdot \textstyle\sum_{m,n}[\cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau \cdot (1 - \tfrac{1}{2}\delta_{mn})] \\
&= \tfrac{9}{2}k_3^2 A_{NBI}^2 \cos\omega_{NBI}\tau \cdot R_{g^2}(\tau) \cdot \textstyle\sum_{m,n} \cos(2\omega_{WBI} + (n+m)\Delta\omega)\tau \\
&\quad -\tfrac{9}{4}k_3^2 A_{NBI}^2 \cos\omega_{NBI}\tau \cdot R_{g^2}(\tau) \cdot \textstyle\sum_{m} \cos(2\omega_{WBI} + 2m\Delta\omega)\tau \\
&= \tfrac{9}{4}k_3^2 A_{NBI}^2 \cdot R_{g^2}(\tau) \cdot \\
&\textstyle\sum_{m,n}\{\cos(2\omega_{WBI} + \omega_{NBI} + (n+m)\Delta\omega)\tau + \cos(2\omega_{WBI} - \omega_{NBI} + (n+m)\Delta\omega)\tau\} \\
&\quad -\tfrac{9}{8}k_3^2 A_{NBI}^2 \cdot R_{g^2}(\tau) \cdot \\
&\textstyle\sum_{m}\{\cos(2\omega_{WBI} + \omega_{NBI} + 2m\Delta\omega)\tau + \cos(2\omega_{WBI} - \omega_{NBI} + 2m\Delta\omega)\tau\}
\end{aligned}
\tag{A.33}
$$

Only those terms around $(2\omega_{WBI} - \omega_{NBI})$ are of interests, $R_{IM3}(\tau)$ is revised to the following:

$$
\begin{aligned}
&R_{IM3}(\tau) \\
&= \tfrac{9}{4}k_3^2 A_{NBI}^2 \cdot R_{g^2}(\tau) \cdot \ \textstyle\sum_{m,n} \cos(2\omega_{WBI} - \omega_{NBI} + (n+m)\Delta\omega)\tau \\
&\quad -\tfrac{9}{8}k_3^2 A_{NBI}^2 \cdot R_{g^2}(\tau) \cdot \textstyle\sum_{m} \cos(2\omega_{WBI} - \omega_{NBI} + 2m\Delta\omega)\tau
\end{aligned}
\tag{A.34}
$$

Following the same procedure as in case I, we can derive the Fourier transform of $R_{IM3}(\tau)$ in (A.34):

$$
\begin{aligned}
&PSD_{IM3}(f) = \\
&\tfrac{9}{4}k_3^2 A_{NBI}^2 \cdot \sigma_{WBI}^4 \cdot \textstyle\sum_{m=-\frac{N}{2}}^{m=\frac{N}{2}} \sum_{n=-\frac{N}{2}}^{n=\frac{N}{2}} sinc^2((f - (2f_{WBI} - f_{NBI} + (n+m)\Delta f))T) \\
&-\tfrac{9}{8}k_3^2 A_{NBI}^2 \cdot \sigma_{WBI}^4 \cdot \textstyle\sum_{m=-\frac{N}{2}}^{m=\frac{N}{2}} sinc^2((f - (2f_{WBI} - f_{NBI} + 2m\Delta f))T)
\end{aligned}
\tag{A.35}
$$

Again, to improve the computation efficiency, we derived the total number of terms at each frequency $f - (2f_{WBI} - f_{NBI} + l\Delta f)$, $l \in [-N, N]$. A simplified expression

can be derived with an equivalent single summation:

$$\begin{aligned}
&PSD_{IM3}(\omega) \\
&= \tfrac{9}{4}k_3^2 A_{NBI}^2 \sigma_{WBI}^4 \cdot \\
&\{\textstyle\sum_{l=-N}^{N}[(N- \mid l \mid +1)\cdot sinc^2((f-(2f_{WBI}-f_{NBI}+l\Delta f))T)] \\
&-\tfrac{1}{2}\textstyle\sum_{l=-N,-N+2,\ldots}^{N} sinc^2((f-(2f_{WBI}-f_{NBI}+l\Delta f))T)\}
\end{aligned} \tag{A.36}$$

A.2 WBI and WBI

We model the two WBIs as OFDM signals, defined in (3.5):

$$\begin{aligned}
S_1(t) &= I_1(t) + Q_1(t) \\
&= g_T(t+\phi_1)\textstyle\sum_{m=-\frac{N}{2}}^{\frac{N}{2}}[i_m \cos((\omega_{WBI_1}+m\Delta\omega)t+\psi_1) + q_m \sin((\omega_{WBI_1}+m\Delta\omega)t+\psi_1)] \\
S_2(t) &= I_2(t) + Q_2(t) \\
&= g_T(t+\phi_2)\textstyle\sum_{n=-\frac{N}{2}}^{\frac{N}{2}}[i_n \cos((\omega_{WBI_2}+n\Delta\omega)t+\psi_2) + q_n \sin((\omega_{WBI_2}+n\Delta\omega)t+\psi_2)]
\end{aligned} \tag{A.37}$$

When S_1 and S_2 pass through a receiver front-end with nonlinearities, according to (3.1), the third order nonlinear outputs are represented as:

$$S_{3rd}(t) = k_3[S_1(t)+S_2(t)]^3 \tag{A.38}$$

The IMD terms that will fall into the band of interest consist of:

$$S_{IM3}(t) = 3k_3 S_1(t) S_2^2(t) = 3k_3[I_1(t)+Q_1(t)][I_2(t)+Q_2(t)]^2 \tag{A.39}$$

Next, we derive the autocorrelation function.

$$\begin{aligned}
&R_{IM3}(\tau) = E_{\phi,\psi,i,q}\{S_{IM3}(0)S_{IM3}(\tau)\} \\
&= E_{\phi,\psi,i,q}\{3k_3[I_1(0)+Q_1(0)][I_2(0)+Q_2(0)]^2 \cdot 3k_3[I_1(\tau)+Q_1(\tau)][I_2(\tau)+Q_2(\tau)]^2\} \\
&= 9k_3^2 E_{\phi_1,\psi_1,i,q}\{[I_1(0)+Q_1(0)][I_1(\tau)+Q_1(\tau)]\}\cdot \\
&\quad E_{\phi_2,\psi_2,i,q}\{[I_2(0)+Q_2(0)]^2[I_2(\tau)+Q_2(\tau)]^2\}
\end{aligned} \tag{A.40}$$

The first term:

$$
\begin{aligned}
&E_{\phi_1,\psi_1,i,q}\{[I_1(0)+Q_1(0)][I_1(\tau)+Q_1(\tau)]\} \\
&= E_{\phi_1,\psi_1,i,q}\{I_1(0)I_1(\tau)+I_1(0)Q_1(\tau)+Q_1(0)I_1(\tau)+Q_1(0)Q_1(\tau)\} \\
&= E_{\phi_1}\{g_T(\phi_1)g_T(\tau+\phi_1)\}\cdot \\
&\ E_{\psi_1,i,q}\{\textstyle\sum_{m=-\frac{N}{2}}^{\frac{N}{2}}\sum_{n=-\frac{N}{2}}^{\frac{N}{2}} i_m i_n \cos\psi_1\cos((\omega_{WBI_1}+n\Delta\omega)\tau+\psi_1) \\
&\ +\textstyle\sum_{m=-\frac{N}{2}}^{\frac{N}{2}}\sum_{n=-\frac{N}{2}}^{\frac{N}{2}} q_m q_n \sin\psi_1\sin((\omega_{WBI_1}+n\Delta\omega)\tau+\psi_1)\} \\
&= R_g(\tau)\cdot[E_{\psi_1}\{\textstyle\sum_{n=-\frac{N}{2}}^{\frac{N}{2}}[\cos\psi_1\cos((\omega_{WBI_1}+n\Delta\omega)\tau+\psi_1)]\} \\
&\ +E_{\psi_1}\{\textstyle\sum_{n=-\frac{N}{2}}^{\frac{N}{2}}[\sin\psi_1\sin((\omega_{WBI_1}+n\Delta\omega)\tau+\psi_1)]\}] \\
&= R_g(\tau)\cdot[\textstyle\sum_{n=-\frac{N}{2}}^{\frac{N}{2}}\frac{1}{2}\cos((\omega_{WBI_1}+n\Delta\omega)\tau)+\sum_{n=-\frac{N}{2}}^{\frac{N}{2}}\frac{1}{2}\cos((\omega_{WBI_1}+n\Delta\omega)\tau)] \\
&= R_g(\tau)\cdot\textstyle\sum_{n=-\frac{N}{2}}^{\frac{N}{2}}\cos((\omega_{WBI_1}+n\Delta\omega)\tau)
\end{aligned}
\tag{A.41}
$$

The second term:

$$
\begin{aligned}
&E_{\phi_2,\psi_2,i,q}\{[I_2(0)+Q_2(0)]^2[I_2(\tau)+Q_2(\tau)]^2\} \\
&= E_{\phi_2,\psi_2,i,q}\{ \\
&\ I_2^2(0)I_2^2(\tau)+2I_2^2(0)I_2(\tau)Q_2(\tau)+I_2^2(0)Q_2^2(\tau)+ \\
&\ 2I_2(0)Q_2(0)I_2^2(\tau)+4I_2(0)I_2(\tau)Q_2(0)Q_2(\tau)+2I_2(0)Q_2(0)Q_2^2(\tau)+ \\
&\ Q_2^2(0)I_2^2(\tau)+2Q_2^2(0)I_2(\tau)Q_2(\tau)+Q_2^2(0)Q_2^2(\tau)\}
\end{aligned}
\tag{A.42}
$$

According to the property in equation (3.19), terms in the above equation that have odd number of I's or Q's will be 0 after computing the expectation with respect to i and q. Therefore,

$$
\begin{aligned}
&E_{\phi_2,\psi_2,i,q}\{[I_2(0)+Q_2(0)]^2[I_2(\tau)+Q_2(\tau)]^2\} \\
&= E_{\phi_2,\psi_2,i,q}\{I_2^2(0)I_2^2(\tau)+Q_2^2(0)Q_2^2(\tau) \\
&\ \ +I_2^2(0)Q_2^2(\tau)+Q_2^2(0)I_2^2(\tau) \\
&\ \ +4I_2(0)I_2(\tau)Q_2(0)Q_2(\tau)\}
\end{aligned}
\tag{A.43}
$$

This equation has the same format as term (II) of equation (A.7), where term

(II)=(II-A)+(II-B)+(II-C). Therefore, we can use the previous results in (A.18).

$$\begin{aligned}
&E_{\phi_2,\psi_2,i,q}\{[I_2(0)+Q_2(0)]^2[I_2(\tau)+Q_2(\tau)]^2\} \\
&= R_{g^2}(\tau)\{2(E^W_{I_0I_\tau}+E^D_{I_0I_\tau}+E^N_{I_0I_\tau})+2(E^W_{I_0Q_\tau}+E^D_{I_0Q_\tau})+4E^W_{I_0Q_0I_\tau Q_\tau}\}
\end{aligned} \tag{A.44}$$

Since only those terms around $2\omega_{WBI_2}-\omega_{WBI_1}$ are of interests, only components around $2\omega_{WBI_2}$ (i.e. $E^W_{I_0I_\tau}$, $E^W_{I_0Q_\tau}$, $E^W_{I_0Q_0I_\tau Q_\tau}$) will be taken into account. This part has been calculated in equation (A.32).

Plug equations A.41 and A.32 into A.40, $R_{IM3}(\tau)$ is derived as the following:

$$\begin{aligned}
&R_{IM3}(\tau)=E_{\phi,\psi,i,q}\{S_{IM3}(0)S_{IM3}(\tau)\} \\
&=9k_3^2E_{\phi_1,\psi_1,i,q}\{[I_1(0)+Q_1(0)][I_1(\tau)+Q_1(\tau)]\}\cdot \\
&\quad E_{\phi_2,\psi_2,i,q}\{[I_2(0)+Q_2(0)]^2[I_2(\tau)+Q_2(\tau)]^2\} \\
&=9k_3^2R_g(\tau)\cdot\textstyle\sum_{k=-\frac{N}{2}}^{\frac{N}{2}}\cos((\omega_{WBI_1}+k\Delta\omega)\tau)\cdot \\
&R_{g^2}(\tau)\cdot\textstyle\sum_{m,n}[\cos(2\omega_{WBI_2}+(n+m)\Delta\omega)\tau\cdot(1-\frac{1}{2}\delta_{mn})] \\
&=9k_3^2R_g(\tau)R_{g^2}(\tau)\cdot\textstyle\sum_{k=-\frac{N}{2}}^{\frac{N}{2}}\cos((\omega_{WBI_1}+k\Delta\omega)\tau)\cdot\{ \\
&\quad -\tfrac{1}{2}\textstyle\sum_{n=-\frac{N}{2}}^{\frac{N}{2}}\cos((2\omega_{WBI_2}+2n)\Delta\omega)\tau)+ \\
&\quad \textstyle\sum_{m=-\frac{N}{2}}^{\frac{N}{2}}\sum_{n=-\frac{N}{2}}^{\frac{N}{2}}\cos((2\omega_{WBI_2}+(m+n)\Delta\omega)\tau)\} \\
&=9k_3^2R_g(\tau)R_{g^2}(\tau)\cdot\{ \\
&\quad -\tfrac{1}{2}\textstyle\sum_{n=-\frac{N}{2}}^{\frac{N}{2}}\sum_{k=-\frac{N}{2}}^{\frac{N}{2}}\cos((2\omega_{WBI_2}+2n)\Delta\omega)\tau)\cos((\omega_{WBI_1}+k\Delta\omega)\tau)+ \\
&\quad \textstyle\sum_{m=-\frac{N}{2}}^{\frac{N}{2}}\sum_{n=-\frac{N}{2}}^{\frac{N}{2}}\sum_{k=-\frac{N}{2}}^{\frac{N}{2}}\cos((2\omega_{WBI_2}+(m+n)\Delta\omega)\tau)\cos((\omega_{WBI_1}+k\Delta\omega)\tau)\} \\
&=9k_3^2R_g(\tau)R_{g^2}(\tau)\cdot\{ \\
&\quad \tfrac{1}{4}\textstyle\sum_{n=-\frac{N}{2}}^{\frac{N}{2}}\sum_{k=-\frac{N}{2}}^{\frac{N}{2}}\{\cos((2\omega_{WBI_2}+\omega_{WBI_1}+(2n+k))\Delta\omega)\tau)+ \\
&\qquad \cos((2\omega_{WBI_2}-\omega_{WBI_1}+(2n-k))\Delta\omega)\tau)\}+ \\
&\quad \tfrac{1}{2}\textstyle\sum_{m=-\frac{N}{2}}^{\frac{N}{2}}\sum_{n=-\frac{N}{2}}^{\frac{N}{2}}\sum_{k=-\frac{N}{2}}^{\frac{N}{2}}\{\cos((2\omega_{WBI_2}+\omega_{WBI_1}+(m+n+k)\Delta\omega)\tau)+ \\
&\qquad \cos((2\omega_{WBI_2}-\omega_{WBI_1}+(m+n-k)\Delta\omega)\tau)\}\}
\end{aligned} \tag{A.45}$$

Again, we only keep the terms around $(2\omega_{WBI_2} - \omega_{WBI_1})$. The final $R_{IM3}(\tau)$ is

$$\begin{aligned} &R_{IM3}(\tau) = \tfrac{9}{2}k_3^2 R_g(\tau) R_{g^2}(\tau) \cdot \\ &\{\textstyle\sum_{m=-\frac{N}{2}}^{\frac{N}{2}} \sum_{n=-\frac{N}{2}}^{\frac{N}{2}} \sum_{k=-\frac{N}{2}}^{\frac{N}{2}} \cos((2\omega_{WBI_2} - \omega_{WBI_1} + (m+n-k)\Delta\omega)\tau) \\ &-\tfrac{1}{2}\textstyle\sum_{n=-\frac{N}{2}}^{\frac{N}{2}} \sum_{k=-\frac{N}{2}}^{\frac{N}{2}} \cos((2\omega_{WBI_2} - \omega_{WBI_1} + (2n-k))\Delta\omega)\tau)\} \end{aligned} \tag{A.46}$$

Fourier transform:

$$R_g(\tau) = tri(\frac{\tau}{T}) \tag{A.47}$$

$$\mathcal{F}\{R_g(\tau)\} = T \cdot sinc^2(fT) \tag{A.48}$$

$$\mathcal{F}\{R_g(\tau) \cdot R_{g^2}(\tau)\} = T \cdot (sinc^2(fT) * sinc^2(fT)) \tag{A.49}$$

We define a function $S(fT) = sinc^2(fT) * sinc^2(fT)$. Assume the average signal power of WBI_1 is $\sigma^2_{WBI_1}$ and the average signal power of WBI_2 is $\sigma^2_{WBI_2}$. Apply Fourier transform on $R_{IM3}(\tau)$, we derive the $PSD_{IM3}(f)$:

$$\begin{aligned} &PSD_{IM3}(f) = \\ &\tfrac{9}{4}k_3^2 \cdot \sigma^2_{WBI_1}\sigma^4_{WBI_2} T \cdot \{ \\ &\textstyle\sum_{m=-\frac{N}{2}}^{\frac{N}{2}} \sum_{n=-\frac{N}{2}}^{\frac{N}{2}} \sum_{k=-\frac{N}{2}}^{\frac{N}{2}} S((f - (2f_{WBI_2} - f_{WBI_1} + (m+n-k)\Delta f))T) \texttt{--(A)} \\ &-\tfrac{1}{2}\textstyle\sum_{n=-\frac{N}{2}}^{\frac{N}{2}} \sum_{k=-\frac{N}{2}}^{\frac{N}{2}} S((f - (2f_{WBI_2} - f_{WBI_1} + (2n-k))\Delta f)T)\} \texttt{-----(B)} \end{aligned} \tag{A.50}$$

Again, to improve the computation efficiency, we derived the total number of terms (A), Λ_A, at each frequency $f - (2f_{WBI_2} - f_{WBI_1} + l\Delta f)$, $l \in [-\frac{3}{2}N, \frac{3}{2}N]$.

$$\Lambda_A = \begin{cases} \frac{1}{2}(l + \frac{3N}{2} + 1) \cdot (l + \frac{3N}{2} + 2), & -\frac{3N}{2} \le l \le -\frac{N}{2} \\ \frac{1}{2}(6N(l + \frac{3N}{2}) - 2(l + \frac{3N}{2})^2 - 3N^2 + 3N + 2), & \\ & -\frac{N}{2} < l \le \frac{N}{2} \\ \frac{1}{2}(3N - (l + \frac{3N}{2}) + 1)(3N - (l + \frac{3N}{2}) + 2), & \\ & \frac{N}{2} < l \le \frac{3N}{2} \end{cases} \tag{A.51}$$

Finally, the simplified PSD is

$$
\begin{aligned}
&PSD_{IM3}(f) = \\
&\tfrac{9}{4}k_3^2 \cdot \sigma_{WBI_1}^2 \sigma_{WBI_2}^4 T \cdot \{ \\
&\quad \textstyle\sum_{l=-\frac{3N}{2}}^{\frac{3N}{2}} \Lambda_A \cdot S((f - (2f_{WBI_2} - f_{WBI_1} + l\Delta f))T) \\
&\quad -\tfrac{1}{2} \textstyle\sum_{n=-\frac{N}{2}}^{\frac{N}{2}} \sum_{k=-\frac{N}{2}}^{\frac{N}{2}} S((f - (2f_{WBI_2} - f_{WBI_1} + (2n-k))\Delta f)T)\}
\end{aligned}
\tag{A.52}
$$

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