

# 0.35 $\mu\text{m}$ CMOS PROCESS ON SIX-INCH WAFERS, Baseline Report VI.

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# **0.35 $\mu\text{m}$ CMOS PPROCESS ON SIX-INCH WAFERS**

## **Baseline Report VI.**

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October, 2008

### **Abstract**

This report presents details of the fourth six-inch baseline run, CMOS180, where a moderately complex 0.35  $\mu\text{m}$  twin-well, silicided, LOCOS, Mix&Match photo process was implemented. This process was based on the first 0.35  $\mu\text{m}$  six-inch run, CMOS161. Different research circuits (IC/MEMS) were placed in the drop-in area: ring oscillators, a MEMS design, a hyperacuity chip and several different memory circuits.

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## 1. INTRODUCTION

The CMOS baseline test chip fabrication in the Microfabrication Laboratory at the University of California, Berkeley has provided an excellent tool to continuous equipment monitoring of VLSI process modules. This is the sixth baseline report submitted, describing the latest developments in the six-inch CMOS baseline run.

CMOS baseline runs were processed regularly on 4 inch wafers until 2001; then the first six-inch run, CMOS150, successfully transferred the old 1  $\mu\text{m}$  baseline onto six-inch wafers [1]. CMOS150 was followed by a new and more advanced 0.35  $\mu\text{m}$  process, which produced the first sub-half micron devices. CMOS161 not only established our new 0.35  $\mu\text{m}$  process, but also helped in pushing the performance of some of our tools to more advanced processes [2]. In the next baseline run, CMOS170, device parameters were successfully improved by adjusting implantation dose. A triple metal process was implemented to satisfy IC requirements on the test chip [3].

CMOS180 was initiated with the main goal of further improving device performance; as well as introducing shallow trench isolation and Mix&Match process in the lithography steps. This report includes the process flow, parametric test results and motivation behind the latest 0.35  $\mu\text{m}$  six-inch run, CMOS180.

## **2. PROCESS DEVELOPMENT**

A successful Mix&Match process was developed in the CMOS180 run which enabled us to use both 6" steppers in the lithography process. We assigned the critical layers to the DUV ASML (5x reducing) stepper, while non-critical layers were exposed on the standard I-line based GCA WS6 (5x reduction) stepper. The Mix&Match process was applied to a group of 5 wafers in this run.

Shallow trench isolation is a mainstream isolation technique in the sub 0.25  $\mu\text{m}$  technology. To improve electrical parameters we began to develop the shallow trench isolation (STI) process in our current run on 5 wafers. However this process needs further investigation and development in the future; the details of the first attempt are presented in this report.

### **2.1. Mix&Match process in CMOS Baseline**

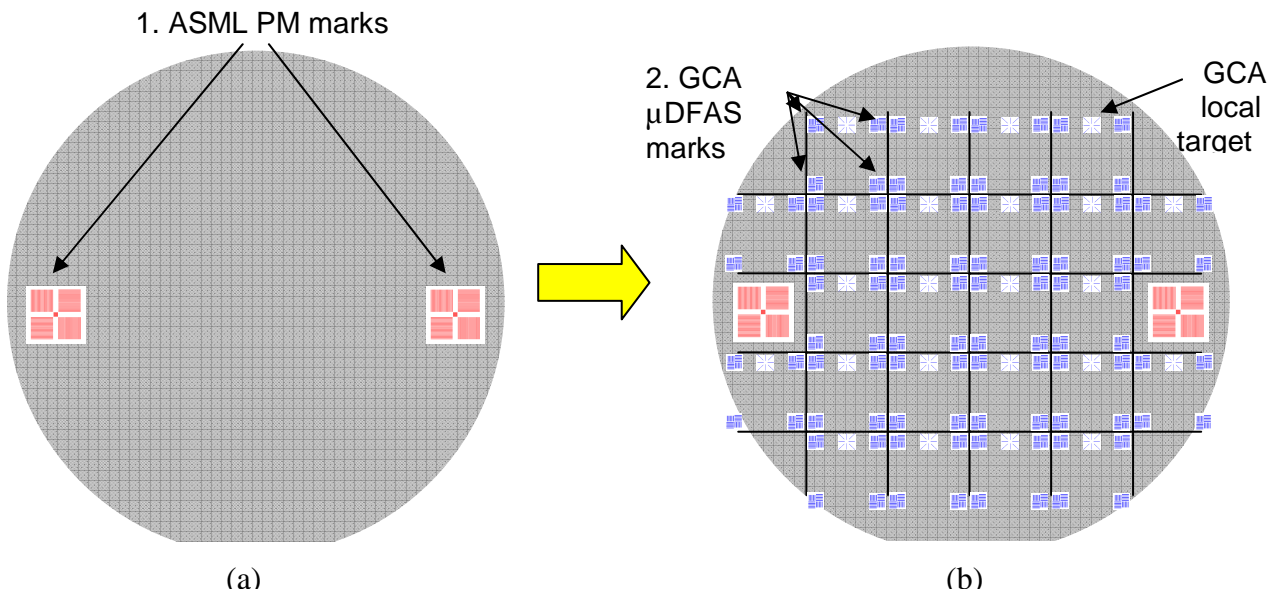
The Mix&Match process incorporated both DUV and I-line lithography, where 11 out of 22 total layers were exposed on the GCA stepper, and the rest on the ASML. The alignment compatibility was established by matching the ASML grid to that of the GCA and by applying a  $-0.5^\circ$  rotation. A second mask (COMBI2) defines the die grid and the GCA alignment marks, with respect to the ASML PM alignment marks. This is done at the first lithography step in the process by the following steps.

1. The Zero layer exposed on ASML stepper defined the PM marks at  $-0.5^\circ$  wafer rotation.
2. ASML PM marks were then etched (Fig. 1.) into the substrate for consequent ASML layer alignment and for printing the Mix&Match zero layer.
3. The Mix&Match zero layer was aligned to the above ASML PM marks. This layer defined the Mix&Match die grid used by both the GCA and ASML steppers and printed the necessary GCA global and  $\mu\text{DFAS}$  (local) alignment targets. These targets printed in every die were used for local alignment by consequent GCA layers. This mask also included some auxiliary structures that made the job of manually locating global alignment targets easier for the GCA stepper layers.

Note: The baseline die size was changed to 10.16 mm x 10.16 mm to accommodate the fixed distance between the two objective lenses of the GCA alignment camera.

- Target coordinates defined by right key offset: (-0.1129, 4.6982)
- dropout dies (2,6) (2,9) (7,2) (7,12) (14,6) (14,9)

4. The Mix&Match Zero layer is then etched into substrate (including the global alignment and  $\mu$ DFAS targets).



**Fig. 1.** ASML PM marks and GCA global alignment/ $\mu$ DFAS targets



## 2.2. STI process and simulation

The STI process was also tried on a group of 5 wafers to eliminate the need for field oxide processing and by isolating active regions on the chip with 1.5  $\mu\text{m}$  wide and 1.5  $\mu\text{m}$  deep trenches. A simulation was performed to study the effect of elimination of the field oxidation step for the STI process. Table 1. below outlines main differences between the standard LOCOS process and the experimental STI process. More information is available in Appendix B on the details of the STI and LOCOS processes

	PMOS		NMOS	
	LOCOS	STI	LOCOS	STI
<b>Well</b>	60keV, $5\text{e}12\text{cm}^{-2}$ , B	<b>20keV, <math>5\text{e}12\text{cm}^{-2}</math>, B</b>	150keV $1\text{e}13\text{cm}^{-2}$ , P	<b>50keV, <math>1\text{e}13\text{cm}^{-2}</math>, P</b>
<b><math>V_t</math></b>	30keV, $2\text{e}12\text{cm}^{-2}$ , P	<b>30keV, <math>2\text{e}12\text{cm}^{-2}</math>, P</b>	50keV, $3\text{e}12\text{cm}^{-2}$ , $\text{BF}_2$	<b>50keV, <math>3.1\text{e}12\text{cm}^{-2}</math>, <math>\text{BF}_2</math></b>

**Table 1.** Parameters of well and  $V_t$  implantation in LOCOS and STI

Wafers were processed together during the N- and P-well formation; followed by the trench fabrication. The STI formation consists of the following steps:

1. Pad oxidation and nitride deposition (Tystar2 and Tystar9). 2200  $\text{\AA}$  thick nitride will act as a hard mask for the trench etch and also a stopping layer for oxide CMP.
2. STI trench lithography on ASML.
3. Trench etch, the target is 1.5  $\mu\text{m}$  (nitride and oxide etch in Centura MxP+, Si trench etch in Lam5 using nitride as the hard mask).
4. Oxide liner growth in Tystar2, the target is 250  $\text{\AA}$ .
5. Dielectric deposition: 2  $\mu\text{m}$  TEOS deposition in P5000.
6. Dielectric planarization with chemical-mechanical polishing.

After the trench fabrication, LOCOS and STI wafers were processed together. From later inspections we found that the cleaning steps in the standard LOCOS process removed most of the TEOS from the trenches. This created a large pit around the active area. The height difference between the active area and the isolation area was so large that the thin poly gate lines

could not be resolved in the poly lithography step over the isolations. The next process flow should be modified in order to protect the trench area.

### 3. CMOS BASELINE FABRICATION PROCESS

A moderately more complex and improved Mix&Match version of the initial 0.35  $\mu\text{m}$  process (CMOS161 run) was used for the new baseline run. This included a triple metal process that utilized chemical-mechanical polishing (CMP) on all of the inter-metal dielectric layers. The new Mix&Match process enabled assigning the non-critical layers to the standard I-line stepper.

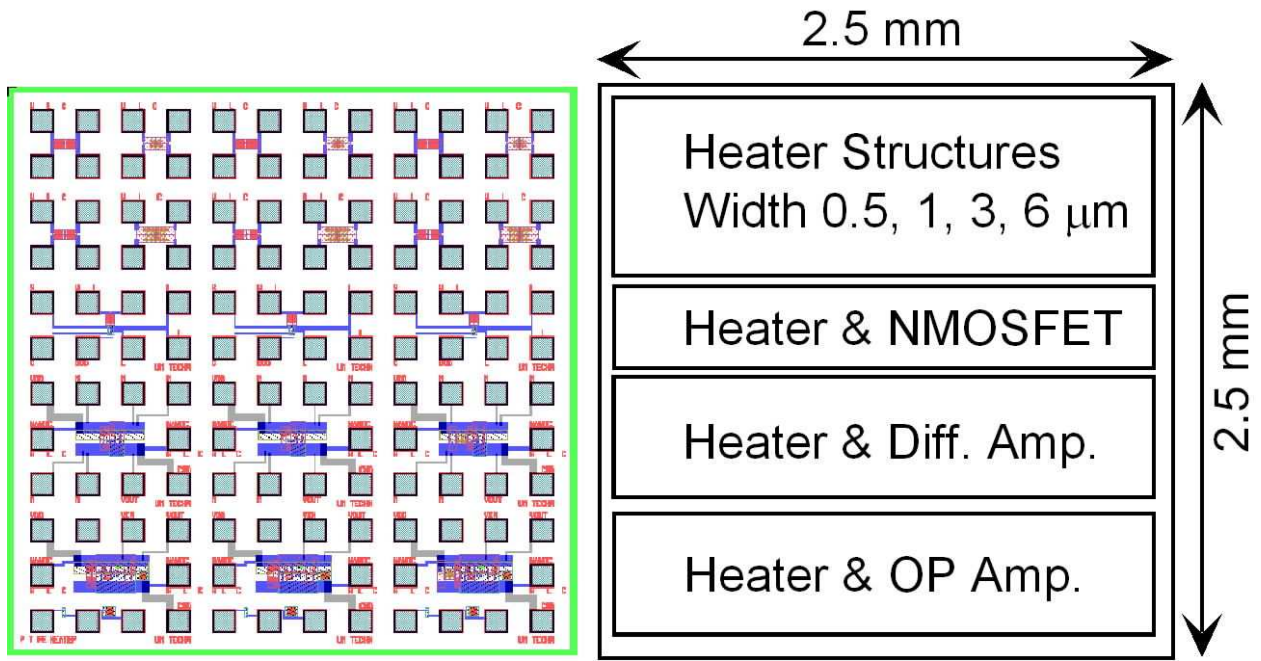
#### 3.1. CMOS180 chip layout

The CMOS180 chip layout – besides the standard groups of baseline transistor sets – includes test structures (contact resistors, contact chains, contact holes, poly lines), basic test circuits (NOR and NAND gates), a MEMS structure, and a hyperacuity circuit from the previous run.

The **single transistor section** of the die consists of three groups differentiated by their design rules. Each column is based on a 5x3 array of PMOS and NMOS transistors, which are varying in channel length ( $L = 0.3, 0.35, 0.4, 0.5$ , and  $1 \mu\text{m}$ ) and channel width ( $W = 2.5, 5$ , and  $7.5 \mu\text{m}$ ). The first column on the left side used a more robust design rule basically following the old transistor layout; which had been tested and proven by the CMOS160 run. This design was scaled down by 2 in CMOS170 and remained as is in the current run. These transistors do not follow any specific industrial layout design rules; their gates are reduced while their contacts, active areas, metal lines, etc. are kept within safe processing limits. This report focuses on this group of transistors

On the second and third groups a more aggressive lambda scale design approach was applied. The column 2 transistors in the middle received Hewlett Packard's (HP)  $\lambda=0.5 \mu\text{m}$  design rules, while transistors on the third column followed the HP design rules for  $\lambda=0.35 \mu\text{m}$ .

A new circuit was added in the drop-in area to verify the integration feasibility of **locally synthesized carbon nanotubes (CNTs) with CMOS circuitry**.



**Fig. 2.** CMOS amplifiers for CNT growth structures

There are three major types of design units included in the above design: basic CNT growth structures, CNT growth structures with one-stage CMOS amplifiers and CNT growth structures with two stage CMOS amplifiers. Critical dimensions, such as the gap between two CNT growth units and the amplifier ratio are varied in the design to investigate their effect. After the CMOS run is finished, some MEMS post-processing steps are required to finish the device.

The **hyperacuity die** is a Time-to-Digital Converter (TDC), which performs an Analog to Digital (A/D) Conversion. The circuit receives rising edge transitions on two input pins, and the timing order and amount of delay between these two signals is coded into a binary number resulting in a much higher resolution (time converted in space) and accuracy in time. A 25 picosecond time resolution can be realized, which in a conventional circuit would be operating in the nanosecond range designed for our 0.35  $\mu\text{m}$  process. More details on the design are available in [3] and [5].

The **MEMS** structure included in the layout is an electrostatic mono-directional in-plane displacement microactuator [6]. The device enables a direct evaluation of Young's modulus in a variety of thin film materials (SiC, SiGe, and poly-Si are examples of the materials that may be evaluated).

### 3.2. CMOS180 Baseline Fabrication Process

The Mix&Match version of the 0.35  $\mu\text{m}$  process consists of 68 steps including the triple metal module. This is needed for the fabrication of more complex circuitry and test dies on the CMOS180 test chip. N-channel and P-channel MOSFET devices, as well as some simple circuits were tested at step 54, post the Metall1 etch/sinter step; all yielding well with functional devices.

Table 2. lists the process steps used for the triple metal version of the 0.35  $\mu\text{m}$  baseline run. The starting material for the process were P-type 6" double polished wafers with the following parameters:  $\langle 100 \rangle$  orientation, 20-60  $\Omega\text{-cm}$  resistivity,  $635 \pm 25$   $\mu\text{m}$  thickness, total thickness variation  $< 7$   $\mu\text{m}$ . This process utilizes thin gate oxide, lightly doped drain structure, PECVD oxide sidewall spacers, titanium silicide S/D, and poly work function engineering. A 0.25  $\mu\text{m}$  thick layer of undoped polysilicon material was deposited, then patterned and etched to form the poly gate electrode structures. These poly gates were then selectively implanted to have their work function adjusted and matched for desired  $V_t$  values, based on earlier computer simulation results. This was achieved by exposing the N- and P- channel transistors' gate electrode during their respective source/drain implant steps (N S/D and P S/D masks were modified to allow this). CMP and PECVD TEOS inter-metal dielectric was also used for the triple metal version of the 0.35  $\mu\text{m}$  process. This version is fully supported by CMOS180 ASML and GCAWS6 mask sets.

For etching the Metall1 layer in Step 52, the recently installed Centura metal chamber was used instead of Lam3 on three of the process wafers. Endpoint was working properly for aluminum; while passivation had to be made separately. Wafers yielded equally after the different etch processes.

Appendix A shows the test chip and an ASML mask plate layout.

Appendix B and C contain the detailed process flow for the LOCOS and STI trench processes.

Step 0. Starting wafers	Step 35. P-type LDD implant
Step 1. Initial oxidation	Step 36. N-type LDD implant photo
Step 2. Zero layer photo	Step 37. N-type LDD implant
Step 3. Scribe wafers	Step 38. LDD spacer deposition
Step 4.. Zero layer etch	Step 39. LDD spacer etch
Step 5. Mix&Match Zero layer photo	Step 40. P+ gate and S/D photo
Step 6. Mix&Match Zero layer etch	Step 41. P+ gate and S/D implant
Step 7. Pad oxidation/nitride deposition	Step 42. N+ gate and S/D photo
Step 8. N-well photo	Step 43. N+ gate and S/D implant
Step 9. Nitride etch	Step 44. Backside etch
Step 10. N-well implant	Step 45. Gate and S/D annealing
Step 11. Nitride removal	Step 46. Silicide formation
Step 12. Pad oxidation/nitride deposition	Step 47. PSG dep. and densification
Step 13. P-well photo	Step 48. Contact photo
Step 14. Nitride etch	Step 49. Contact etch
Step 15. P-well implant	Step 50. Metal 1 deposition
Step 16. Nitride removal	Step 51. Metal 1 photo
Step 17. Well drive in	Step 52. Metal 1 etch
Step 18. Pad oxidation/nitride deposition	Step 53. Sintering
Step 19. Active area photo	Step 54. Testing
Step 20. Nitride etch	Step 55. Dielectric deposition/planarization
Step 21. P-well field implant photo	Step 56. Via 1 Photo
Step 22. P-well field ion implant	Step 57. Via 1 Etch
Step 23. LOCOS oxidation	Step 58. Metal 2 deposition
Step 24. Nitride and pad oxide removal	Step 59. Metal 2 photo
Step 25. Sacrificial oxidation	Step 60. Metal 2 etch
Step 26. Screen oxidation	Step 61. Testing
Step 27. NMOS Vt adjust. implant photo	Step 62. Dielectric deposition/planarization
Step 28. NMOS Vt adjustment implant	Step 63. Via 2 photo
Step 29. PMOS Vt adjust. implant photo	Step 64. Via 2 etch
Step 30. PMOS Vt adjustment implant	Step 65. Metal 3 deposition
Step 31. Gate oxidation, poly-Si dep.	Step 66. Metal 3 photo
Step 32. Gate photo	Step 67. Metal 3 etch
Step 33. Poly-Si etch	Step 68. Testing
Step 34. P-type LDD implant photo	

**Table 2.** Process steps of the CMOS180 baseline run

The CMOS180 process included 22 lithography steps. Some masks were used on two layers, which brought the total number of masks down to 16, including the zero layer and the Mix&Match zero layer masks. In the Mix&Match process we have shown that 10 lithography steps can be done on the GCA I-line stepper using 4 masks. All the lithography steps were done by  $-0.5^\circ$  wafer rotation to provide alignment condition for the GCA stepper in the Mix&Match process.

Table 3. lists all the lithography steps used for the fabrication of CMOS180, as well as the corresponding mask ID and the hard bake methods used for these lithography steps. All steps were done on the DUV 248 nm ASML stepper. As indicated, BARC (Bottom Anti-Reflective Coating, ARC-600 type) layer was applied at several lithography steps.

Step	Resist	Mask	Hard bake
Zero layer photo	Shipley UV-210-0.6 9000 Å	Zero layer mask PM marks	UVBake, program U
Mix&Match Zero layer photo	Shipley UV-210-0.6 9000 Å	GCA alignment mark for Mix&Match	UVBake, program U
N-well photo	Shipley UV-210-0.6 9000 Å W#1-10 OiR 897- 10i 12000 Å W#11-15	NWELL mask (Dark field)	UVBake, program J
P-well photo	Shipley UV-210-0.6 9000 Å W#1-10 OiR 897- 10i 12000 Å W#11-15	PWELL mask (Clear field)	UVBake, program J
Active area photo	Shipley UV-210-0.6 9000 Å	ACTIVE mask (Clear field)	UVBake, program J
P-well field implant photo	Shipley UV-210-0.6 9000 Å	PFIELD mask (Clear field)	UVBake, program J
NMOS Vt adj. implant photo	Shipley UV-210-0.6 9000 Å W#1-10 OiR 897- 10i 12000 Å W#11-15	PWELL mask (Clear field)	UVBake, program J
PMOS Vt adj. implant photo	Shipley UV-210-0.6 9000 Å W#1-10 OiR 897- 10i 12000 Å W#11-15	NWELL mask (Dark field)	UVBake, program J
Poly gate photo	Shipley UV-210-0.6 9000 Å + ARC-600	POLY mask (Clear field)	UVBake, program U
P-type LDD implant photo	Shipley UV-210-0.6 9000 Å W#1-10 OiR 897- 10i 12000 Å W#11-15	PSELECT mask (Dark filed)	UVBake, program J
N-type LDD implant photo	Shipley UV-210-0.6 9000 Å W#1-10 OiR 897- 10i 12000 Å W#11-15	NSELECT mask (Dark field)	UVBake, program J
P+ Gate & S/D photo	Shipley UV-210-0.6 9000 Å W#1-10 OiR 897- 10i 12000 Å W#11-15	PSELECT mask (Dark filed)	UVBake, program J

N+ Gate & S/D photo	Shipley UV-210-0.6 9000 Å W#1-10 OiR 897- 10i 12000 Å W#11-15	NSELECT mask (Dark field)	UVBake, program J
Contact photo	Shipley UV-210-0.6 9000 Å + ARC-600	CONTACT mask (Dark field)	UVBake, program U
New PM marks	Shipley UV-210-0.6 9000 Å	Zero layer mask PM marks	UVBake, Program U
Metal1 photo	Shipley UV-210-0.6 9000 Å + ARC-600	METAL1 mask (Clear field)	UVBake, program U
Via1 photo	Shipley UV-210-0.6 9000 Å	VIA1 mask (Dark field)	UVBAKE program U
Opening 4 dies for PM marks	Shipley UV-210-0.6 9000 Å W#1-10 OiR 897- 10i 12000 Å W#11-15	Blank mask	UVBake, Program U
Metal2 photo	Shipley UV-210-0.6 9000 Å + ARC-600	METAL2 mask (Clear field)	UVBake, program U
Via2 photo	Shipley UV-210-0.6 9000 Å	VIA2 mask (Dark field)	UVBake, program U
Opening 4 dies for PM marks	Shipley UV-210-0.6 9000 Å W#1-10 OiR 897- 10i 12000 Å W#11-15	Blank mask	UVBake, Program U
Metal3 photo	Shipley UV-210-0.6 9000 Å + ARC-600	METAL3 mask (Clear field)	UVBake, program U

**Table 3.** Lithography steps and related information

The CMOS180 process required 9 ion implantations, all of which were performed at Core Systems (Sunnyvale, CA). The list of the implantation steps, including implant parameters and blocking materials are shown in Table 3. All of the implant steps were done at standard 7° tilt. Wafers designated as PCH and NCH were used as in line test monitors.

Table 5. contains the list of tools used for the fabrication of the CMOS180 run.

Detailed tool information is available at:

<http://microlab.berkeley.edu/labmanual/Labmanualindex.html>

Step	Species	Dose (cm <sup>-2</sup> )	Energy (KeV)	Wafers	Masking materials
N-well implant	Phosphorus	1E13	150 50	#1-5 and #11-15, PCH for LOCOS #6-10 for STI	220 nm Si <sub>3</sub> N <sub>4</sub> + PR (UVBake)
P-well implant	Boron	5E12	60 20	#1-5 and #11-15, NCH for LOCOS #6-10 for STI	220 nm Si <sub>3</sub> N <sub>4</sub> + PR (UVBake)
P-well field imp.	Boron	2E13	80	#1-5 and #11-15 for LOCOS	Pad oxide + PR (UVBake)
NMOS Vt imp.	BF2	3E12 3.1E12	50	#1-5 & #11-15, NCH for LOCOS #6-10 for STI	Pad oxide + PR (UVBake)
PMOS Vt imp.	Phosphorus	2E12	30	#1-15, PCH	Pad oxide + PR (UVBake)
P-type LDD imp.	BF2 BF2	5E13 5E13	10, +7° 10, -7°	#1-15, PCH, Tpoly1	PR (UVBake)
N-type LDD imp.	Arsenic Arsenic	5E13 5E13	30, +7° 30, -7°	#1-15, NCH, Tpoly2	PR (UVBake)
P+ Gate & S/D imp.	Boron	3E15	20	#1-15, PCH, Tpoly1	PR (UVBake)
N+ Gate & S/D imp.	Phosphorus	3E15	40	#1-15, NCH, Tpoly2	PR (UVBake)

**Table 4.** List of implantation steps and parameters

Process module	Equipment	Process step
Lithography	ASML 5500/90 DUV stepper GCA 8500 I-line stepper	Listed in Table 2.
	SVGCoat6	PR/BARC spinning
	SVGDev6	PR develop
	Matrix	PR removal
	Technics-C	PR removal/descum
	UVBake	PR hardbake



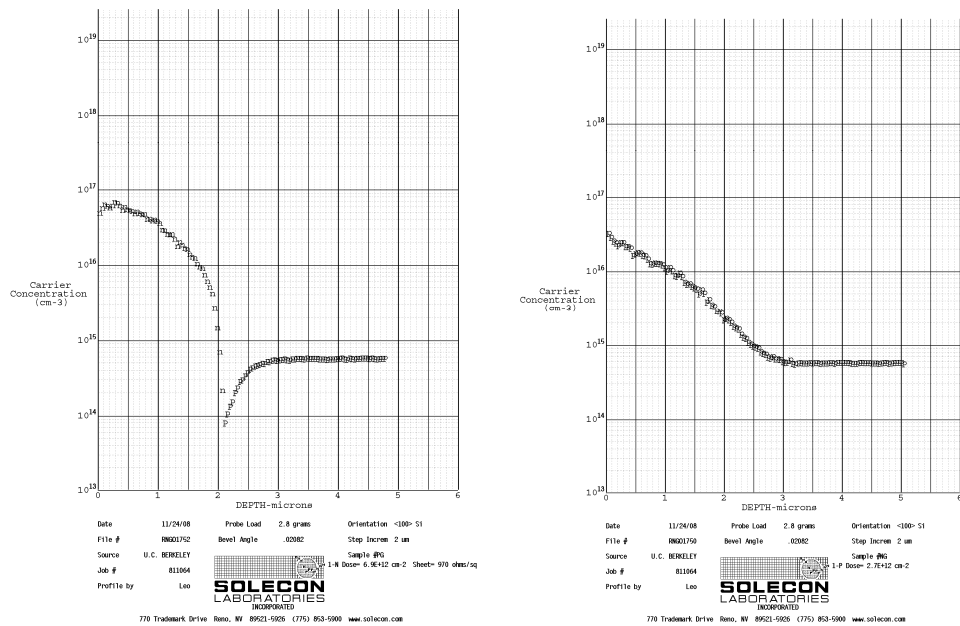
Plasma etch	AMAT Centura-MxP+	Nitride etch
		Oxide etch
		Oxide spacer etch
	AMAT Centura metal	Aluminum etch
	Lam 3	Aluminum etch
	Lam 5	Poly-Si etch
High temperature treatment	Tystar 1	Wet/dry oxidation
	Tystar 2	
	Tystar18	Sintering
	Heatpulse 3 (RTP)	Annealing
	Heatpulse 4 (RTP)	Silicidation
CVD	Applied P-5000 (PECVD)	Oxide spacer deposition
	Tystar 9 (LPCVD)	Nitride deposition
	Tystar 10 (LPCVD)	Poly-Si deposition
	Tystar 11 (LPCVD)	PSG deposition
Thin film systems	Novellus	Ti deposition
		Al deposition
Wet etch/Cleaning	Sink 6	Pre-furnace piranha clean
		HF dip (10:1, 25:1)
		Rinse (QDR)
	Sink 7	Hot phosphoric etch
		Titanium wet etch
		Rinse (QDR)
	Sink 8	Post-lithography piranha clean
		HF dip (5:1)
		Rinse (QDR)
Measurement	ASIQ	Surface profiling
	Nanospec	Dielectric thickness
	Leo	SEM
	4pt probe	Sheet resistance
	Autoprobe	Electrical parameters
	Sopra	Ellipsometry
Planarization	CMP	Mechanical polishing

**Table 5.** Process tool set

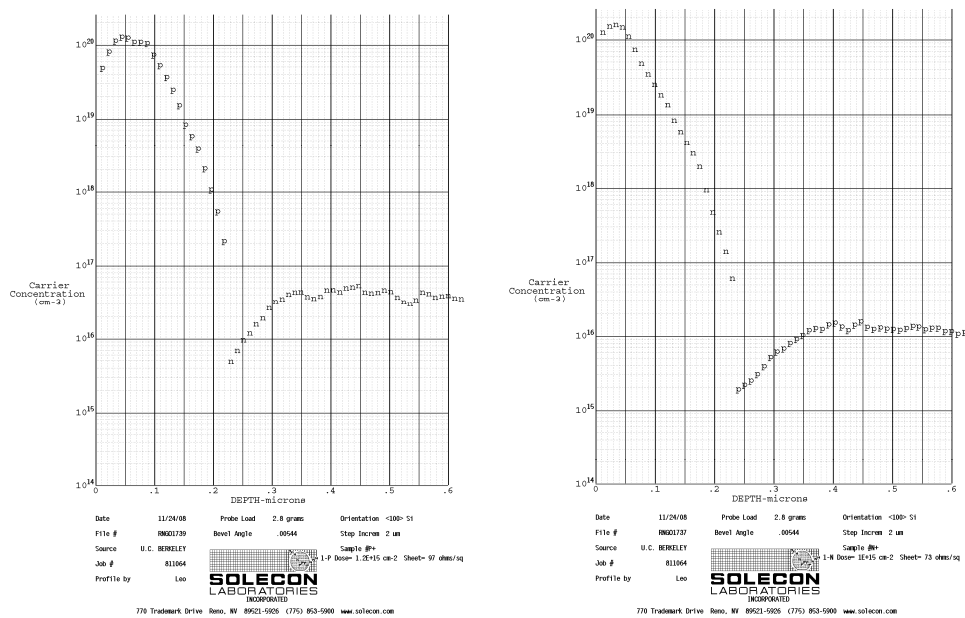
## 4. MEASUREMENT RESULTS OF CMOS180

### 4.1 Spreading Resistance Analysis (SRA)

The Spreading Resistance Analysis was carried out by Solecon Laboratories Inc. (Reno, NV). Graphical presentation of the measurement results, carrier concentration vs. implant depth profile are shown on Fig. 3. and 4.



**Fig. 3.** P-channel (left) and N-channel (right) doping profile under gate oxide

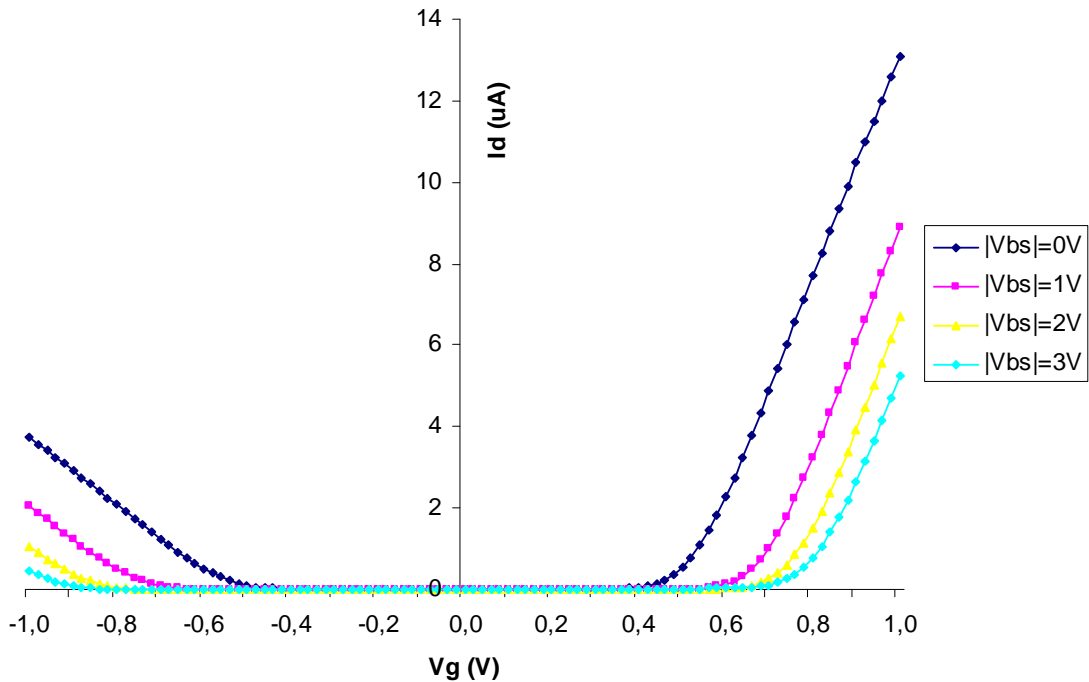


**Fig. 4.** P+ source-drain (left) and N+ source-drain (right) doping profile

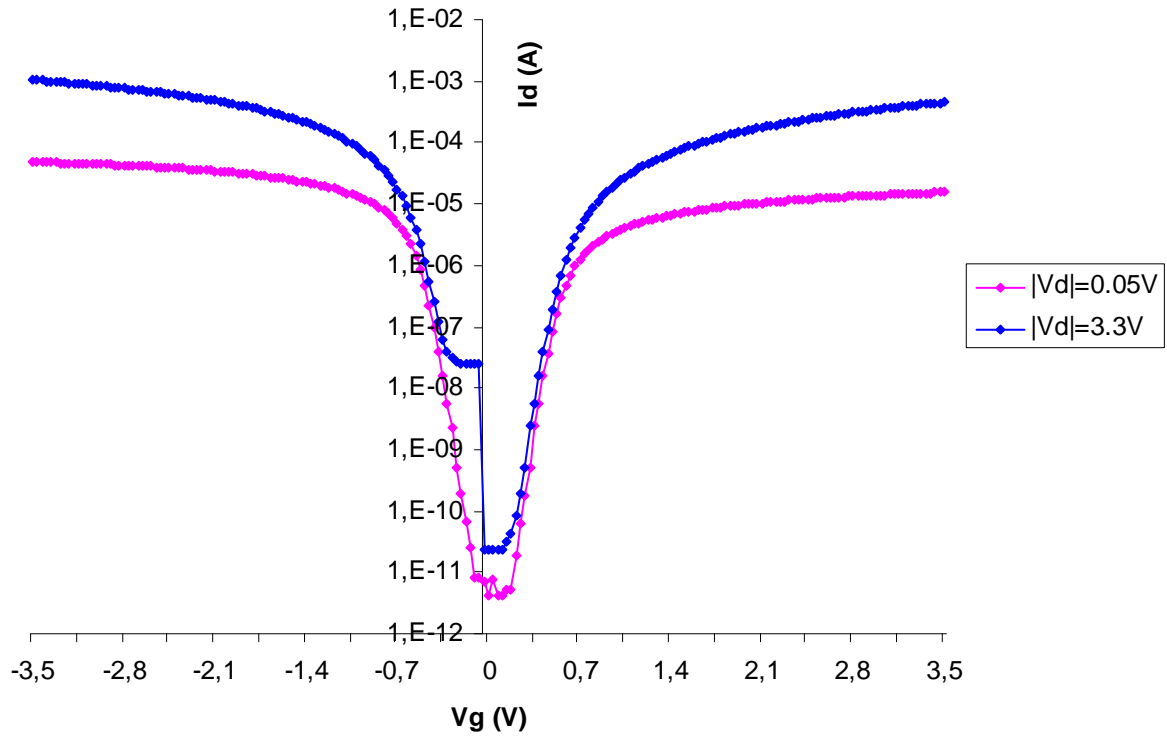
## 4.2. Electrical measurements

Electrical measurements were obtained using an automated test system (Autoprobe). The HP4062A Semiconductor Parametric Test System utilizes an HP4085A Switching Matrix, an HP4084B Switching Matrix Controller and an Agilent4142B Modular DC Source/Monitor Unit. The system is connected to a Model 2001X Electroglas probe station, which is controlled by a Metrics I/CV software running on a PC workstation. All the test structures and transistors were configured with proper pad array on the chip that would support a 2 x 5 pin probe card (10 tips). Test structure layout was set up this way to allow fast and accurate collection of a large amount of data on device parameters, and other process monitoring related items. The PC based Metrics software, which includes measurement modules, was used for parametric testing [4], [8].

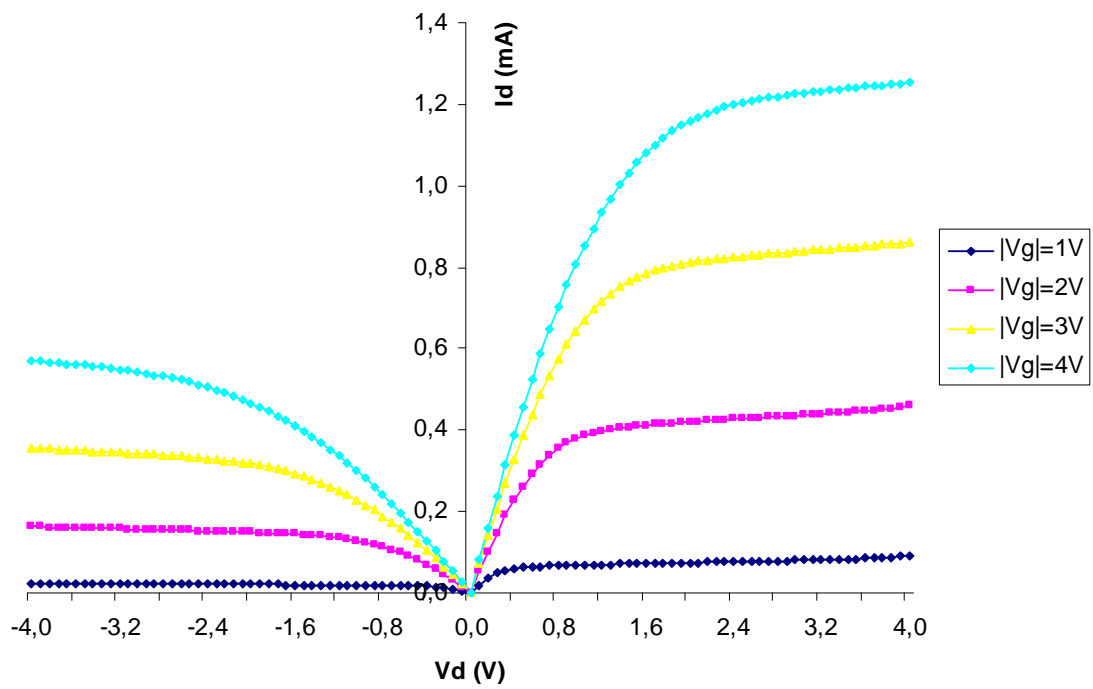
*I-V results* – The following graphs show typical I-V characteristics of the CMOS180 transistors, which were measured on 0.3  $\mu\text{m}$  drawn channel length and 2.5  $\mu\text{m}$  width transistors. Fig. 5. and Fig. 6. demonstrate  $I_d$ - $V_g$ , Fig. 7. shows  $I_d$ - $V_d$  curves.



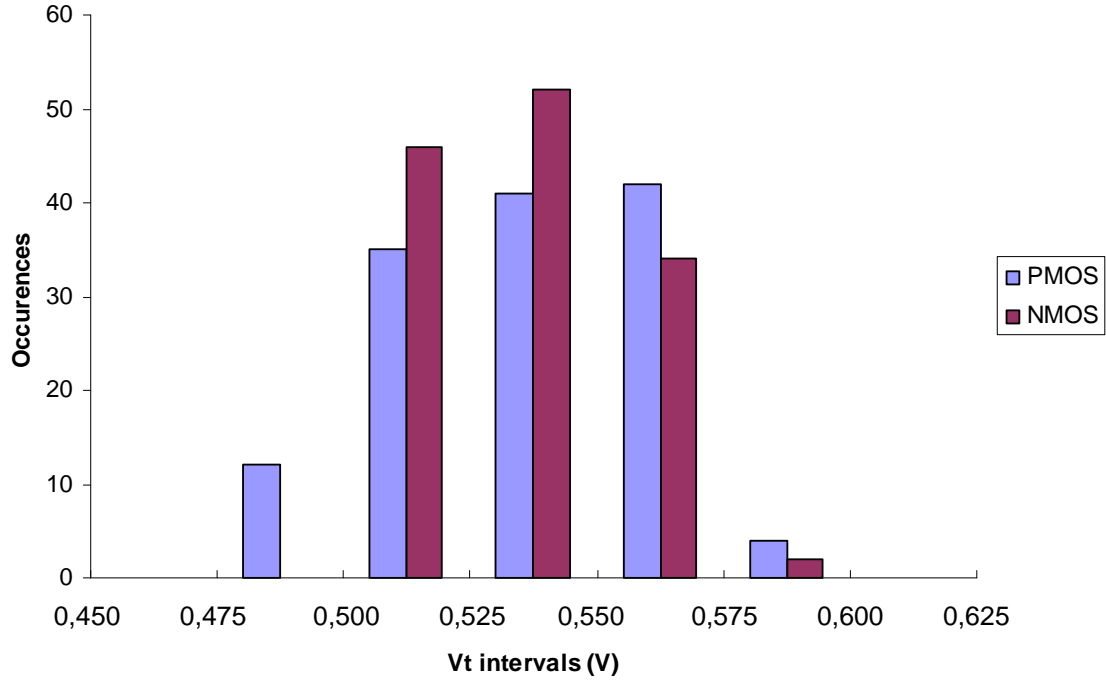
**Fig. 5.** Drain current vs. gate voltage at varying substrate bias on PMOS and NMOS transistors in the linear region ( $V_d = 50\text{mV}$ )



**Fig. 6.** PMOS and NMOS sub-threshold characteristics



**Fig. 7.** Drain current vs. drain voltage characteristics of PMOS and NMOS devices



**Fig. 8.**  $V_t$  targeting for 2.5/0.3  $\mu\text{m}$  devices

### *Ring oscillators*

After completion of the second metal layer deposition, ring oscillators were tested. Various types and gate length ring oscillators are available on the test chip; 0.35  $\mu\text{m}$ , 0.5  $\mu\text{m}$ , 1  $\mu\text{m}$  and 2  $\mu\text{m}$  gate length conventional; as well as 0.6  $\mu\text{m}$  and 1.2  $\mu\text{m}$  gate length voltage controlled ring oscillators (VCO). Each device consists of 31 stages. The average oscillation frequency was measured to be 12.5 MHz on the standard 1.2  $\mu\text{m}$  VCOs. The gate delay time using the  $t_d$  equation below was calculated to be 1.29 ns.

$$t_d = 1 / ( 2 * n_s * f_{osc} )$$

where  $n_s$  is the number of stages (31) and  $f_{osc}$  is the oscillation frequency (12.5 MHz).

## 5. PROCESS AND DEVICE PARAMETERS

Table 6. shows the summary of various measurements and test results of the CMOS180 process. Values shown in this table were extracted from measurements on  $L=0.3\ \mu\text{m}$ ,  $W=2.5\ \mu\text{m}$  devices.

No.	Parameter	Unit	NMOS	PMOS
1	$V_t$	V	0.54	-0.55
2	Sub Threshold Slope	mV/decade	79	85
3	$K (\mu C_{ox})$	$\mu\text{A}/\text{V}^2$	74	69
4	$\gamma_1 ( V_{sb} =1\text{V})$	$\text{V}^{1/2}$	0.18	-0.14
5	$\gamma_2 ( V_{sb} =3\text{V})$	$\text{V}^{1/2}$	0.15	-0.13
6	Surface dopant concentration	$\text{Atom}/\text{cm}^3$	$3\text{E}+16$	$6\text{E}+16$
7	Substrate dopant concentration	$\text{Atom}/\text{cm}^3$	$0.5\text{E}+16$	$4\text{E}+16$
8	$T_{ox}$ (Gate)	nm	7.7	7.7
9	$X_j$ (S-D depth)	$\mu\text{m}$	0.24	0.23
10	$X_w$ (Well depth)	$\mu\text{m}$	3.0	2.2
11	$R_{diff}$ (Sheet resistance, S-D)	$\Omega/\text{square}$	52	64
12	$R_{poly}$ (Sheet resistance, Gate)	$\Omega/\text{square}$	129	211
13	$R_c$ M1-diff	$\Omega$	1.15	0.92
14	S-D breakdown	V	$>9.5$	$>8$
15	S-D leakage ( $V_{ds}=3.3\text{V}$ , $V_{gs}=0\text{V}$ )	$1/\mu\text{m}$	320 pA	18 nA
16	Eff. mobility ( $V_{bs}=0\text{V}$ , $V_{gs}=1\text{V}$ )	$\text{cm}^2/\text{Vsec}$	194	57
17	Ring oscillator frequency (31 stages, $1.2\ \mu\text{m}$ , $3.3\text{V}$ VCO)	MHz	12.5	

**Table 6.** Process and device parameters of CMOS180 ( $W=2.5\ \mu\text{m}$  and  $L=0.3\ \mu\text{m}$ )

*Methods, measurement conditions, and explanations for obtaining the parameters in Table 6.*

1. Threshold voltages were measured by the autoprobe V<sub>t</sub> module using the linear extrapolation method [8].

2. Sub-threshold slope values are hand calculated based on the autoprobe DIBLE module (log (I<sub>d</sub>) vs. V<sub>g</sub>). Using the autoprobe's DIBL module a log (I<sub>d</sub>) vs. V<sub>g</sub> graph was plotted when the device was operating in the linear region: V<sub>d</sub>=|50 mV|. By picking a decade of I<sub>d</sub> change on the Y scale the corresponding V<sub>g</sub> difference was read from the X scale.

3. K values (gain factor in the linear region) were obtained by hand calculation based on the autoprobe I<sub>d</sub>-V<sub>g</sub> measurements when devices were operating in the linear region. Using the V<sub>t</sub> module on the autoprobe, I<sub>d</sub> vs. V<sub>g</sub> and G<sub>m</sub> vs. V<sub>g</sub> curves were plotted simultaneously (V<sub>d</sub>=|50 mV|). The I<sub>d</sub> and the corresponding V<sub>g</sub> values were picked where G<sub>m</sub> maximized. Using the equations

$$K = \mu C_{ox}$$

and

$$I_{ds} = \mu C_{ox} W/L (V_{gs} - V_{th} - V_{ds} / 2) V_{ds}$$

values were substituted and K was extracted.

4-5.  $\gamma_1$  and  $\gamma_2$  (body effect parameters at different body biases) were obtained by hand calculation based on the autoprobe V<sub>t</sub> measurements at different body biases. Using the V<sub>t</sub> module on the autoprobe, threshold voltage values were defined under different body bias conditions (|V<sub>bs</sub>| = 0 V, 1 V, 3 V). Using

$$V_t = V_{to} + \gamma ((|2\Phi_B| + |V_{sb}|)^{1/2} - (|2\Phi_B|)^{1/2})$$

and

$$\Phi_B = kT/q \ln (N_{well}/n_i)$$

$\gamma$  was extracted for |V<sub>bs</sub>| = 1 V, 3 V values.

6-7. Surface dopant concentration numbers are based on the SRA results (Fig. 3. and Fig. 4.).

8. Gate oxide thickness was measured by the Sopra ellipsometer during processing.

9-10. Well depth and the source-drain depth data arise from the SRA graphs (Fig. 3. and Fig. 4.).

11-12. Sheet resistance values were obtained by four-point-probe measurements during processing.

13. Contact resistances were measured on designated test structures by the autoprobe CONTR\_SCB module.

14. S-D breakdown measurements were taken using the autoprobe.

15. S-D leakage values were calculated based on the graphs given by autoprobe DIBLE module. Using the  $\log(I_d)$  vs.  $V_g$  graph, the value of  $I_d$  was read at  $V_g = 0$  V point on the  $V_{ds} = 3.3$  V curve.

16.  $\mu_{eff}$  (effective mobility) data came from autoprobe measurements using the EFFMOB module. Measurement values were modified to reflect actual  $C_{ox}$  value. The originally measured value with the autoprobe's EFFMOB module was multiplied by the factor of 1.23. This ratio was found between the "ideal"  $C_{ox}$  value (for  $t_{ox} = 80$  Å) and the lower  $C_{ox}$  value that C-V measurement showed in inversion (for " $t_{ox}$ " =  $t_{ox}$  + partially depleted poly gate thickness). The factor of 1.23 multiplication was applied because  $C_{ox}$  is in the nominator in the  $\mu_{eff}$  equation:

$$\mu_{eff} = g_d / C_{ox} (W/L) (V_g - V_{to})$$

17. Ring oscillator frequency was calculated using the autoprobe RingOsc module.



## 6. FUTURE WORK

This run will be repeated as CMOS191 to serve as a starting point and to ensure proper equipment functionality in the new Marvell Nanofabrication Laboratory. Two splits will be made for the LOCOS and the STI processes, as the Mix&Match process is considered successful. The LOCOS process will remain as-is, while modifications will be applied to the shallow trench isolation process flow to enable proper device functionality.

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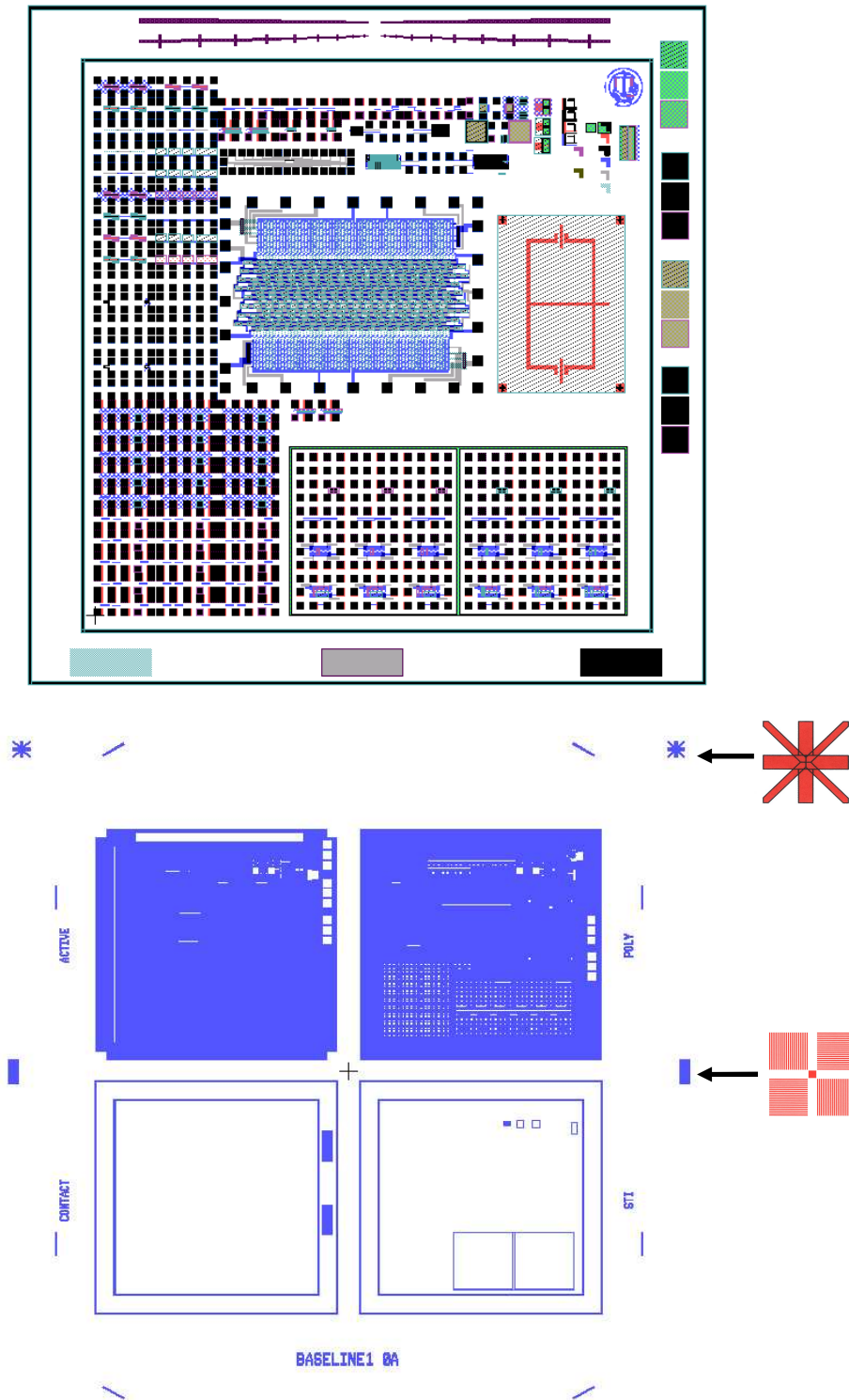
## **Biographies**

**Laszlo Petho** earned his M.S. degree in Engineering Physics in 2007 from the Technical University of Budapest, Hungary. Laszlo has been working as a baseline process engineer in the UC Berkeley Microfabrication Laboratory since November 2007. His main tasks include CMOS device fabrication and testing, training and equipment characterization.

**Anita Pongracz** earned her M.S. degree in Engineering Physics in 2004 from the Technical University of Budapest, Hungary. Anita was working as a baseline process engineer in the UC Berkeley Microfabrication Laboratory from August 2006 to December 2007. Her main responsibilities were to design, fabricate, test, and evaluate CMOS test devices.

# Appendix A

## Baseline test chip layout



**Figure 9.** Baseline chip layout (top) and four mask quadrants on one ASML reticle (bottom)

## Appendix B

### CMOS Baseline 180 process flow Mix&Match with LOCOS

Step Nr.	Process step	Substeps	Equipment / recipe	Target and process specification	Notes
0	<b>STARTING WAFERS</b>		20-60 $\Omega$ -cm, p-type, <100>, 6"		2 monitor wafers (PCH, NCH)
1	<b>INITIAL OXIDATION</b>	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	
		b) Standard cleaning	Sink 6	Piranha + 25:1 HF until dewets	
		c) Dry oxidation	Tystar2, 2DRYXA	Target: 250 A 950C, 30 min; 20 min N2 annealing	
2	<b>ZERO LAYER PHOTO</b>		ASML	COMBI mask UVBAKE pr. J	Defines ASML alignment PM marks
3	<b>SCRIBE WAFERS</b>		Diamond pen	Scribe numbers into the photoresist	
4	<b>ZERO LAYER ETCH</b>	a) Etch through oxide	Centura-MxP+, recipe: MXP_OXSP_ETCH	250 A etch	
		b) Etch PM marks	Lam5, recipe: 5003	1200 A etch	
		c) Photoresist strip	Matrix	2.5 min O2 ash	
		d) Measure etch depth	ASIQ		
		d) Standard cleaning	Sink8		
5	<b>MIX&amp;MATCH ZERO LAYER PHOTO</b>		ASML	COMBI2 mask UVBAKE pr. J	Defines GCA alignment marks
6	<b>MIX&amp;MATCH ZERO LAYER ETCH</b>	a) Etch through oxide	Centura-MxP+, recipe: MXP_OXSP_ETCH	250 A etch	
		b) Etch PM marks	Lam5 recipe: 5003	1200 A etch	
		c) Photoresist strip	Matrix	2.5 min O2 ash	
		d) Measure etch depth	ASIQ		
7	<b>PAD OXIDATION / NITRIDE DEPOSITION</b>	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	
		b) Standard cleaning	Sink8 + Sink 6	Piranha + 25:1 HF until dewets	Include NCH, PCH
		c) Dry oxidation	Tystar2, 2DRYXA	Target: 250 A 1000C, 21 min; 15 min N2 annealing	
		d) Nitride deposition	Tystar9, 9SNITA	Target: 2200A	
8	<b>N-WELL PHOTO</b>		ASML, GCAWS6	Mask: NWELL UVBAKE program J	
9	<b>NITRIDE ETCH</b>		Centura-MxP+, recipe: MXP_NITRIDE_OE	Monitor endpoint	

10	<b>N-WELL IMPLANT</b>		CORE Systems	Specie/Dose/Energy: P, 1E13, 150 keV	Include PCH
11	<b>NITRIDE REMOVAL</b>	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8	Piranha	
		c) Nitride wet etch	Sink7	160C fresh phosphoric acid ~4 hours	
		d) Pad oxide wet etch	Sink8	5:1 BHF until dewets	Include PCH, NCH
12	<b>PAD OXIDATION / NITRIDE DEPOSITION</b>	a) TLC clean	Tystar2, 2TLCA	2 hrs of cleaning	
		b) Standard cleaning	Sink8 + Sink 6	Piranha + 25:1 HF until dewets	Include NCH, PCH
		c) Dry oxidation	Tystar2, 2DRYOSA	Target: 250 A 1000C, 21 min; 15 min N2 annealing	
		d) Nitride deposition	Tystar9, 9SNITA	Target: 2200 A	
13	<b>P-WELL PHOTO</b>		ASML, GCAWS6	Mask: PWELL UVBAKE pr. J	
14	<b>NITRIDE ETCH</b>		Centura MxP+, recipe: MXP_NITRIDE_OE	Monitor endpoint	
15	<b>P-WELL IMPLANT</b>		CORE Systems	Specie/Dose/Energy: B, 5E12, 60keV	Include NCH
16	<b>NITRIDE REMOVAL</b>	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8	Piranha	
		c) Nitride wet etch	Sink7	160C fresh phosphoric acid ~4 hours	
		d) Pad oxide wet etch	Sink8	5:1 BHF until dewets	Include PCH, NCH
17	<b>WELL DRIVE-IN</b>	a) TLC clean	Tystar2, 2TLCA	2 hrs of cleaning	
		b) Standard cleaning	Sink8 + Sink 6	Piranha + 25:1 HF until dewets	Include NCH, PCH
		c) Well drive-in	Tystar2, 2WELLD	1100C, 150 min; 15 min N2 annealing	
		d) Oxide wet etch	Sink8	5:1 BHF until dewet	
18	<b>PAD OXIDATION / NITRIDE DEPOSITION</b>	a) TLC clean	Tystar2, 2TLCA	2 hrs of cleaning	
		b) Standard cleaning	Sink8 + Sink 6	Piranha + 25:1 HF until dewets	Include NCH, PCH
		c) Dry oxidation	Tystar2, 2DRYOSA	Target: 250 A 1000C, 21 min; 15 min N2 annealing	
		d) Nitride deposition	Tystar9, 9SNITA	Target: 200 A	Include PCH only
19	<b>ACTIVE AREA PHOTO</b>		ASML	ACTIVE mask UVBAKE pr U	Use BARC if needed

20	<b>NITRIDE ETCH</b>		Centura MxP+, recipe: MXP_NITRIDE_OE	Monitor endpoint, allow some over etch	
21	<b>P-WELL FIELD IMPLANT PHOTO</b>	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8	Piranha	
		c) Lithography	ASML	Mask: PFIELD UVBAKE pr. J	
22	<b>P-WELL FIELD IMPLANT</b>		CORE Systems	Specie/Dose/Energy: B, 2E13, 80keV	
23	<b>LOCOS OXIDATION</b>	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	
		b) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8 + Sink 6	Piranha + 10 sec dip in 25:1 HF	Include NCH, PCH
		d) Wet oxidation	Tystar2, 2WETOXA	Target: 5500 A 1000C, 120 min; 20 min N2 annealing	
24	<b>NITRIDE REMOVAL / PAD OXIDE REMOVAL</b>	a) Oxide wet etch	Sink 6	10:1 HF for 60 sec	Include PCH
		b) Nitride wet etch	Sink 7	160C fresh phosphoric acid ~4 hours	
		c) Oxide wet etch	Sink 6	10:1 HF for 60 sec until PCH dewets	Etch pad oxide
		d) Oxide wet etch on NCH	Sink7	Fresh 5:1 BHF until dewets	
25	<b>SACRIFICIAL OXIDATION</b>	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	
		b) Standard cleaning	Sink 6	Piranha + 10 sec dip into 25:1 HF	Include NCH, PCH
		c) Dry oxidation	Tystar2, 2DRYOSA	Target: 250 A 900C, 40 min; 1 sec (meaning zero) N2 annealing	
26	<b>SCREEN OXIDATION</b>	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	
		b) Standard cleaning	Sink 6	Piranha + 25:1 HF dip until NCH, PCH dewet	Include NCH, PCH
		c) Dry oxidation	Tystar2, 2DRYOSA	Target: 250 A 900C, 40 min; 15 min N2 annealing	
27	<b>NMOS Vt IMPLANT PHOTO</b>		ASML, GCAWS6	Mask: PWELLUVBAKE program J	
28	<b>NMOS Vt IMPLANT</b>		CORE Systems	Specie/Dose/Energy: BF2, 3E12, 50keV	Include NCH
29	<b>PMOS Vt IMPLANT PHOTO</b>	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8	Piranha	
		c) Lithography	ASML	Mask: NWELL UVBAKE program J	

30	<b>PMOS Vt IMPLANT</b>		CORE Systems	Specie/Dose/Energy: P, 2E12, 30keV	Include PCH
31	<b>GATE OXIDATION / POLY DEPOSITION</b>	a) TLC clean	Tystar1, 1TLCA	2 hours of cleaning	
		b) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8 + Sink 6	Piranha + dip in 25:1 HF until NCH, PCH dewet	Include NCH, PCH, Tox, Tpoly1, Tpoly2
		c) Gate oxidation	Tystar1, 1THIN-OX	Target: 80 A 850C, 30 min oxidation; 900C, 30 min N2 anneal	Include NCH, PCH, Tox, Tpoly1, Tpoly2
		d) Poly-Si deposition	Tystar10, 10SUPLYA	Target: 2500 A Dep. Time: ~ 28 min	Include Tpoly1, Tpoly2
		e) Measurements	Sopra, Rudolph	Measure oxide thickness on Tox	
			SCA	Measure Dit, Qox, Nsc, Ts on Tox	
			Nanospec		
			4PTRB	Strip oxide from NCH and PCH; measure Rs	
32	<b>POLY GATE PHOTO</b>		ASML	Mask: POLY UVBAKE program U	Use BARC if needed, GCA 2nd uDFAS marks included in poly mask
33	<b>POLY-Si ETCH</b>	a) Poly etch	Lam5, recipe 5003	Monitor endpoint, ~50% over etch	
		b) Photoresist strip	Matrix	2.5 min O2 ash	
		c) Standard cleaning	Sink7 + Sink 8	100:1 HF dip to remove polymers formed in Lam5, Piranha	
		d) Measure channel length with SEM	Leo	Check Poly-Si lines with SEM	
34	<b>PMOS LDD IMPLANT PHOTO</b>		ASML, GCAWS6	Mask: PSELECT UVBAKE program J	
	<b>PMOS LDD IMPLANT</b>		CORE Systems	Specie/Dose/Energy: BF2, 5E13, 10keV, +7° tilt @ 0 orientation; BF2, 5E13, 10keV, -7° tilt @ 180 orientation	Include PCH, Tpoly1
36	<b>NMOS LDD IMPLANT PHOTO</b>	a) Photoresist strip	Matrix	Std. 2.5 min O2 ash	
		b) Standard cleaning	Sink8	Piranha	
			ASML	Mask: NSELECT UVBAKE pr. J	
37	<b>NMOS LDD IMPLANT</b>		CORE Systems	Specie/Dose/Energy: As, 5E13, 30keV, +7° tilt @ 0 orientation; As, 5E13, 30keV, -7° tilt @ 180 orientation	Include NCH, Tpoly2
38	<b>LDD SPACER DEPOSITION</b>	a) Photoresist strip	Matrix	2.5 min O2 ash	

		b) Standard cleaning	Sink8 + Sink 6	Piranha	
		c) TEOS deposition	P-5000; recipe AH-USG	Target: 4000 A; Dep. rate: ~80 A/sec	
		d) Annealing	Tystar2; 2HIN2ANA	900C, 30 min	
		e) Measurement	Nanospec		
39	<b>LDD SPACER FORMATION</b>		Centura MxP+, recipe: MXP_OXSP_ET_EP	Monitor endpoint, stop etch when drops	
40	<b>P+ GATE &amp; S/D PHOTO</b>		ASML	Mask: PSELECTUVBAKE program J	
41	<b>P+ GATE &amp; S/D IMPLANT</b>		CORE Systems	Specie/Dose/Energy: B, 3E15, 20keV	Include PCH, Tpoly1
42	<b>N+ GATE &amp; S/D PHOTO</b>	a) Photoresist strip	Matrix	Std. 2.5 min O2 ash	
		b) Standard cleaning	Sink8	Piranha	
		c) Lithography	ASML	Std. litho Mask: NSELECT UVBAKE pr. J	
43	<b>N+ GATE &amp; S/D IMPLANT</b>		CORE Systems	Specie/Dose/Energy: P, 3E15, 40keV	Include NCH, Tpoly2
44	<b>BACK SIDE ETCH</b>	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8	Piranha	
		c) Coat wafers	SVGCOAT6	UVBAKE pr. J	
		d) Oxide wet etch	Sink8	5:1 BHF until backside dewets	
		e) Poly-Si etch	Lam5 recipe 5003	No overetch step	Etch to endpoint plus 10 sec
		f) Oxide wet etch	Sink8	5:1 BHF until backside dewet	Include NCH, PCH, Tpoly1, Tpoly2
45	<b>GATE &amp; S/D ANNEALING</b>	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8 + Sink 6	Piranha	Include NCH, PCH, Tpoly1, Tpoly2
		c) RTA annealing	Heatpulse3, recipe 1050RTA6.RCP	450C 30 sec, 900C 10 sec, 1050C 5 sec	Device chamber
		d) Measurement	4PTRB	Measure Rs on NCH, PCH, Tpoly1, Tpoly2	For gate <250 Ohm/sq, for S/D <100 Ohm/sq
46	<b>SILICIDATION</b>	a) Sputter etch	Novellus, recipe ETCHSTD	1 min etch	
		b) Ti deposition	Novellus, recipe TI300STD	25 sec deposition	
		c) RTA annealing	Heatpulse3, recipe 650RTA6.RCP	450C 20sec, 650C 15sec	Silicide chamber, N2 atmosphere
		d) Wet etch Ti & TiN	Sink7	Remove unreacted Ti and TiN in fresh piranha	



47	PSG DEPOSITION & DENSIFICATION	a) Standard cleaning	Sink 6	Piranha (NO HF dip)	Include PCH, Si and TiSi test wafers
		b) PSG deposition	Tystar11, recipe 11SDLTOA	Target: 7000 A ~45 min, 450C	
		c) Coat wafers	SVGCOAT6	UVBAKE pr. J	
		d) Oxide wet etch	Sink8	5:1 BHF until backside dewet	
		e) Photoresist strip	Matrix	2.5 min O2 ash	
		f) Standard cleaning	Sink8+Sink6	Piranha	
		g) RTA annealing	Heatpulse3, recipe 900RTA6.RCP	450C 30 sec, 900C 10 sec	Silicide chamber, N2 atmosphere
		h) Measurement	Nanospec		
			4PTPRB		
48	CONTACT PHOTO	a) Litho	ASML	Mask: CONT	Overexpose contact (30-40 mJ/cm2)
		b) Litho	ASML	Second exposure Mask: COMBI UVBAKE pr. U	2nd PM marks should be exposed before developing
49	CONTACT ETCH	a) Contact etch	Centura-MxP+, recipe: MXP_OXSP_ET_EP	Monitor endpoint, allow 15 sec overetch after signal drops	Etching through BARC takes ~50-60 sec.
		b) Measurement	Manual probe		
50	METAL 1 DEPOSITION	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8 + Sink 6	Piranha, NO HF	
		c) Sputter etch	Novellus, recipe: ETCHSTD	1 min etch	
		d) Al deposition	Novellus: Ti liner (TI300STD) Al/2%Si (AL6KGV)	Target: 6000 A	
		e) Measure Rs	4ptprb		
51	METAL1 PHOTO		ASML	BARC litho, Mask: METAL1 UVBAKE pr. U	GCA 3rd uDFAS included
52	METAL1 ETCH	a) Al etch	Lam3, Standard recipe	allow 50% overetch	No need to etch BARC separately
		b) Measurement	Manual probe		
53	SINTERING	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Rinse	Sink8	Rinse and spin dry, no piranha or HF	
		c) Sintering	Tystar18, recipe: H2SINT4A.018	20 min, 400C	
54	TESTING		Autoprobe	Test devices with 1 metal layer	Vt, IdVd, Isat, EffMob, Body effect

55	<b>DIELECTRIC DEPOSITION &amp; PLANARIZATION</b>	a) TEOS deposition	P-5000, recipe: AP-USG2	Target: 2µm; Dep. rate: ~80 Å/sec	
		b) Planarization	CMP, recipe: oxide_st00	1 µm removal	
56	<b>VIA1 PHOTO</b>	a) Rinse wafers	Sink8	Rinse and spin dry, no piranha or HF	Dehydrate wafers in 120C oven for 30 min
		b) Lithography	ASML	Mask: VIA1 UVBAKE pr. U	
57	<b>VIA1 ETCH</b>	a) Oxide etch	Centura-MxP+, recipe: MXP_OXSP_ET_EP	Monitor endpoint, allow 15 sec overetch after signal drops	
		b) Measurement	Manual probe		
58	<b>METAL 2 DEPOSITION</b>	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Sputter etch	Novellus, recipe ETCHSTD	1 min etch	
		c) Al deposition	Novellus, Std. Al process	Target: 9000 Å	
59	<b>METAL2 PHOTO</b>	a) Opening PM marks	ASML	Mask: blank UVBAKE pr. U	
		b) Etch Al from 4 dies	Lam3		
		c) Resist removal	Matrix	2.5 min O2 ash	SVC-14 at 80C for 10 min for dense structures
		d) Metal2 lithography	ASML	BARC litho, Mask: METAL2 UVBAKE pr. U	
60	<b>METAL2 ETCH</b>	a) Al etch	Lam3, Standard recipe	allow 50% overetch	
		b) Measurement	Manual probe		
		c) Resist removal	Matrix	2.5 min O2 ash	
61	<b>TESTING</b>		Probe station	Test devices with 2 metal layers	M1-M2 contact resistors and chains, ring oscillators
62	<b>DIELECTRIC DEPOSITION &amp; PLANARIZATION</b>	a) TEOS deposition	P-5000, recipe: AP-USG2	Target: 2 µm	
		b) Planarization	CMP, recipe: oxide_st00	1 µm removal	
63	<b>VIA2 PHOTO</b>	a) Rinse wafers	Sink8	Rinse and spin dry, no piranha or HF	
		b) Lithography	ASML	Mask: VIA2 UVBAKE pr. U	
64	<b>VIA2 ETCH</b>	a) Oxide etch	Centura-MxP+, recipe: MXP_OXSP_ET_EP		
		b) Measurement	Manual probe		
65	<b>METAL 3 DEPOSITION</b>	a) Photoresist strip	Matrix	2 min O2 ash	
		b) Sputter etch	Novellus, recipe ETCHSTD	1 min etch	

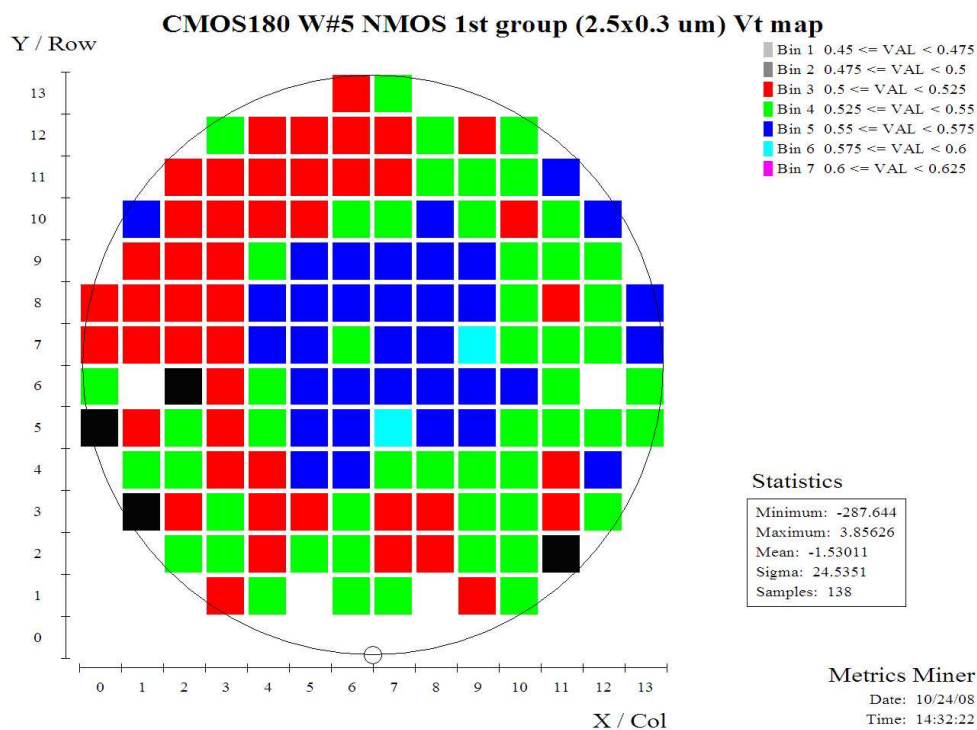
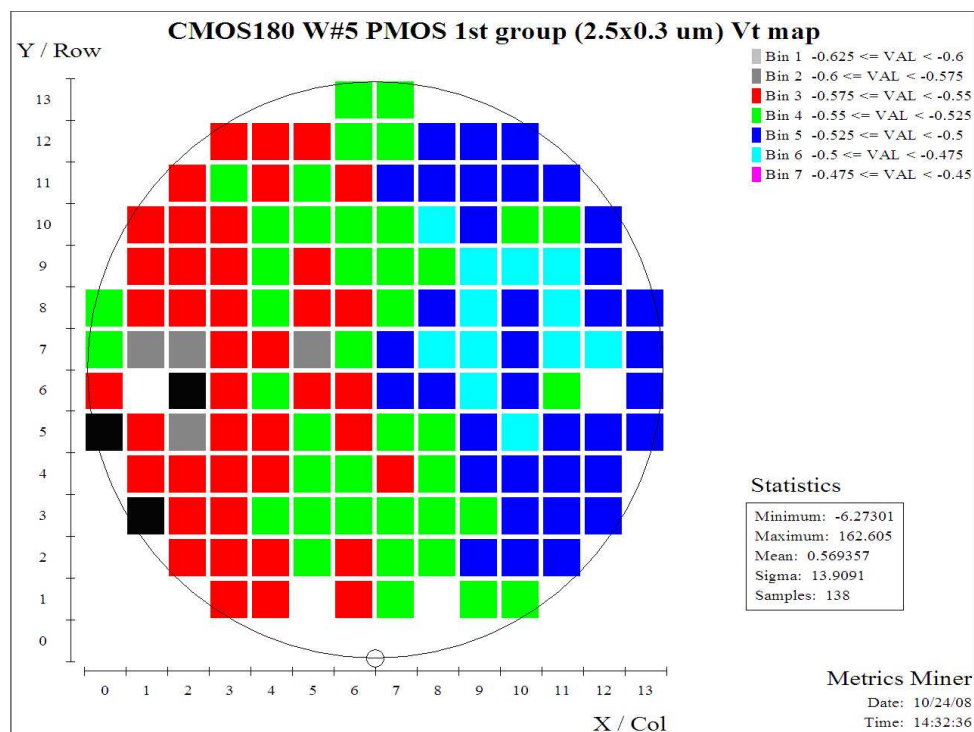
		c) Al deposition	Novellus, Std. Al process	Target: 9000 Å	
66	<b>METAL3 PHOTO</b>	a) Opening PM marks	ASML	Mask: blank UVBAKE pr. U	
		b) Etch Al from 4 dies	Lam3		
		c) Resist removal	Matrix	2.5 min O2 ash	SVC-14 at 80C for 10 min for dense structures
		d) Metal2 lithography	ASML	BARC litho, Mask: METAL3 UVBAKE pr. U	
67	<b>METAL3 ETCH</b>	a) Al etch	Lam3, Standard recipe	allow 50% overetch	
		b) Measurement	Manual probe		
68	<b>TESTING</b>		Probe station	Test devices with 3 metal layers	M2-M3 contact resistors and chains

**CMOS Baseline 180 process flow split for  
Shallow trench isolation (STI)**

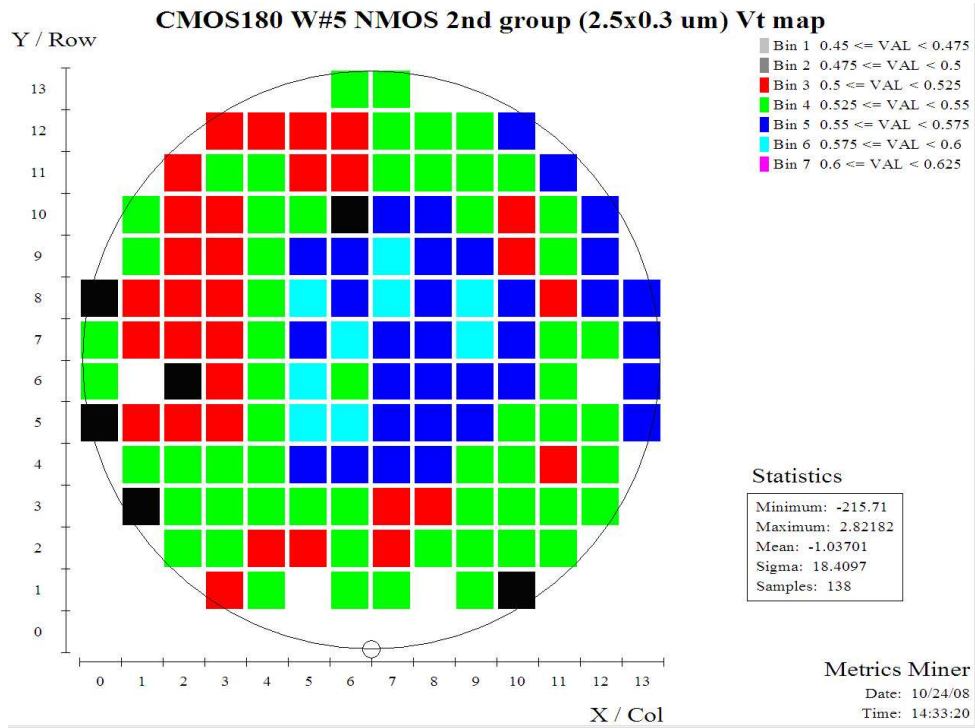
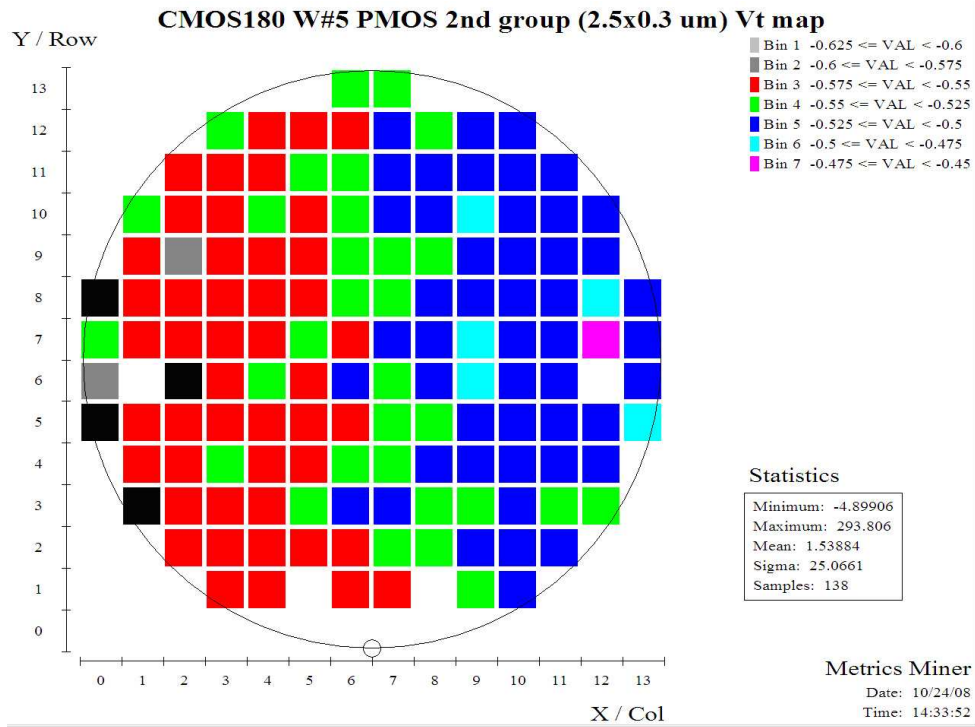
19	<b>STI PHOTO</b>		ASML	STI mask UVBAKE pr. U	Use BARC if needed
20	<b>TRENCH ETCH</b>	a) Nitride etch	Centura MxP+, recipe: MXP_NITRIDE_OE	Monitor endpoint, allow some over etch	
		b) Oxide etch	Centura MxP+, recipe: MXP_OXSP_ETCH		
		c) Si etch	Lam5 recipe 5003 no overetch	Target: 1.5 µm	
21	<b>OXIDE LINER GROWTH</b>	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	
		c) Standard cleaning	Sink8 + Sink 6	Piranha + 25:1 HF until dewets	Include NCH, PCH
		d) Dry oxidation	Tystar2, 2DRYXA	Target: 250 Å 1000C, 21 min; 15 min N2 annealing	
22	<b>DIELECTRIC DEPOSITION</b>		P-5000, recipe: AP-USG2	Target: 2 µm	
23	<b>DIELECTRIC PLANARIZATION</b>	a) Planarization	CMP, recipe: oxide_st00	Target: 2 µm removal	Change CMP head
		b) Cleaning	Sink CMP + Sink8	DI water	

## Appendix C

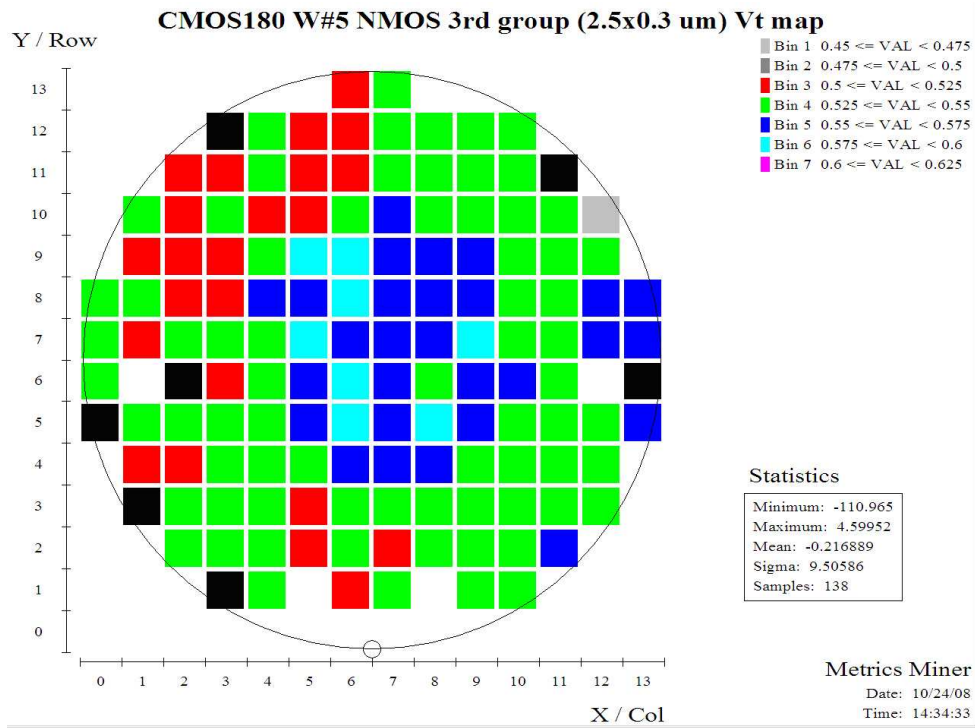
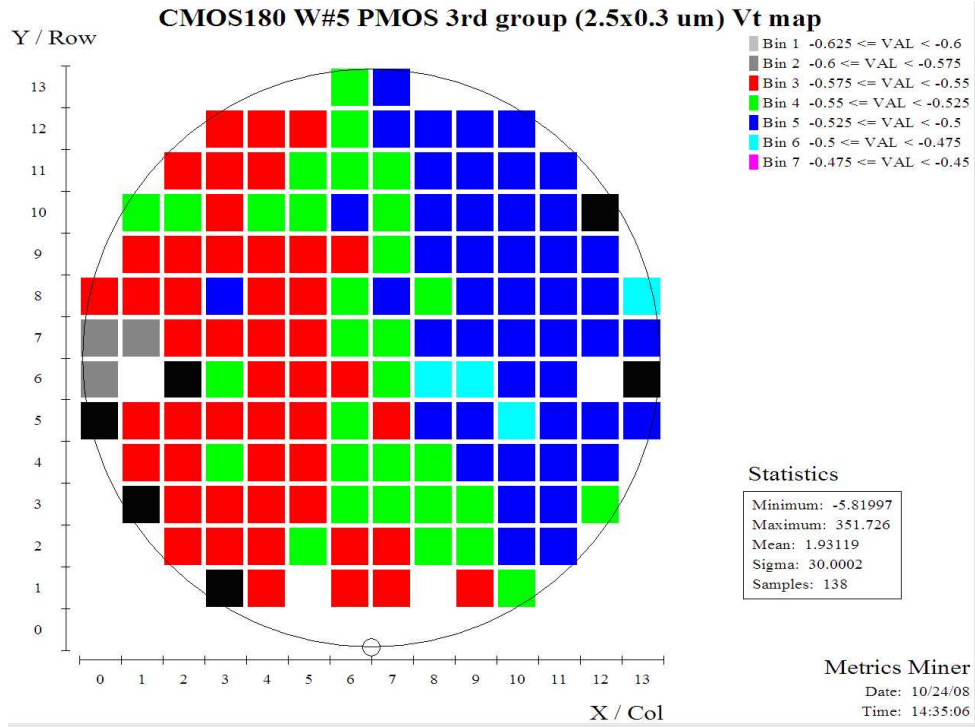
### Threshold voltage distribution maps



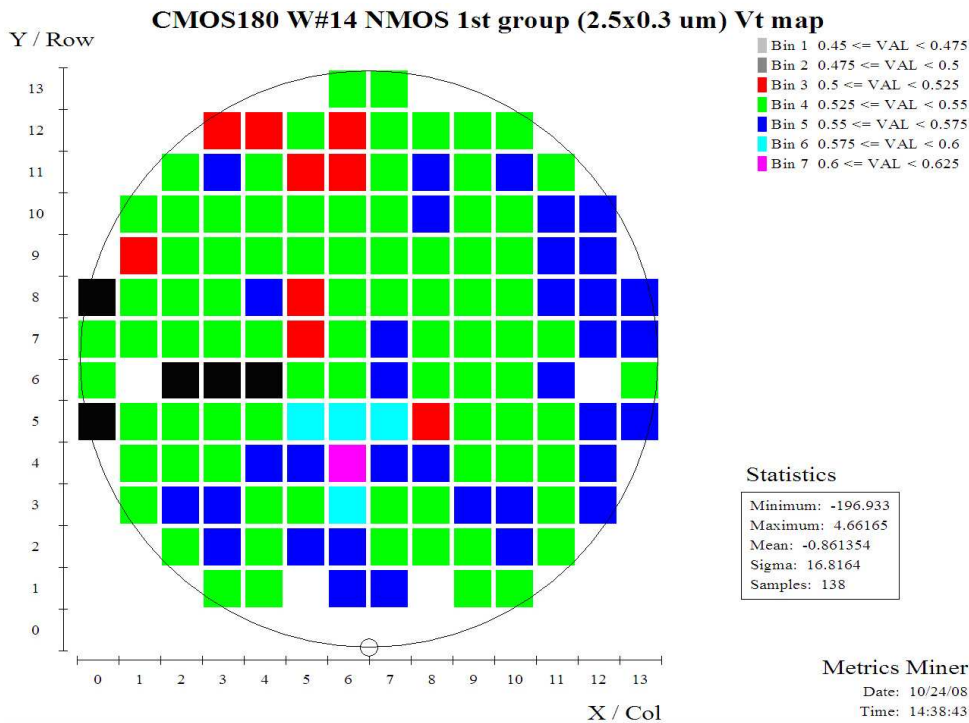
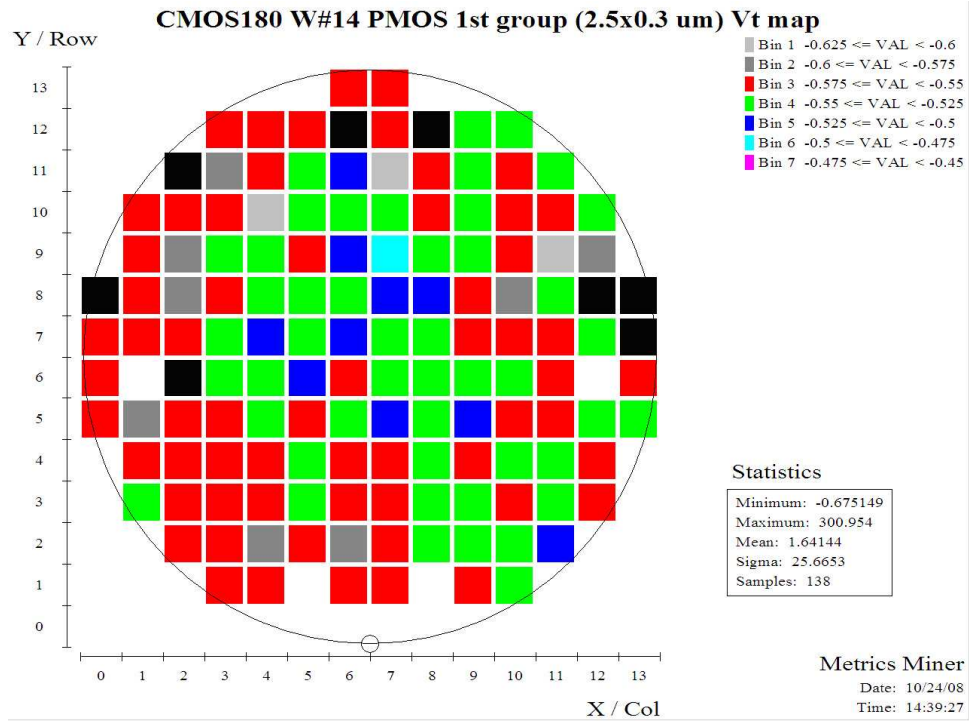
**Figure 10. Vt distribution maps of PMOS and NMOS transistors with in-house design rules (1st group)**



**Figure 11. Vt distribution maps of PMOS and NMOS transistors with  $\lambda=0.5 \mu\text{m}$  (2nd group)**



**Figure 12. Vt distribution map of PMOS and NMOS transistors with  $\lambda=0.35 \mu\text{m}$  (3rd group)**



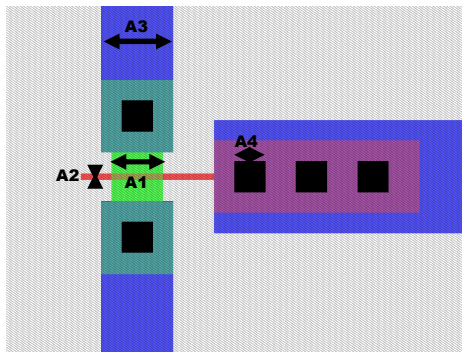
**Figure 13. Vt distribution maps of PMOS and NMOS transistors with Mix&Match lithography**

## Appendix D

### Layout design rules

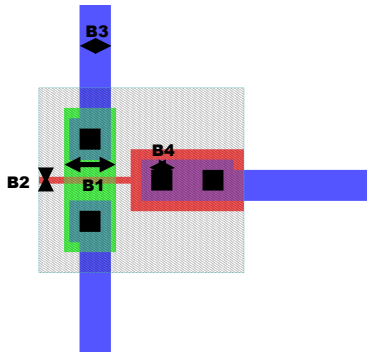
In the CMOS170 baseline process we introduced additional transistors with standard, lambda scaled design rules. The comparison of  $V_t$  distributions for NMOS and PMOS transistors in groups 1-3 are shown in Fig. 10-12.

*1st column of transistors with robust design (In house design rules applied)*



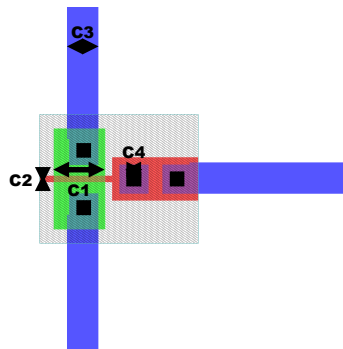
- A.1. Gate width: 2.5  $\mu\text{m}$
- A.2. Gate length: 0.3  $\mu\text{m}$
- A.3. Metal line width: 3.5  $\mu\text{m}$
- A.4. Contact hole: 1.5  $\mu\text{m}$

*2nd column of transistors with  $\lambda=0.5 \mu\text{m}$  (HP design rules applied)*



- B.1. Gate width: 2.5  $\mu\text{m}$
- B.2. Gate length: 0.3  $\mu\text{m}$
- B.3. Metal line width: 1.5  $\mu\text{m}$
- B.4. Contact hole: 1  $\mu\text{m}$

*3rd column of transistors with  $\lambda=0.35 \mu\text{m}$  (HP design rules applied)*



- C.1. Gate width: 2.5  $\mu\text{m}$
- C.2. Gate length: 0.3  $\mu\text{m}$
- C.3. Metal line width: 1.5  $\mu\text{m}$
- C.4. Contact hole: 0.7  $\mu\text{m}$

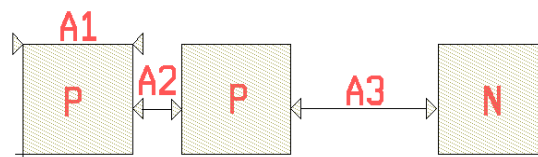


## Appendix E

### Suggested design rules for layout submission

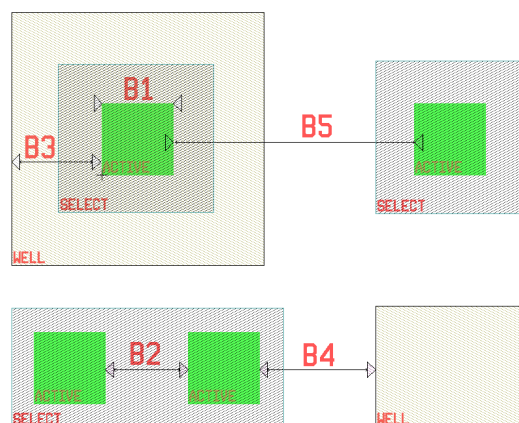
#### A. P and N Well

- A.1 Minimum size: 8.0  $\mu\text{m}$   
A.2 Minimum spacing for same potential: 3.6  $\mu\text{m}$   
A.3 Minimum spacing for different potential: 10.8  $\mu\text{m}$



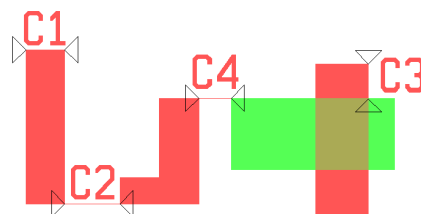
#### B. Active area

- B.1 Minimum size: 2.2  $\mu\text{m}$   
B.2 Minimum spacing: 3  $\mu\text{m}$   
B.3 Space to Well edge: 2.8  $\mu\text{m}$   
B.4 Space to Well: 3.2  $\mu\text{m}$   
B.5 Space between N+ and P+:



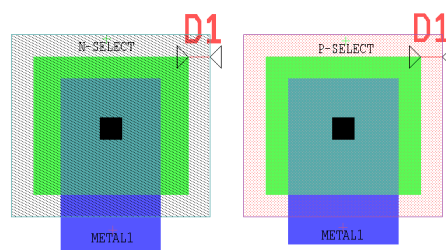
#### C. Poly

- C.1 Minimum size: 0.4  $\mu\text{m}$   
C.2 Minimum spacing: 2.2  $\mu\text{m}$   
C.3 Gate extension out of Active: 1.4  $\mu\text{m}$   
C.4 Minimum spacing to Active: 0.7  $\mu\text{m}$



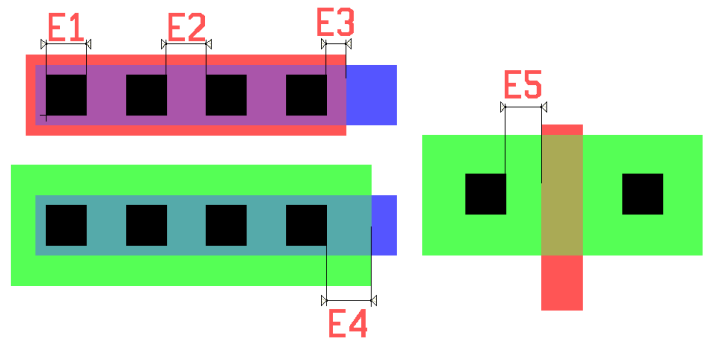
#### D. N and P Selects

- D.1 Minimum overlap of Active: 2  $\mu\text{m}$



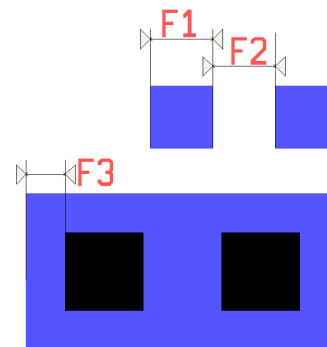
## E. Active and Poly Contacts

E.1 Minimum size:	2 $\mu\text{m}$
E.2 Minimum spacing:	2 $\mu\text{m}$
E.3 Minimum overlap by Poly:	1 $\mu\text{m}$
E.4 Minimum overlap by Active:	2 $\mu\text{m}$
E.5 Minimum spacing to Gate:	2 $\mu\text{m}$



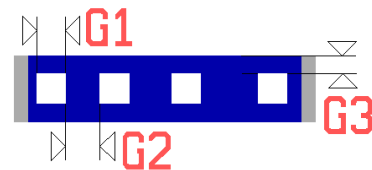
## F. Metal 1

F.1 Minimum size:	1.6 $\mu\text{m}$
F.2 Minimum spacing:	1.6 $\mu\text{m}$
F.3 Minimum overlap of Contacts:	1 $\mu\text{m}$



## G. Via

G.1 Minimum size:	3.0 $\mu\text{m}$
G.2 Minimum spacing:	4.0 $\mu\text{m}$
G.3 Minimum overlap by Metal1:	2.0 $\mu\text{m}$



## H. Metal 2

H.1 Minimum size:	3.0 $\mu\text{m}$
H.2 Minimum spacing:	3.0 $\mu\text{m}$
H.3 Minimum overlap of Via:	3.0 $\mu\text{m}$

